7100-30 MASS STORAGE SYSTEM

MAINTENANCE MANUAL

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1. INTRODUCTION

This section tells you what subjects are included in this manual and gives you an overview of the features and benefits of the 7100-30 Mass Storage System.

1.1 Scope of Manual

This manual describes the 7100-30 Mass Storage System. Included are a description of the boards in the system, system block diagrams, equipment installation procedures, subassembly replacement procedures, the troubleshooting menu, and preventive maintenance procedures.

1.2 Features and Benefits

CDC 170/180 Series Compatibility. The 7100-30 provides high-performance, online data storage for Control Data CYBER 170 and 180 computer systems. The 7100-30 is compatible with the 170 data channel and operates with any currently supported software level of the NOS, NOS/BE, or NOS/VE operating systems.

Disk Array Design. The 7100-30 stores data in an array of small, high capacity disk drives. An array of up to sixteen dual-ported disk drives is housed in the 7100-30 cabinet for a total of 8.83 billion bytes of disk storage.

Small Footprint. A 7100-30 containing the dual controller and up to sixteen disk drives has a footprint of only 12.13 square feet.

FIPS Compliancy. The 7100-30 uses an Enhanced Storage Module Device (ESMD) interface and therefore comply with FIPS 111.

Performance. Disk drives provide average seek times of 16 milliseconds.

Reduced Energy Consumption. Lower power consumption and less heat dissipation reduce utility bills.

Installation. The 7100-30 is easily installed. No operating system changes or additions are required except configuring the operating system to support a standard CDC 7155/885 disk system.

A block diagram of the 7100-30 (figure 1-1) is provided on the following page.

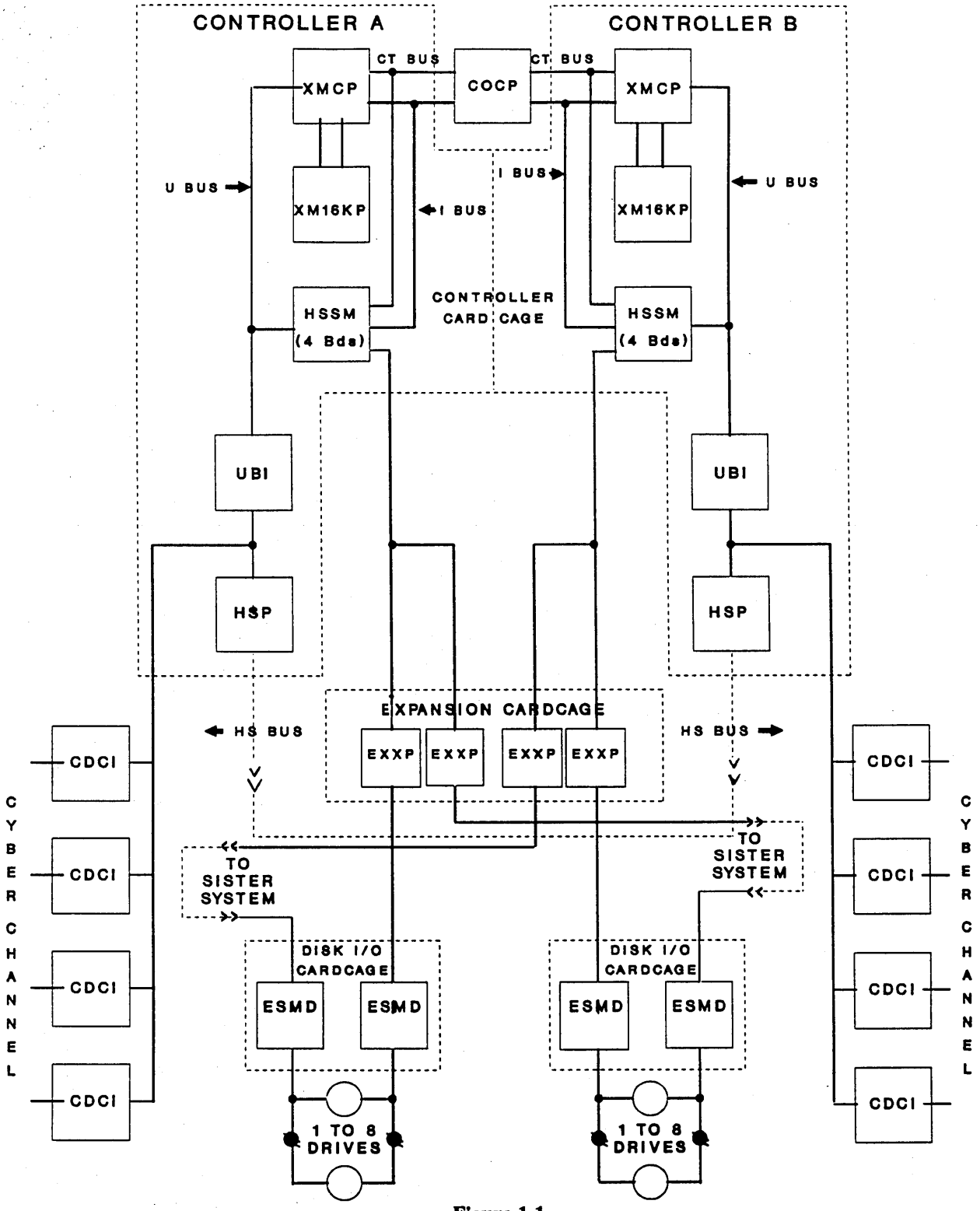


Figure 1-1
7100-30 Mass Storage System Block Diagram

2. SYSTEM DESCRIPTION

This section provides the user with a functional description of each of the features that comprise a 7100-30 Mass Storage System.

A 7100-30 contains a dual controller containing two independent controllers; up to four channel interfaces per controller to the host; and a data storage base made up of up to sixteen disk drives. Figures 2-1 through 2-3 show a front view of the outside of the 7100-30 cabinet and a front and rear view of the components which may be contained in the 7100-30 cabinet.

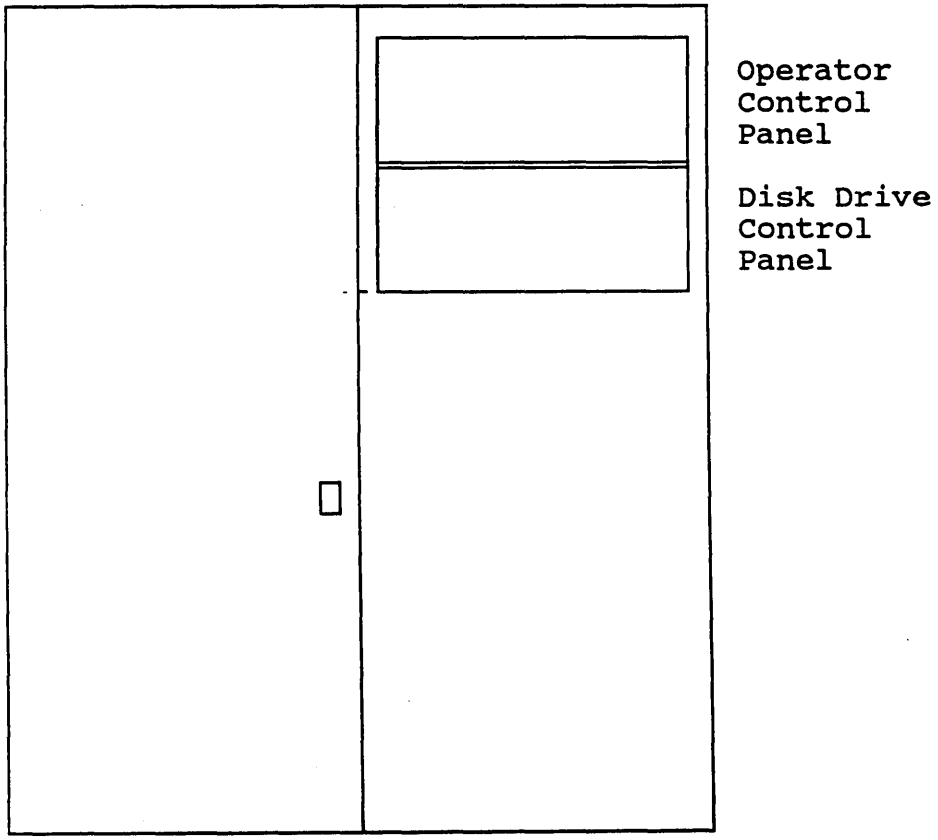


Figure 2-1
Front View of Outside of 7100-30 Cabinet

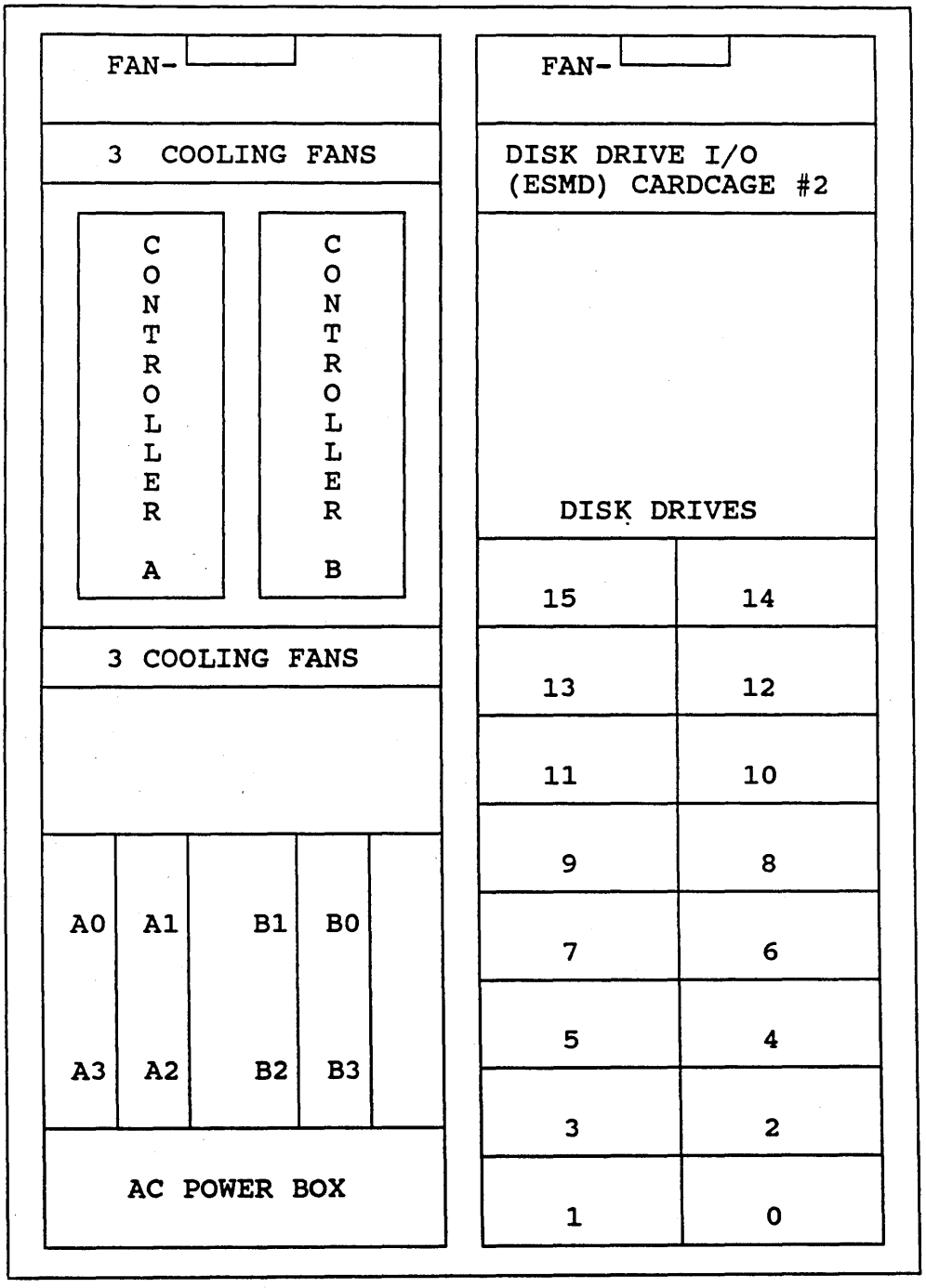
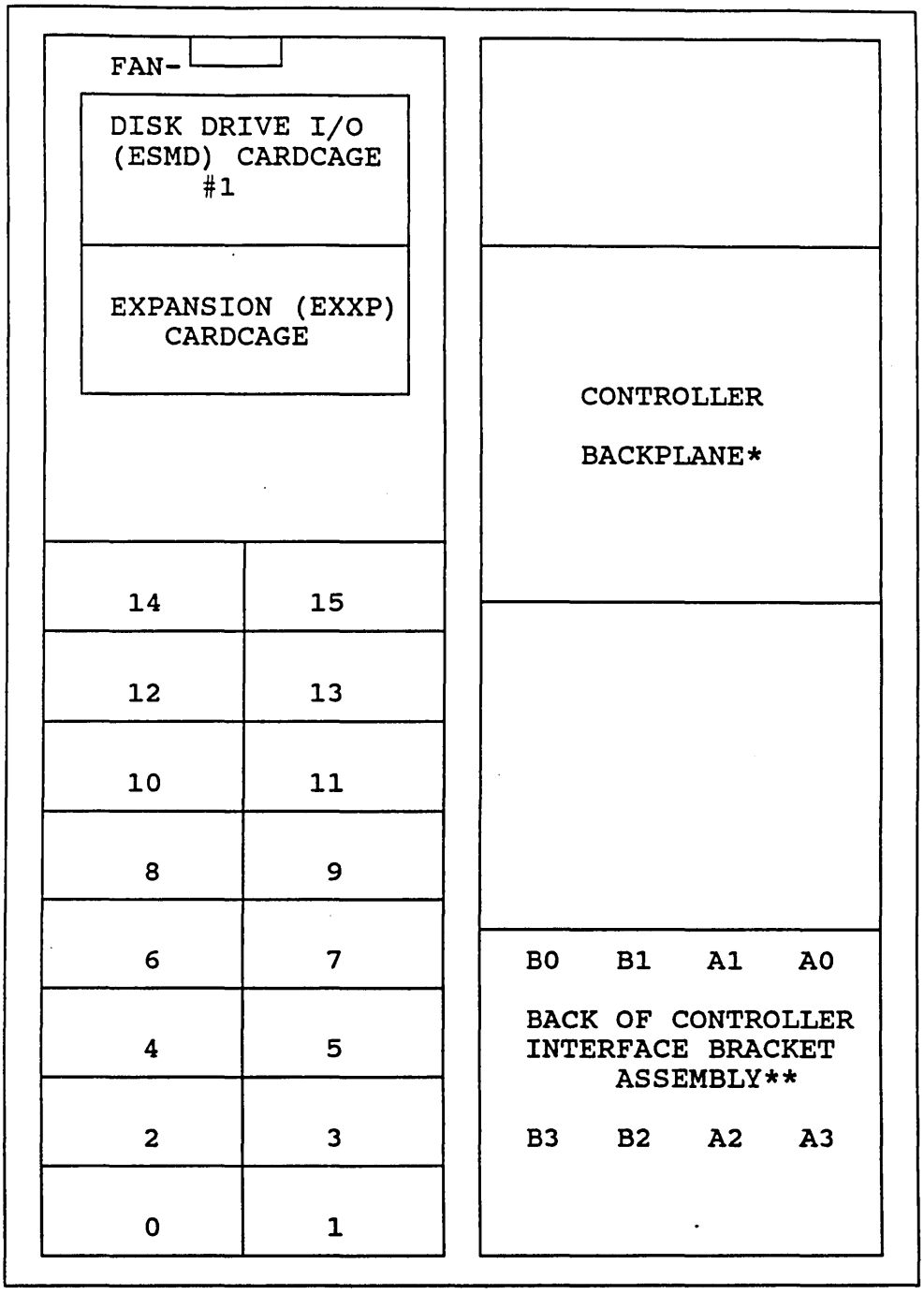


Figure 2-2
Front View of Inside of 7100-30 Cabinet



* The back panel covers the controller backplane; on the inside of the back panel are the five system power supplies: OCP, channel A (+5V and -5V) and channel B (+5V and -5V).

** A metal sheet covers the back of the controller interface bracket assembly.

Figure 2-3
Rear View of Inside of 7100-30 Cabinet

2.1 Dual Controller

The dual controller is intelligent, microprogrammed, and controls all the functions for direct access storage operations. It contains two independent controllers that emulate Control Data 7155 controllers. Each controller is capable of operating its storage devices should the other controller be offline.

Operation is via the standard Control Data CYBER device handler without modifications. The following operations are executed by the dual controller:

- o Receives and interprets control information from the I/O channels
- o Directs the activity of the selected storage device
- o Accepts data read from the selected disk drive and transfers the data over the CYBER channel to the 170/180 Series central system processor.
- o Routes the data received from the I/O channel to the selected drive and controls the writing of this data on drives.
- o Executes command retry and error recovery without host intervention

The above operations are handled by the dual controller via the boards in the system. These boards are located in the dual controller cardcage (figure 2-4) and are comprised of the following:

XMC — contains the microprocessor that controls all disk drive functions. It communicates with and commands the devices that comprise the mass storage system. The XMC is located in slot E of controller A and slot Q of controller B.

XM16KP — provides the storage area for the microprogram code which is used for the operation of the processor in the XMC. The XM16KP is located in slot F of controller A and slot P of controller B.

UBI — provides an external interface between the XMC and the host channel adapter; converts the CDC 12-bit data bus to the Amperif 36-bit U-bus. The UBI is located in slot H of controller A and slot N of controller B.

HSP — generates checksums on data during writes and validates these during reads. Maintains sources and destinations of data and generates address-related information to ensure proper addressing. The HSP is located in slot J of controller A and slot M of controller B.

The following boards are part of the HSSM which comprises the section that interfaces between the controller and the disk drives.

XMCIP — interfaces with the controller. The XMCIP is located in slot D of controller A and slot R of controller B.

MDBP — buffers the data. The MDBP is located in slot C of controller A and slot S of controller B.

MPCP — controls the operation of all the HSSM boards. The MPCP is located in slot B of controller A and slot T of controller B.

DIFE — interfaces with the disk drive. The DIFE is located in slot A of controller A and slot U of controller B.

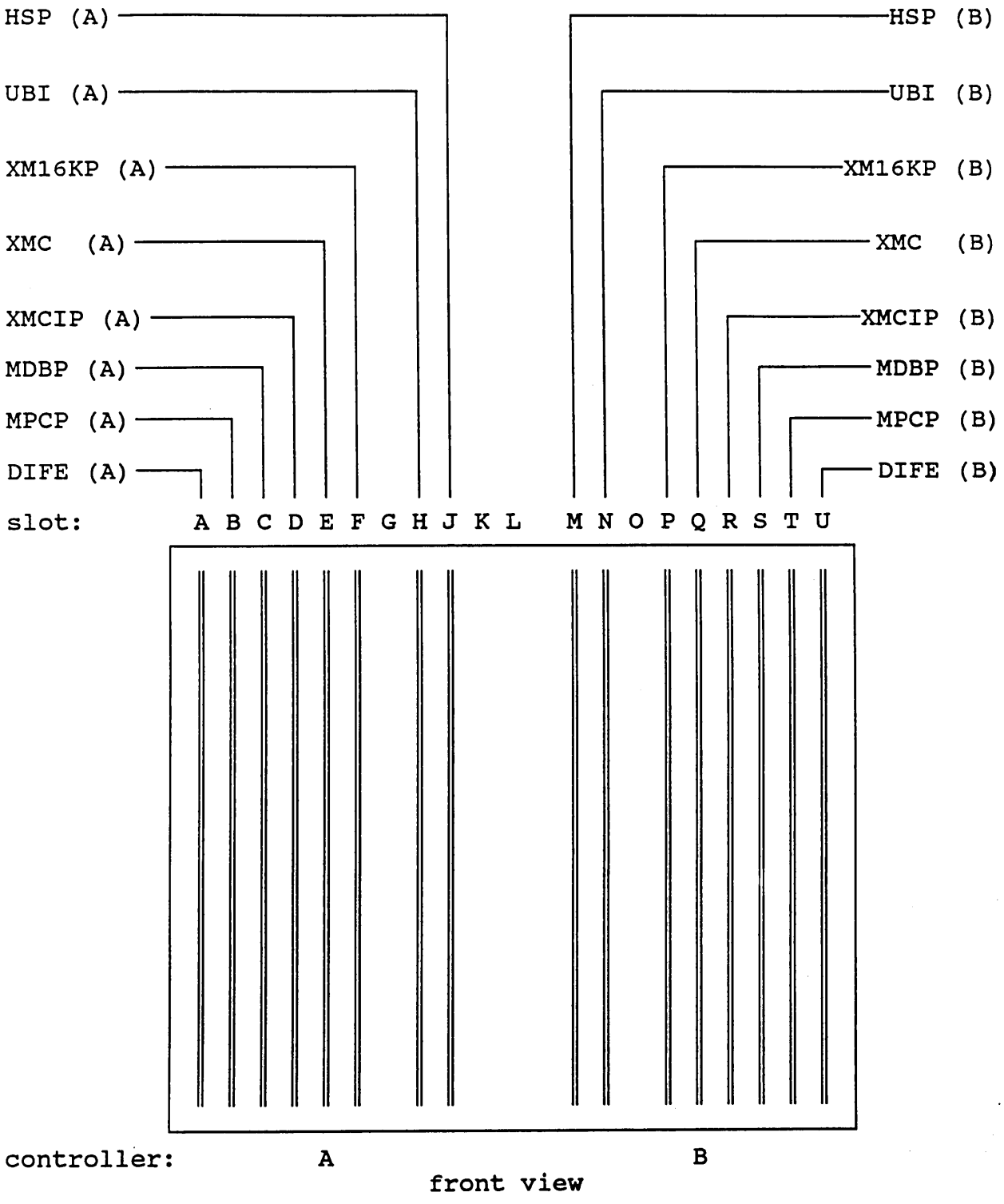


Figure 2-4
Dual Controller Cardcage

2.1.1 Channel Interface

The dual controller employs CYBER channel I/O protocol to communicate with the CDC computer system. Communication between a CDC channel and the dual controller takes place by transferring 12-bit data words, function words, and status words.

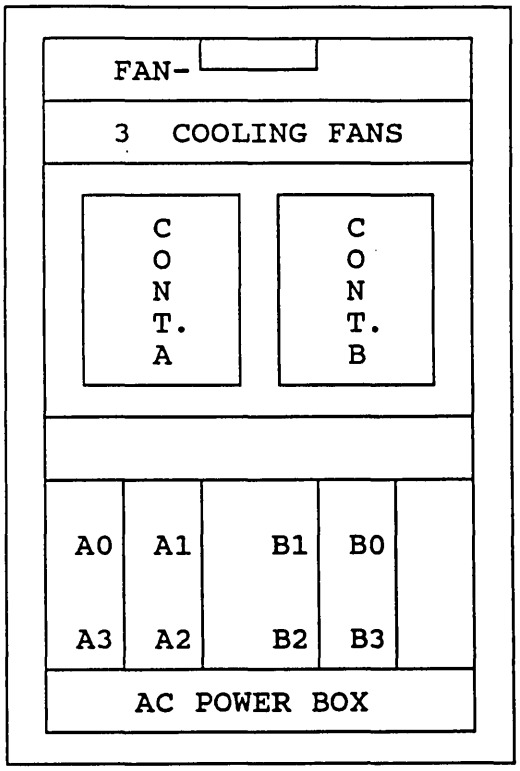
Each of the two independent controllers in the dual controller is attached to one channel of the CDC system. Optional channel interface expansion units allow each controller to be attached to a maximum of four host channels; thus, the dual controller may communicate with two to eight channels.

One mass storage system may be attached to up to eight hosts. Each half of the dual controller may be shared by up to four hosts, any of which can access each shared device.

The CDCI and UBI provide the channel interface between the CDC channel and the internal U-bus of the dual controller. See figure 2-5 for a view of the channel interface bracket assembly (where the CDCI boards reside) and figure 2-6 for the cable locations on the dual controller cardcage.

2.1.2 Data Integrity

Protection from data transfer errors is provided by parity checking, which takes place throughout the data path in the dual controller and through the channel. The microprogram contained in the dual controller performs automatic error recovery in a manner transparent to the system. Error and usage counters are maintained in the dual controller for each disk drive, whether or not the error is recoverable. In the case of recoverable errors, the error is recovered and the host CPU is not notified. In the case of nonrecoverable errors, the host CPU is notified that an error has occurred.



front view of inside of 7100-30 cabinet (left-hand side of the cabinet only)

CHANNEL INTERFACE BRACKET ASSEMBLY

four racks: each rack holds two CDCI boards

one rack holds two CDCI boards

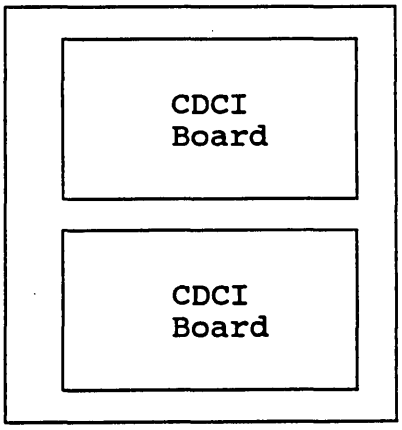


Figure 2-5
Channel Interface Bracket Assembly with CDCI Boards

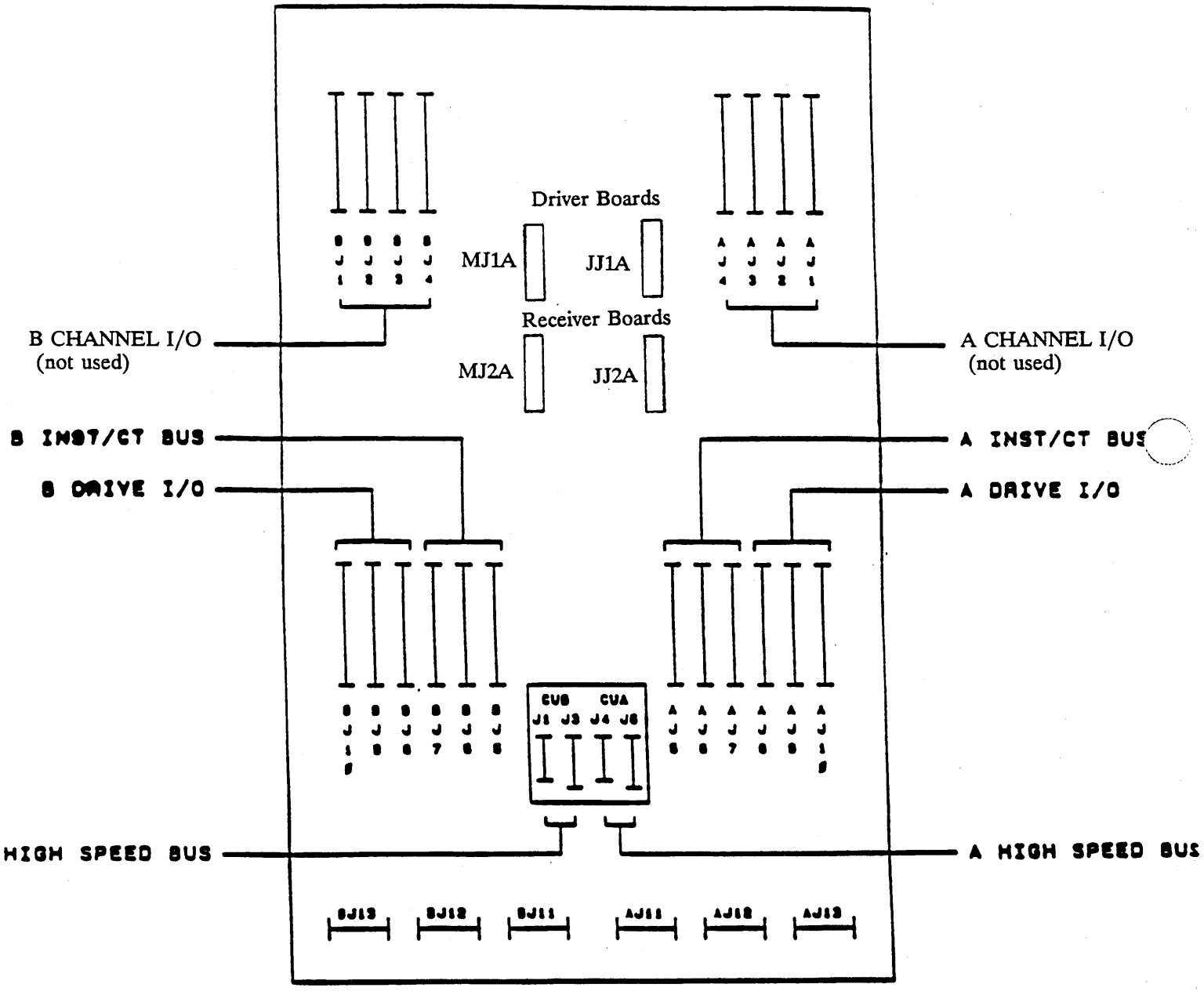


Figure 2-6
Cable Socket Locations on the Dual Controller Cardcage

2.2 Expansion Cardcage (EXXP)

The expansion cardcage contains four EXXP boards: two for each controller. The EXXP boards act as buffers for DIFE ECL logic going to the disk drive I/O cardcage. The EXXP boards for controller A are located in slots E and G, and the EXXP boards for controller B are located in slots J and L. See figure 2-7 below.

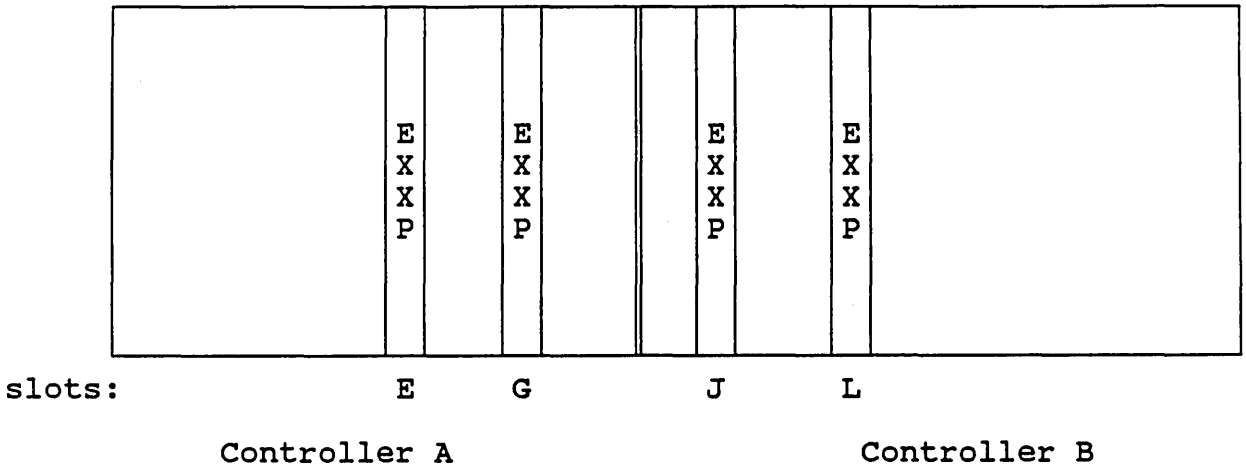


Figure 2-7
Expansion (EXXP) Cardcage

2.3 Disk Drive I/O Cardcages (ESMD)

There are two disk drive I/O cardcages in each 7100-30 system. Each of these cardcages contains the same four types of boards for controller A and controller B. Descriptions of the boards in these cardcages follow and they are shown in figure 2-8.

AIX provides receivers, drivers, and level translation logic required to interface the A cable signals with the EXXP cardcage. The AIX boards are located in slot A for controller A and in slot Y for controller B.

AIO provides receivers, drivers, and level translation logic required to interface the A cable signals with the ESMD interface. The AIO boards are located in slot B for controller A and in slot W for controller B.

BIX provides receivers, drivers, and level translation logic required to interface the B cable signals with the EXXP cardcage. The BIX boards are located in slot D for controller A and in slot V for controller B.

BIOE (In each disk drive I/O cardcage there are one to four BIOE boards for controller A and one to four BIOE boards for controller B.)

provides the receivers, drivers, and level translation logic required to interface with a specific disk drive. The BIOE boards are located in slots E, F, G, and H for controller A, and slots N, O, P, and Q for controller B. Each BIOE board interfaces with two disk drives; the particular disk drives each BIOE board interfaces with depends on whether you are looking at disk drive I/O cardcage #1 or #2. The specifics are listed below.

Disk drive I/O cardcage slot	cardcage #1 drive numbers	cardcage #2 drive numbers
E	0-1	8-9
F	2-3	10-11
G	4-5	12-13
H	6-7	14-15
N	0-1	8-9
O	2-3	10-11
P	4-5	12-13
Q	6-7	14-15

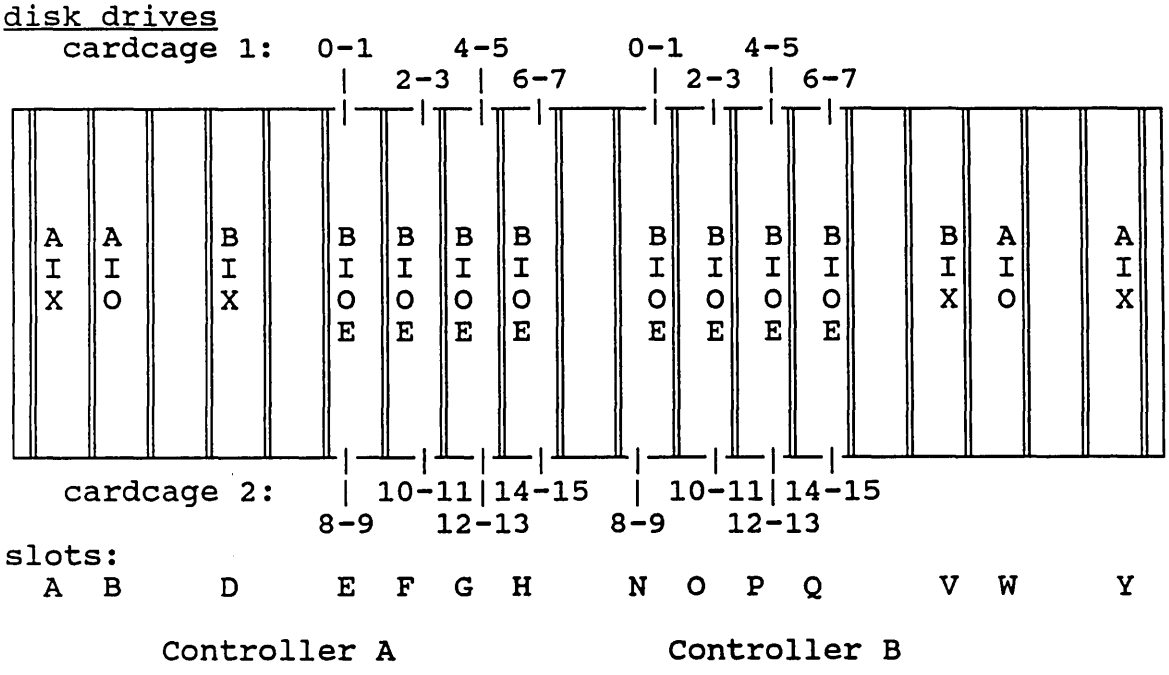


Figure 2-8
Disk Drive I/O Cardcage

2.4 9720 Disk Drives

The 9720-1230 disk drive emulates the CDC 885 disk unit. Managed by the dual controller, the drives store information on selected drive surfaces or read information from them. The 9720 contains the electronics required to perform the following functions:

- Rotate the drive at the proper speed
- Position the read/write heads at a particular cylinder (perform a seek operation)
- Transfer data to/from the accessed area on the drive

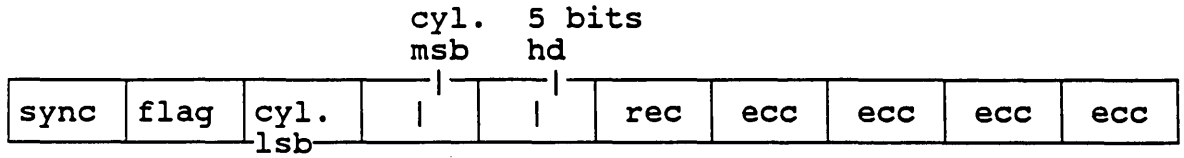
The disk drives are random access mass storage devices using movable heads and rotating disks. A 7100-30 contains up to sixteen disk drives.

2.4.1 Track Organization

Physical Track. A track is one complete disk revolution. The physical track begins at an index point and continues until the index point is reached again. One index point serves the entire drive in indicating the physical beginning of all tracks.

Each track has the same basic organization and consists of equal-length data records. Data records are 522 bytes. A record consists of a header area and a data area. See figure 2-10 for illustration.

Header Area. The header area contains information about where the record is stored and how to access the information it contains. It contains the address and length of the data record, and an error detection code (ECC for the header). The header area is composed of ten sections, each of which is one byte in length. Additional information on the sync and flag bytes is given below in figure 2-9.



Sync = AA
flag byte

0	Defective track	
1 2 3	\ -Drive type /	1 = Sabre 5 (9720)
4 5	Record length "	1 = 116 WD
6 7	Emulation "	0 = 8470

Figure 2-9
Header Area

Data Area. The data area contains information defined by the user. An error correction code (ECC) is appended to the data area. The ECC contains a 35-bit detection and 12-bit correction capability (per physical record), thus enabling the system to correct data that has been erroneously recorded due to drive flaws.

Defective/Alternate Tracks. Should a drive track become defective, it is possible to substitute an alternate track for the defective track. An inline diagnostic (ILD) may be started from the operator control panel (OCP) to mark a given track as no longer usable and assign a track from a special reserved area to replace the defective track. Once an alternate track is assigned, its use is transparent to the user. This process guarantees that the drive space as specified is always available for use.

2.4.2 Data Integrity

All drive storage operations are protected from flaws in the storage medium by an error correction code (ECC), which can detect any 35-bit burst that is in error and is able to self-correct any 12-bit burst in error for each physical record. Should any drive error occur, the information is recorded in an error log in the control unit.

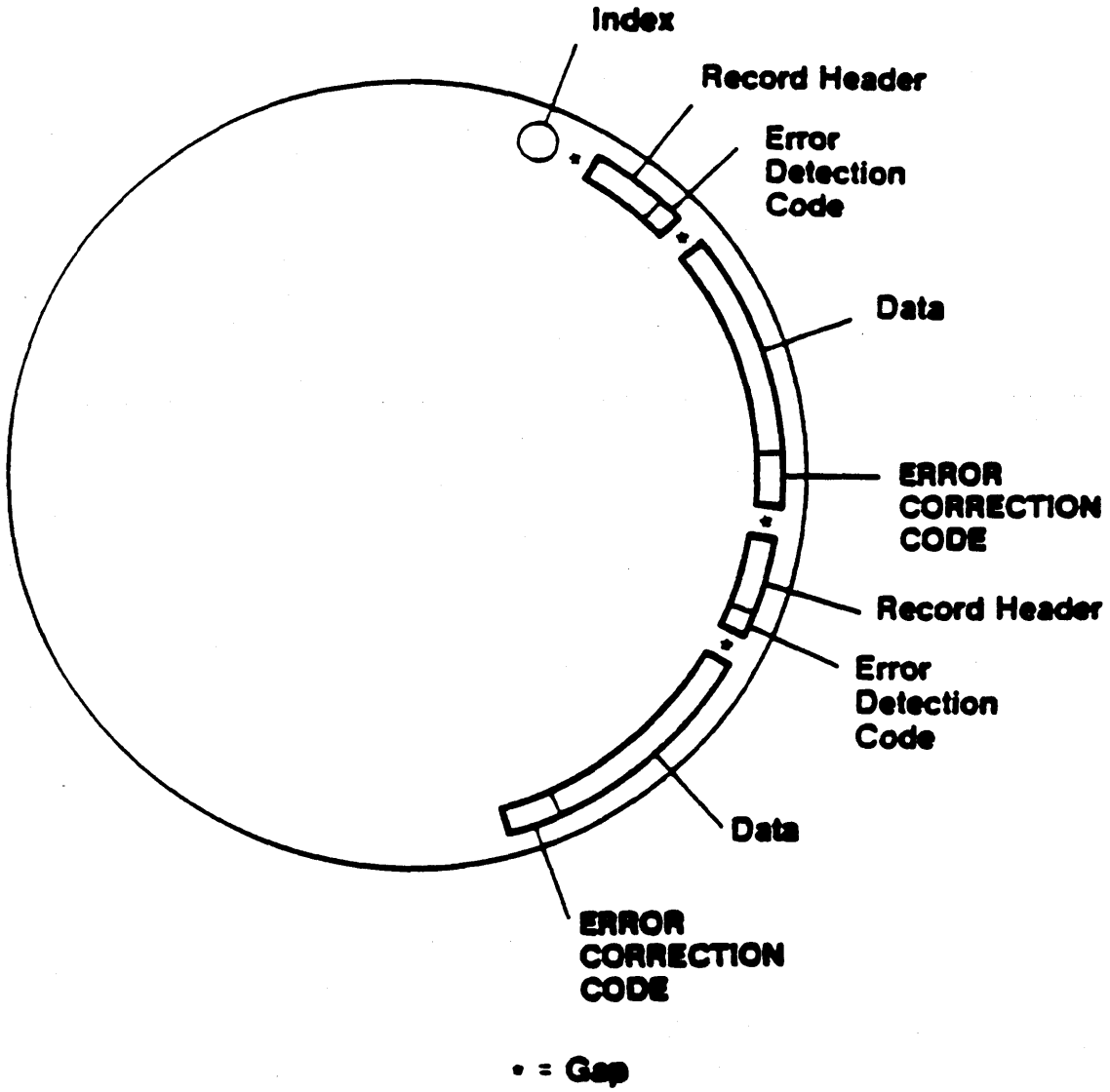


Figure 2-10
Track Organization

2.5 Operator Control Panel

Functions such as monitoring system status, system reset, changing drive states, and running offline system diagnostics are performed at the operator control panel (OCP). When commands are entered at the OCP, the user must have the appropriate level of clearance to execute a given command. Clearance is acquired by entering a correct password. There are three clearance levels:

- Monitoring
- Operator
- Engineering

To ensure protection of data during normal operation, the OCP can be set to disallow all system commands and allow only display functions. This is done by setting the clearance level to monitoring level clearance.

With operator level clearance, the operator may enter system commands such as setting time of day or changing drive caching states. Maintenance and diagnostic routines may also be performed under operator level clearance.

Under engineering level clearance, all functions may be performed.

See figure 2-11 and 2-12 for illustrations of the OCP and gates.

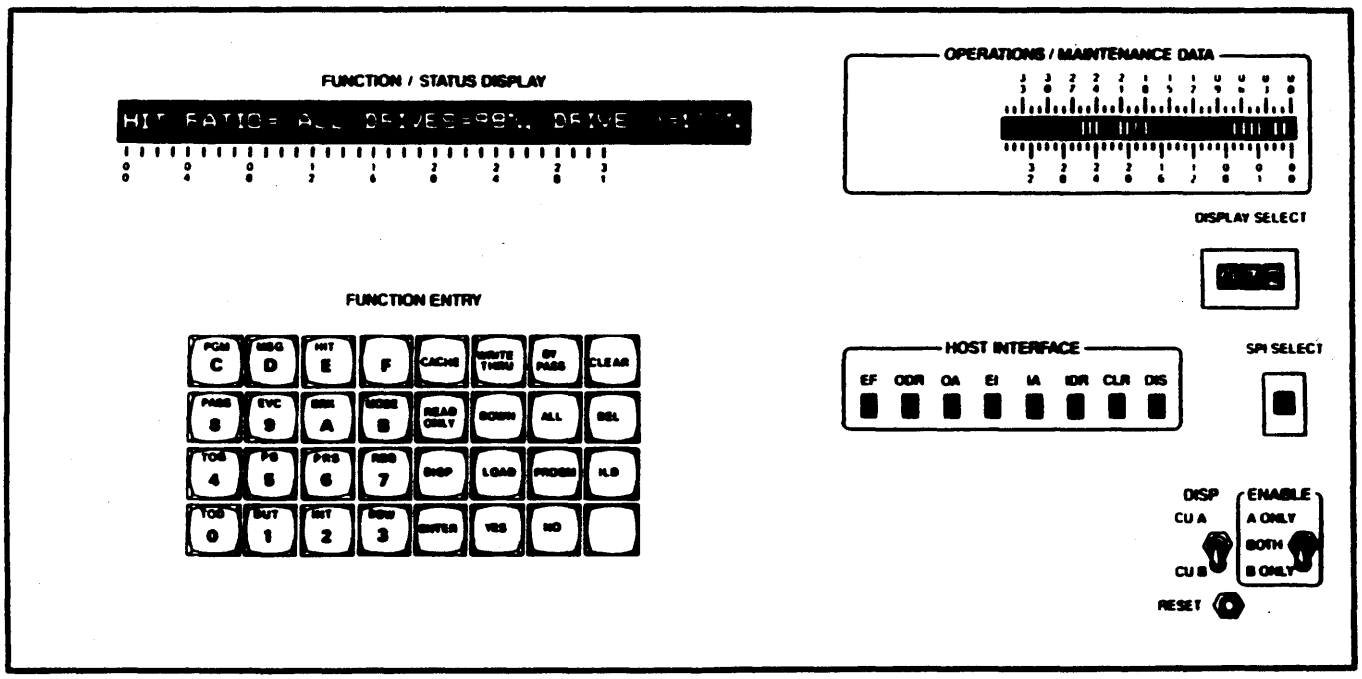
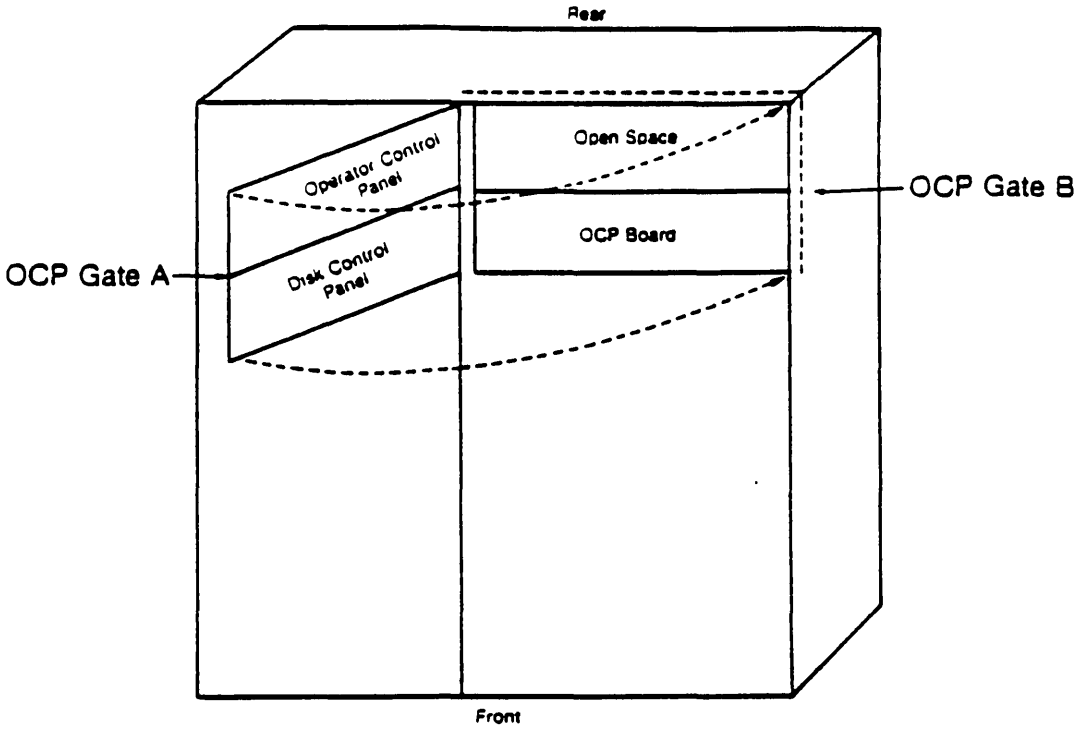
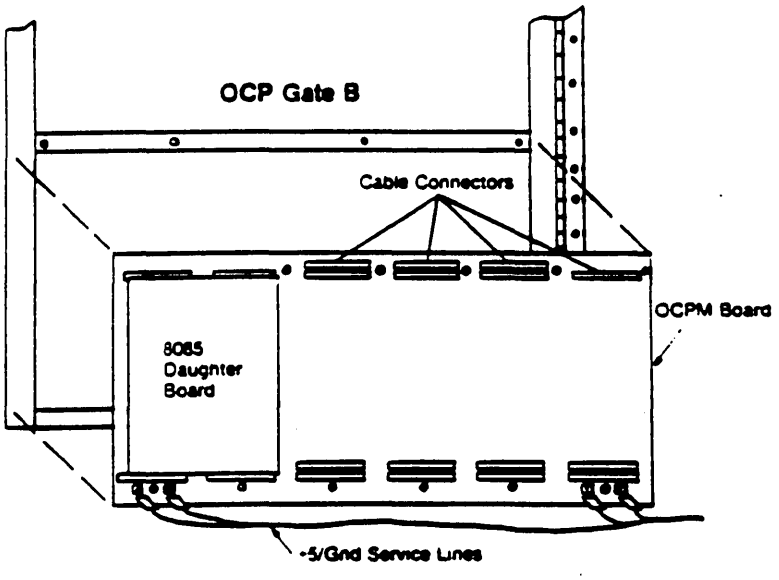


Figure 2-11
Operator Control Panel





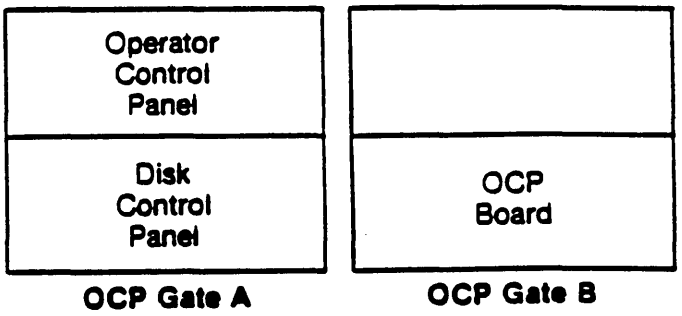


Figure 2-12
OCP Gates

2.6 Disk Drive Control Panel

The disk drive control panel contains 16 sets of switches and indicators which are used to operate the disk drives. Each set operates an individual disk drive and includes the switches and indicators described below. In addition, the panel contains a drive operation area. See figure 2-13 for an illustration of the disk drive control panel.

Disk drive switches and indicators

Each disk drive has the switch and indicators described below. (The expressions in parentheses are those which actually appear on the panel.)

Drive select switch (DR)	When pressed, this switch selects the drive.
Selected indicator (SLTD)	When lit, this indicator shows that the drive has been selected (individually or as part of a SELECT ALL) and will perform the drive operation chosen.
Power indicator (PWR)	When lit, this indicator shows that the drive has spun up.
Fault indicator (FLT)	When lit, this indicator shows that there is a fault on that disk drive.
Write protect indicator (WP)	When lit, this indicator shows that the disk drive is in write protect mode. (It was put in write protect mode from the disk drive control panel.)
Ready indicator (RDY)	When lit, this indicator shows that the disk drive is rotating at full speed and is ready to accept commands from the controller.
Channel A indicator (CHA)	When lit, this indicates that controller A is enabled; this means that you can access a disk drive through controller A.
Channel B indicator (CHB)	When lit, this indicates that controller B is enabled; this means that you can access a disk drive through controller B.

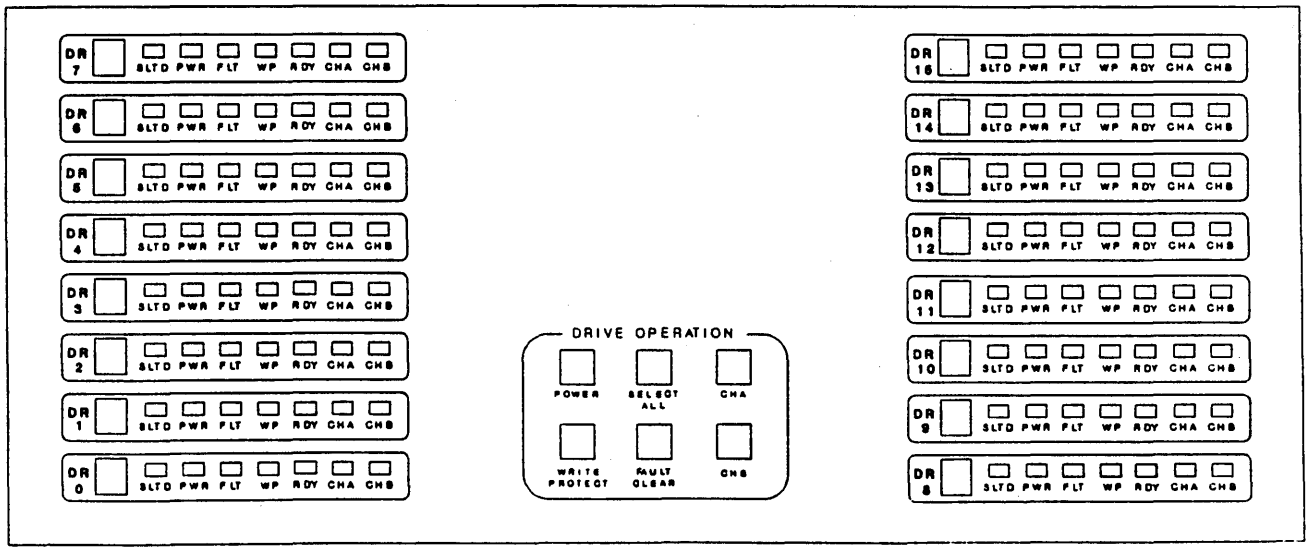


Figure 2-13
Disk Drive Control Panel

Drive operation area

Operator functions are selected at the disk drive operation area. Each disk drive has a switch and a set of indicators. The following switches appear on the disk drive operation area of the disk drive control panel. (The expressions in uppercase type are those which actually appear on the panel.)

POWER switch	When pressed, this push button will power up the drive.
SELECT ALL switch	When pressed, this switch selects all the disk drives at once. Pressing this switch causes the SLTD (selected) indicator for each disk drive to light up.
CHA switch	When pressed, this push button enables or disables the disk interface for the A controller (for the selected disk drive, or for all disk drives if you pressed SELECT ALL).
WRITE PROTECT switch	When pressed, this push button enables or disables the write protect mode for the selected disk drive(s). When a disk drive is in write protect mode, the WP indicator for that disk drive is lit and neither controller can write to that disk drive.
FAULT CLEAR switch	When pressed, this push button resets the electronic portion of a disk drive.
CHB switch	When pressed, this push button enables or disables the disk interface for the B controller (for the selected disk drive, or for all disk drives if you pressed SELECT ALL).

2.7 Power Supplies

There are five main power supplies in the 7100-30 (see figure 2-14). These power supplies supply the DC power to the entire 7100-30 system excluding the disk drives. The supplies, which are single phase, are capable of operating from a system three-phase source of 200-250 VAC at either 50 or 60 Hz.

1. OCP power supply, +5V
   Supplies +5V DC power to the OCP.

2. Controller A power supply, +5V
   Supplies +5V DC power for controller A, ESMD-I/O cardcages, EXXP cardcage, and the CDCIs.

3. Controller A power supply, -5V
   Supplies -5V DC power for the controller ESMD-I/O cardcages, and the EXXP cardcage.

4. Controller B power supply, +5V
   Supplies +5V DC power for controller B, ESMD-I/O cardcages, EXXP cardcage, and the CDCIs.

5. Controller B power supply, -5V
   Supplies -5V DC power for the controller ESMD-I/O cardcages, and the EXXP cardcage.

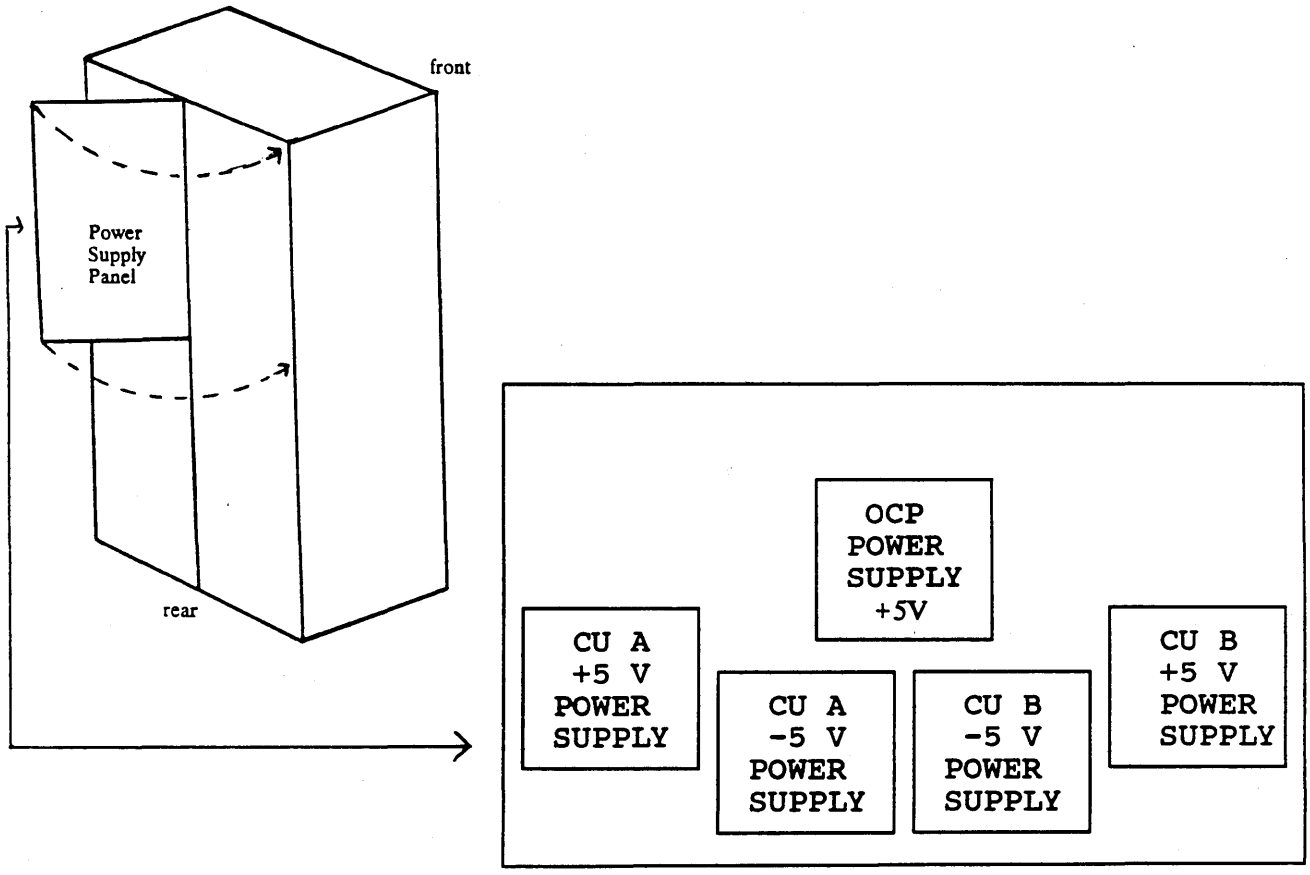

front
Power Supply Panel
rear
OCP POWER SUPPLY +5V
CU A +5 V POWER SUPPLY
CU A -5 V POWER SUPPLY
CU B -5 V POWER SUPPLY
CU B +5 V POWER SUPPLY

Figure 2-14
Power Supply Panel

3. SYSTEM CONFIGURATION

The controller is basic and necessary to every 7100-30. In addition, the data storage base included consists of one to sixteen disk drives. There are two possible 7100-30 configurations; these are illustrated in figures 3-1 and 3-2 and are described below.

3.1 Controller

This section describes the channel interface and the 7100-30 cabinet.

3.1.1 Channel Interface Configuration

The 7100-30 contains two I/O channel interface assemblies, one for each controller in the 7100-30. (Though some 7100-30's may only contain a single controller.) These interfaces allow two 170/180 Series CYBER channels to access their respective controllers within the system.

By selecting the channel interface expansion feature, the interface capability may be expanded to accommodate a maximum of eight I/O channels. With the maximum configuration, any one of a set of four I/O channels may access the first controller and any other one (of another set of four channels) may access the second controller.

3.1.2 7100-30 Cabinet

This cabinet houses all logic, wiring, channel interface assemblies, controls and indicators essential to controller operation. In addition, the cabinet provides space for sixteen 9720 disk drives and individual power supplies. The drives are mounted on drive trays which can slide out of the cabinet and there are two drives per drive tray.

3.2 Storage Device Configuration

If your system is configured as a standalone unit (not connected to a sister unit), then both sides of the dual controller can access all of the disk drives (one to sixteen) within the 7100-30 cabinet.

If your system is configured with a sister system, then each side of the dual controller can access from one to eight disk drives in your system, along with one to eight drives in the sister system.

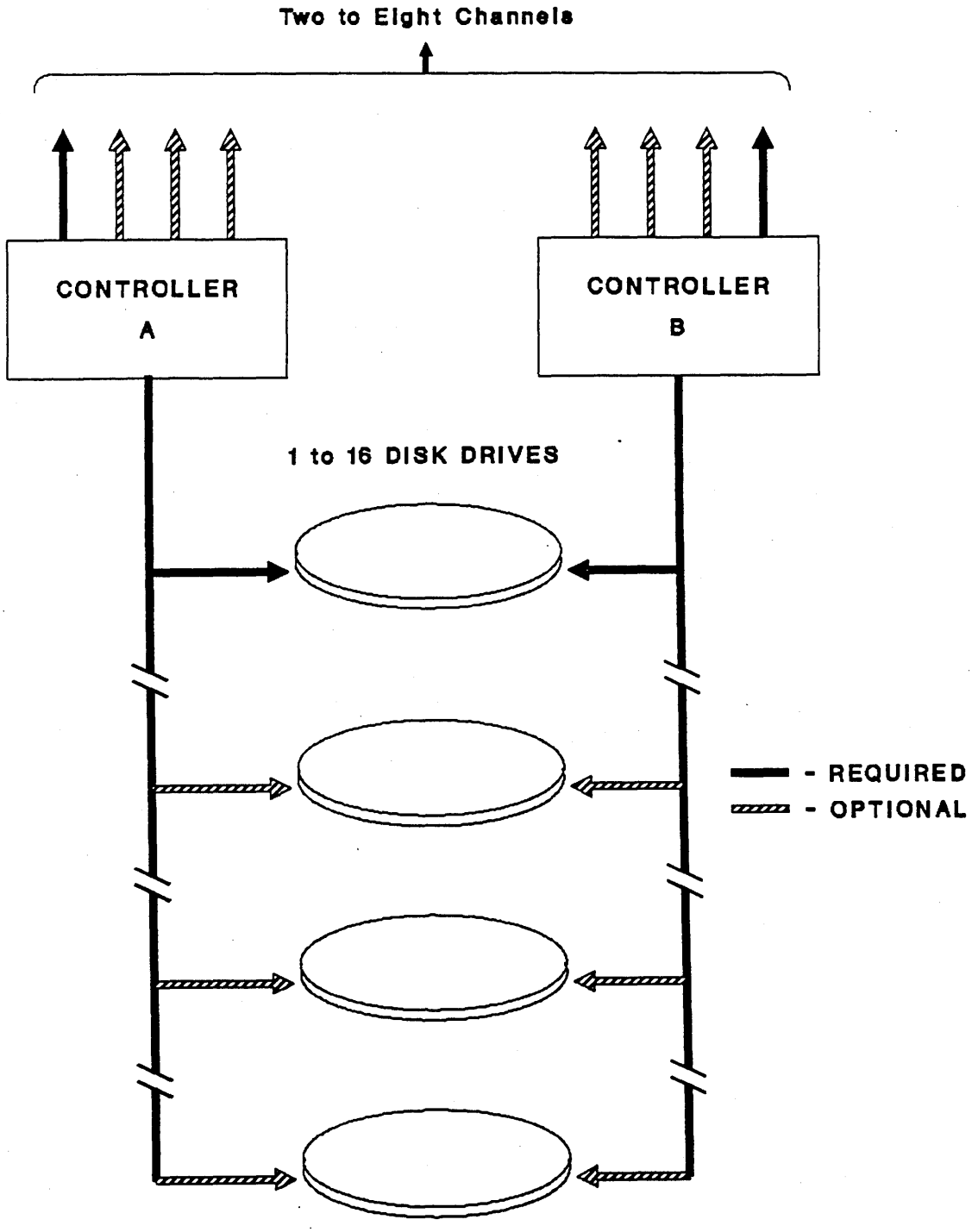


Figure 3-1
7100-30 Mass Storage System Configuration: As a Standalone Unit

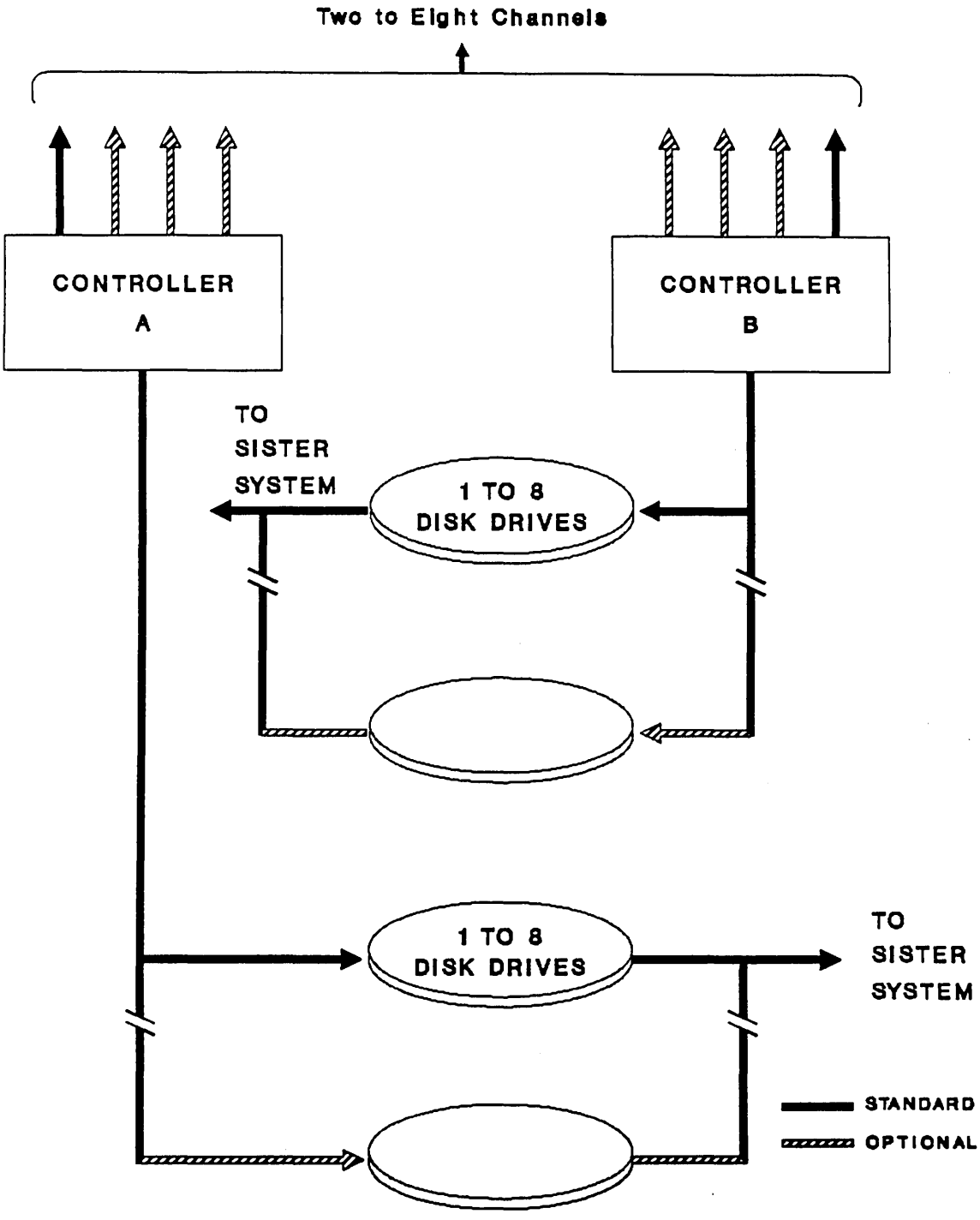


Figure 3-2
7100-30 Mass Storage System Configuration: With a Sister System

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4. SYSTEM SPECIFICATIONS

This section contains specifications for the dual controller and the disk drives.

Dual Controller Performance

Characteristic	Specification
Microinstruction execution time	5 million instructions/second
System bus bandwidth	25.0 megabytes/second

Dual Controller Physical Characteristics

Dimensions

Height	72.5 inches
Width	44.5 inches
Depth	39.3 inches

Front/Rear Clearance 36/36 inches

Weight

Dual controller and cabinet (With 16 disk drives)	1808 lb.

Power Requirements

Voltage - 3 Phase-AC	208 delta	220/ 380 Wye	240/ 415 Wye
Frequency - hertz	60 Hz	50 Hz	50 Hz
Current max - amps per phase	13.2	13.5	13.5
Apparent Power - kva	5.2	6.0	6.1
True Power - kw	5.1	5.9	6.0
Power Factor	.99	.98	.98
Heat Dissipation- Btu/hr	17,500	20,000	20,500
User Circuit Wires	4	5	5
Power Source Receptacles	Specified and provided by installation.		
Logic Ground Connections	Separate logic and ground connections.		

Environment

Operating Temperature	50°F to 90°F (10°C to 32°C)
Shipping Temperature	-40°F to 140°F (-40°C to 60°C)
Operating Humidity	20% to 80%
Shipping Humidity	5% to 90% noncondensing

Disk Drive Performance
(9720)

Characteristic	Specification
Minimum seek time	5 milliseconds
Average seek time	16 milliseconds
Maximum seek time	30 milliseconds
Average latency	8.33 milliseconds
Average access time	24.3 milliseconds
Instantaneous transfer rate	3.0 megabytes/second
Sustained transfer rate	2.6 megabytes/second
Rotational speed	3,600 rpm
Disk drive storage capacity	
formatted	552 megabytes (885 capacity)
unformatted	1.23 gigabytes
Records per track	67 records @ 522 megabytes/record

Disk Drive Physical Characteristics
(9720)

Weight	
1 disk drive (including power supply)	40.8 lb.

For more detailed information, see Imprimis Product Specification #64402300.

5. OCP INDICATORS AND OPERATING FUNCTIONS

This section describes the indicators on the operator control panel (OCP), the operating functions which can be performed there, and the error messages which can be displayed there. In addition, there is a discussion of offline diagnostics and utilities for the 7100-30.

5.1 Operator Control Panel

Except for the power switches, all controls for the mass storage system are handled through the operator control panel (OCP). The OCP (see figure 5-1) displays the system status and allows system functions and commands to be initiated.

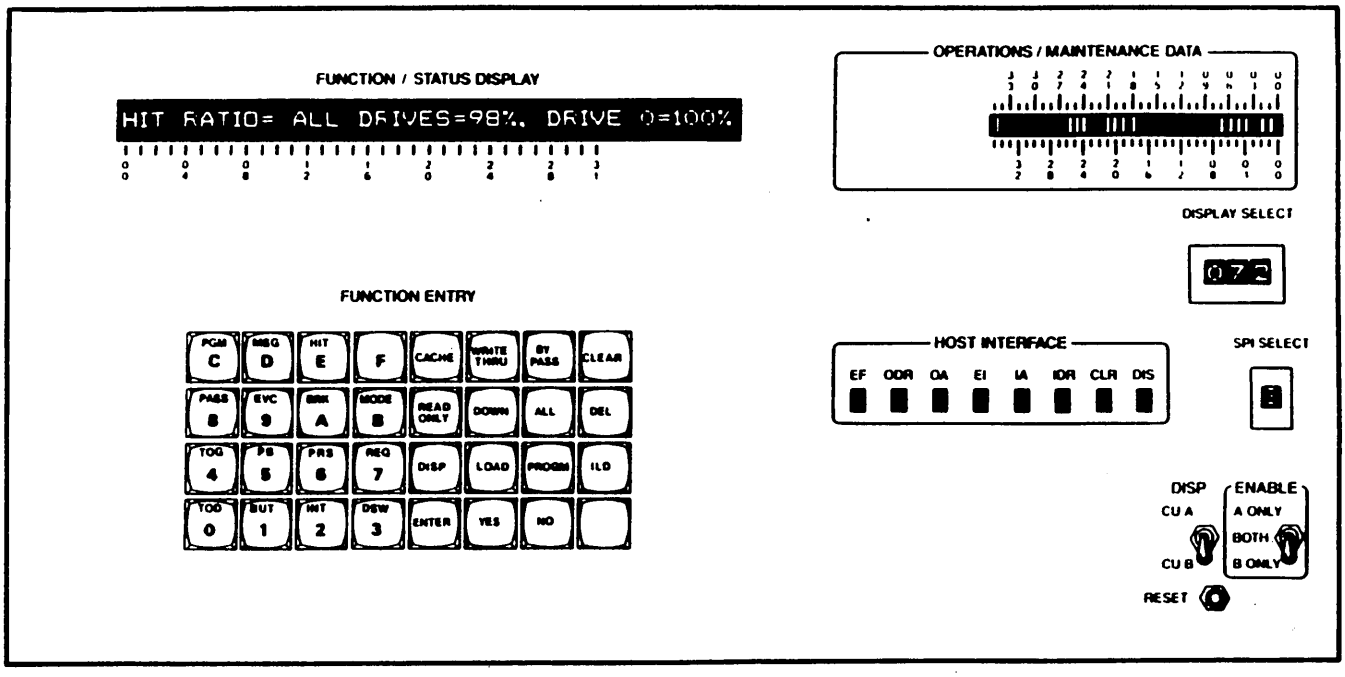

Figure 5-1
Operator Control Panel

5.1.1 Function/Status Display

The function/status display, located at the upper left of the OCP, shows one line of up to 40 alphanumeric characters. It communicates information directly to the operator. This information may be data, messages, or requests for operator response. It also echoes data and responses typed by the operator.

5.1.2 Function Entry Keypad

The function entry keypad, located at the lower left of the OCP, has 16 numeric keys and 16 function keys. These keys are used to initiate display functions, enter data, respond to questions, or initiate system commands.

Numeric Keys

The numeric keys (0 through F) are used to enter decimal or hexadecimal data. When used in conjunction with one of the function keys, the numeric key specifies which of several subfunctions is to be performed.

Function Keys

The function keys are used to enter specific commands. There are three types of function keys:

- o Unit state request keys
- o Master function keys
- o Special response keys

Unit State Request Keys. The unit state request keys are CACHE, WRITE THRU, BYPASS, READ ONLY, and DOWN. Pressing one of these keys followed by a number (0 through 15) or followed by the ALL key initiates a command requesting the system to change the present state of one or all drives to the state specified. The numbers 0 through 15 represent one of sixteen possible disk drives. See section 5.2.8 for a description of the unit state r keys.

CACHE	This key has no function in the 7100-30.
WRITE THRU	This key has no function in the 7100-30.
BYPASS	All operations are directed to the drive.
READ ONLY	Write operations are not allowed.
DOWN	No operations are allowed.

Master Function Keys. The master function keys are DISP, LOAD, PROGM, and ILD.

DISP/LOAD Pressing the DISP key or the LOAD key followed by a numeric key specifies a certain register, data, status, or message to be displayed or loaded. The abbreviated word above each numeric key identifies the subfunctions for DISP and LOAD master function keys only.

Below is a list of keys associated with the corresponding DISP and LOAD functions. See section 5.2 (Operating Functions) for a detailed description of the display functions which may be performed by an operator.

Key/Code	DISP Function	LOAD Function
0/TOD	Time of day	Time of day
1/BUT	Backup time	Backup time
2/INT	Interval time	Interval time
3/DSW	Data switches	Data switches
4/TOG	Toggle register	Toggle register
5/PB	Push button register	Push button register
6/PRS	Present unit state	not applicable
7/REQ	Requested unit state	not applicable
8/PASS	Password/clearance status	Password/clearance status
9/EVC	Event counter	Clear event counter
A/BRK	Break point address	Break point address
B/MODE	Operating mode (for ILDs)	Operating mode (for ILDs)
C/PGM	Program display	Clear message display
D/MSG	System message	Clear message display

PROGM The PROGM key, followed by the number 1, specifies that the initialize controller program be performed. See section 5.2 for a detailed description of this function.

ILD The ILD key, followed by a number, specifies an inline diagnostic (ILD) or operator function to be performed. These include verifying the drives, assigning alternate tracks, diagnosing drive and system problems, and performing special maintenance programs.

Two ILD routines may be run simultaneously, one on each controller. All ILD routines may be run while the system is online, but ILD processing is given a low priority so that it interferes minimally with normal system operations.

For this reason, when an ILD routine is started, the message "ILD PENDING" may appear on the display. This means that the controller is busy, and will start the ILD when time is available, usually within a few seconds. An ILD running on a drive takes that drive offline. It is therefore recommended that ILDs not be performed for an online drive without full intent and knowledge of the resulting effect. ILD routines which can be performed by an operator are discussed in section 5.2.

Below is a list of keys associated with the ILD function which may be performed by an engineer:

Key	ILD Function
0	ILD halt
1	Format disk drive
2	Verify disk drive
3	Verify a track
4	Assign alternate tracks
5	Perform oscillating seek test
6	Perform random seek test
7	Perform sequential seek test
8	Clear disk ECC display

Special Response Keys. The proper use of each of these six keys is explained below.

ALL — Press ALL to respond to a question that asks for a drive number. Answering ALL means all of the drives are to be acted upon, not just one.

DEL — Press DEL to delete the last numeric key entered so that it can be replaced with a new entry.

ENTER — Press ENTER when the numeric data entered does not equal the default parameters. Any data that was not specified is set to zero.

YES/NO — Press YES or NO to respond to yes/no questions.

CLEAR — Press CLEAR if you decide to clear the data entered at the OCP. (Pressing CLEAR only works if you press it prior to pressing the ENTER key.) The current operating routine or function terminates and the panel reverts to the last used display function. The CLEAR key does not affect any current operating system command or ILD; it only terminates an ILD during the time when you are entering the parameters.

5.1.3 Operations/Maintenance Data Display

The operations/maintenance data display, located at the upper right of the OCP, consists of 36 light-emitting diodes (LEDs). The octal scale above the display and the hex scale below the display help you interpret the data displayed on the LEDs. This display is used primarily by customer engineers for diagnostic purposes.

5.1.4 DISPLAY/SELECT Thumbwheel Switches

The DISPLAY/SELECT thumbwheel switches, located at the upper right of the OCP, are used in conjunction with the operations/maintenance data display. The thumbwheel switch setting selected determines the data which is displayed at the operations/maintenance data display. This display is used for diagnostic purposes.

The thumbwheel settings are shown below:

000 to 3FF	MDBP memory data, using a single 36-bit word format.
400 to 555	XMC scratchpad memory data, using three 12-bit words as a format.
E00 to EFF	XMC microcode address.

The display generated by each thumbwheel setting is explained in section 8.

5.1.5 Host Interface Display

This display is not functional in the 7100-30.

5.1.6 SPI Select Thumbwheel Switch

This switch is not functional in the 7100-30.

5.1.7 DISP Channel Select Switch

The DISP channel select switch, located at the lower right of the OCP, determines which controller (CU A or CU B) has its data displayed at, and controlled by, the OCP. All statuses, messages, and commands are from the specified controller, except for ILD error messages from the other controller and OCP-originated functions such as time of day.

5.1.8 ENABLE Switch

The ENABLE switch, located at the lower right of the OCP, disconnects one of the two controllers for diagnostic purposes. Setting the switch to A ONLY enables only the A controller to the host; setting it to B ONLY enables only the B controller. Setting it to BOTH enables both controllers. When the system is online, this switch should normally be set to BOTH.

5.1.9 RESET Button

The function of the RESET button, located at the lower right of the OCP, depends on the value in the toggle register (see section 5.2.6). The RESET button will abort the operation of a controller and reinitialize the system; it may clear all interrupts, de-select the disk drives, clear disk drive faults, or clear cache memory. The button affects only the controller selected at the DISP channel select switch.

CAUTION: The RESET button should be used with caution, since pressing it indiscriminately may cause loss of data.

The PROGM 4 key increases the extent of the initialization caused by pushing the RESET button. It does this by causing the reset to initialize the buffer and the display memory of the channel specified by the channel DISPLAY/SELECT switch.

5.2 Operating Functions

This section provides instructions explaining how to perform specific operating functions. The level of clearance assigned to a function determines who may access that particular function. The type of clearance level required for each function is indicated within the function descriptions. All functions can be accessed when in engineering level clearance. This section primarily explains functions which are engineering level functions.

5.2.1 Levels of Clearance

There are three clearance levels: monitoring, operator, and engineering. Each clearance level has restrictions limiting the information which can be accessed, thus preventing unauthorized personnel from altering system functions or commands.

Monitoring Level Clearance

Key/Code: DISP 8(PASS)

Monitoring level clearance allows functions which do not require operator or engineering intervention; it allows display functions only.

Operator Level Clearance

Key/Code: LOAD 8(PASS)

Operator level clearance enables an operator to enter certain system commands.

Engineering Level Clearance

Key/Code: LOAD 8(PASS)

Engineering level clearance allows additional maintenance and diagnostic routines needed only by field service representative. The following procedure describes how to obtain engineering level clearance.

1. At the OCP keypad, press **LOAD 8.**
2. xxxxxxxx **LEVEL CLEARANCE CANCELLED** and **MONITORING LEVEL CLEARANCE** are consecutively displayed at the OCP. Note that "xxxxxxxx" denotes monitoring, operator or engineering level clearance.
3. At the OCP keypad, press **LOAD 8** again.
4. **ENTER PASSWORD** appears at the OCP display.
5. Key in **xCExCE**, where "x" represents any digit from 0 through F.
6. **ENGINEERING LEVEL CLEARANCE GRANTED** appears at the OCP display. After **ENGINEERING LEVEL CLEARANCE** is displayed the system is ready to accept engineering level commands.

5.2.2 Time of Day

Key/Code: DISP/LOAD 0(TOD)

Clearance: Operator

This is the system's day clock. When the system is powered on, the time-of-day register should be loaded with the correct time. All system times are on a 24-hour clock, so 2 p.m. is 14:00:00. The system clock must be set each time the system is powered on, since the time of day is lost when power is lost.

5.2.3 Backup Time

Key/Code: DISP/LOAD 1(BUT)

Clearance: Operator

This function does not apply to the 7100-30.

5.2.4 Interval Time

Key/Code: DISP/LOAD 2(INT)

Clearance: Operator

This function does not apply to the 7100-30.

5.2.5 Data Switch

Key/Code: DISP/LOAD 3(DSW)

Clearance: Engineering

The data switches are used to make sure the ECC circuitry is correct. This register holds nine hex digits (36-bits) which come from a register in the OCP. The value of the data switch is written to the data field when the disk is formatted (ILD 1).

The following procedure describes how to set the value of the data switches.

1. At the OCP keypad, press **LOAD 3.**
2. **LOAD DATA SWITCHES:** is displayed at the OCP.
3. Enter a number up to nine digits. Note if fewer than nine digits are keyed in, press **ENTER;** the system automatically precedes the number with zeros.
4. **DATA SWITCH: nnnnnnnnn** is displayed at the OCP. Note "nnnnnnnnn" indicates the value of the nine data switches. Each of the nine switches contains four bits representing the 36-bit word.

5.2.6 Toggle

Key/Code: DISP/LOAD 4(TOG)

Clearance: Monitoring (for display); Engineering (for load)

This register holds two hex digits (eight bits). It is read by the XMC board to control the depth of initialization done when the RESET button is pushed. There are five settings, with settings 00 through 17 having a cumulative effect. For example, setting 07 has the effect of setting 00, 01, as well as 07.

Toggle (hex)	Action taken when RESET is pushed
00	Resets XMC, clears interrupts, de-selects drives and clears faults.
01	Same as 00, plus clears error/usage log and ECC history.
07	Same as 01, plus initializes control unit memory and executes controller diagnostic tests; builds operating tables in SMB memory and determines drive types.
17	Same as 07.
83	Resets system when drives have not been previously formatted or when the drive header cannot be read.

Any other setting of the toggle is treated as 00.

The following procedure describes how to set the value of the toggle switch.

1. At the OCP keypad, press **LOAD 4.**
2. **LOAD TOGGLE:** appears at the OCP display.
3. Key in a valid toggle number, as described above.
4. **TOGGLE REGISTER:nn** appears at the OCP display. Note "nn" represents the selected toggle register.

5.2.7 Push Button

Key/Code: DISP/LOAD 5(PB)

Clearance: Engineering

The push button holds two hex digits that are read by the XMC to initiate ILD routines. The following procedure describes how to initiate an ILD routine using the push button key.

1. At the OCP keypad, press **LOAD 5.**
2. **LOAD PUSH BUTTON** appears at the OCP display.
3. Key in an ILD number (**1, 2, 3, 4, 5, 6, 7,** or **8**) and press **ENTER.**
4. The ILD routine selected is initiated. See the appropriate ILD routine description for additional instructions.
5. Press **CLEAR** to terminate this procedure.

5.2.8 Present and Requested Drive States

Key/Code: DISP 6(PRS); DISP 7(REQ)

Clearance: These are display functions only; they have no meaning for LOAD.

The present drive state and requested drive state functions have the same format. The present drive state displays the states of the drives as they are when you are making the request. The requested drive state displays the states of the drives according to what you have requested they be changed to.

Each of the first 32 spaces of the function/status display contains a letter code; each letter code indicates the state of one disk drive. The space farthest to the left displays the state of drive unit 0 (the unit numbers are printed underneath the function/status display on the panel). The three possible letter codes follow.

Code	Unit State
B	Bypass
R	Read only
D	Down

A blank in the request display indicates all requests for that unit have been processed, so the requested state is cleared.

Bypass - All operations are directed to the drive.
Key: BYPASS
Clearance: Operator

Read Only - Write operations are not allowed.
Key: READ ONLY
Clearance: Operator

Down - No operations are allowed.
Key: DOWN
Clearance: Operator

5.2.9 Event Counter

Key/Code: DISP/LOAD 9(EVC)

Clearance: Monitoring

The event counter holds the running total of times the break point address or an externally attached hardware signal was triggered. Loading the event counter sets the count to zero.

5.2.10 Breakpoint Address

Key/Code: DISP/LOAD A(BRK)

Clearance: Monitoring

For monitoring purposes, any of the system's instruction code addresses can be set as the breakpoint address. Whenever this address is triggered, the event counter is incremented by one. Used for troubleshooting, this function traces the system code operation to make sure it is going through certain parts of the microprogram. The following procedure describes how to load the breakpoint address.

1. At the OCP keypad, press **LOAD A.**
2. **ENTER BREAK POINT ADDRESS** appears at the OCP display.
3. Key in a four-digit number representing a valid microprogram address.
4. **ADDRESS xxxx TRIGGERED yyyy TIMES** appears at the OCP display. Note "xxxx" represent the microprogram address selected and "yyyy" represents the number of times the microprogram was triggered.

5.2.11 Operating Mode Register

Key/Code: DISP/LOAD B(MODE)

Clearance: Monitoring (for display); Operator (for load)

The operating mode register is used to modify the way ILDs are run; it affects ILDs 1, 2, 5, 6, and 7. For example, an ILD may terminate on completion, run continuously until an error is encountered, or run until it is halted by the operator. The operating mode selected determines which of these will occur. An operating mode can be selected at any time except while parameters are being entered.

Sections 5.2.24 and 5.2.25 as well as 5.2.28 through 5.2.30 explain how to perform ILDs using modes.

5.2.12 Program Display

Key/Code: DISP C(PGM)

Clearance: This is a display function only; it cannot be loaded.

The program display is not functional in the 7100-30.

5.2.13 System Message

Key/Code: DISP D(MSG)

Clearance: Monitoring

This register holds a system-generated message conveyed to the operator via the function/status display. The OCP automatically displays this register whenever a new message is generated. Loading this register causes the message to be erased.

5.2.14 Introduction Routine

Key/Code: PROGM 0

Clearance: Monitoring

This is an advertising and introduction program. It displays a series of messages, each for two seconds, then the program repeats. To exit this program, press **CLEAR**.

5.2.15 Initialize Channel

Key/Code: DISP 4

Clearance: Operator

When used in conjunction with the RESET button, this reset initializes one of the channels. The channel initialized is the one selected at the DISP channel select switch at the time the RESET button is pressed.

5.2.16 Initialize Controller

Key/Code: PROGM 4

Clearance: Operator

This program clears the memory of the controller.

5.2.17 Initialize OCP

Key/Code: PROGM 8

Clearance: Engineering

This operation is equivalent to powering off the system and then powering it on again. The following procedure describes how to initialize the OCP.

1. At the OCP keypad, press **PROGM 8.**
2. **INITIALIZE OCP, ARE YOU SURE?** appears at the OCP display.
3. Press **YES** to cause the OCP software to jump directly to its power-on initialization routine. This is equivalent to powering off and then powering on the OCP.
4. The system automatically places all drives in bypass mode. **PROGRAM DISPLAY: 00000000** is displayed at the OCP.
5. Press **NO** to abort the program. The display is cleared.

5.2.18 Initialize RAM Buffer

Key/Code: PROGM 9

Clearance: Engineering

The RAM buffer contains all the drive states (they are set to bypass mode), the XMC/OCP communication area, and the interchannel communication status. The following procedure describes how to initialize the RAM buffer portion of the power-on initialization routine.

1. At the OCP keypad, press **PROGM 9.**
2. **INITIALIZE RAM BUFFER, ARE YOU SURE?** appears at the OCP display.
3. Press **YES** to cause the OCP software to execute the initialize RAM buffer section of the power-on initialization routine.
4. The system automatically places all drives in bypass mode. **BBBBBBBBBBBBBBBBBBB PRSNT** is displayed at the OCP.
5. Press **NO** to abort the program. The display is cleared.

5.2.19 8085 Editor Mode

Key/Code: PROGM A

Clearance: Engineering

This program is used to examine and edit the OCP 8085 software. When the program is initiated, the display reads:

ADDR aaaa = dd

Where **aaaa** is an address of the 8085 software and **dd** is the content of that address.

The keypad is used to enter the commands to the editor:

Key	Command
ENTER	Increment to the next address
DEL	Decrement to the last address
DISP	Get a new address to display
LOAD	Change the data of the displayed address
PROGM	Jump the OCP software to the displayed address
CLEAR	Exit the editor

Addresses 0000 to 1FFF are the 8085 ROM and cannot be reloaded.
Addresses 8000 to 83FF are the 8085 RAM and may be reloaded.

5.2.20 Repeat XMC Reset

Key/Code: PROGM C

Clearance: Engineering

This program is used primarily as an in-house debugging aid. Running this program causes the OCP to re-issue an XMC reset every 100 milliseconds. The following procedure describes how to repeat the XMC reset.

1. At the OCP keypad, press **PROGM C.**
2. **RESETTING XMC EVERY 100 MS** appears at the OCP display.
3. Press **CLEAR** to cancel the program.

5.2.21 Slow Run Mode

Key/Code: PROGM E

Clearance: Engineering

This program enables the XMC instructions to be run very slowly for diagnostic purposes.

NOTE: *In a dual channel configuration, both channels are affected by this program.*

1. At the OCP keypad, press **PROGM E.**
2. **ENTER DELAY IN TICKS** appears at the OCP display. A tick is one tenth of a second.
3. Enter a number from 1 to 255 (.1 to 25.5 seconds). One XMC instruction is executed per delay time.
4. **HIT CLEAR TO RESUME NORMAL MODE** is displayed at the OCP while the system is in slow run mode.
5. Press **CLEAR** to cancel the program.

5.2.22 Step Run Mode

Key/Code: PROGM F

Clearance: Engineering

This program allows you to execute XMC instructions one at a time or halt the XMC completely. The following procedure describes how to execute one XMC instruction at a time.

NOTE: *In a dual channel configuration, both channels are affected by this program.*

1. At the OCP keypad, press **PROGM F.**
2. **SINGLE STEP MODE** is displayed at the OCP.
3. **STEP ?** appears at the OCP display indicating the XMC is halted.
4. Press **YES** each time the next instruction is to be executed.
5. Press **NO** to abort the program. The display is cleared.

5.2.23 Halt ILD Routine

Key/Code: ILD 0

Clearance: Monitoring

This procedure aborts an ILD routine while it is running.

5.2.24 Format and Verify a Disk Drive

Key/Code: ILD 1

Clearance: Engineering

ILD 1 formats disk drives and in the formatting process writes header information to each record. This information includes the logical drive i.d. number. ILD 1 automatically starts ILD 2, regardless of the mode selected. ILD 2 then verifies header information, data, and ECC. Since headers include drive i.d. numbers, the verification process ensures that data is being read or written from the correct drive.

When ILD 1 is running, mode 0, 1, 2, or 4 can be used. See table 5-1 for a description of mode functions.

Conditions: The operator may format and/or verify any selected range of cylinders and heads. Parameters for that function (drive unit, starting and ending cylinder, and starting and ending head) must be specified by the operator. Unless mode 4 or 6 is set when ILD 1 is initiated, ILD 2 then performs a data verification upon successful completion of the ILD 1 formatting routine.

The mode may be set before an ILD key is pressed, or after the formatting procedure has actually begun. It may not be set while the ILD routine is prompting for drive number, cylinder number, etc. The example below sets the mode while ILD 1 is formatting a drive.

Default Parameters:

Drive unit = last one used in the last executed ILD function.

Cylinders and heads = last used range for the default drive unit, or the full range if a new drive is specified.

When the format function is initiated, the system displays the default parameters it has, then asks if the operator wants to use them.

If the operator responds with a NO, or the system has no default parameters, the system requests the operator to enter new parameters using the keypad.

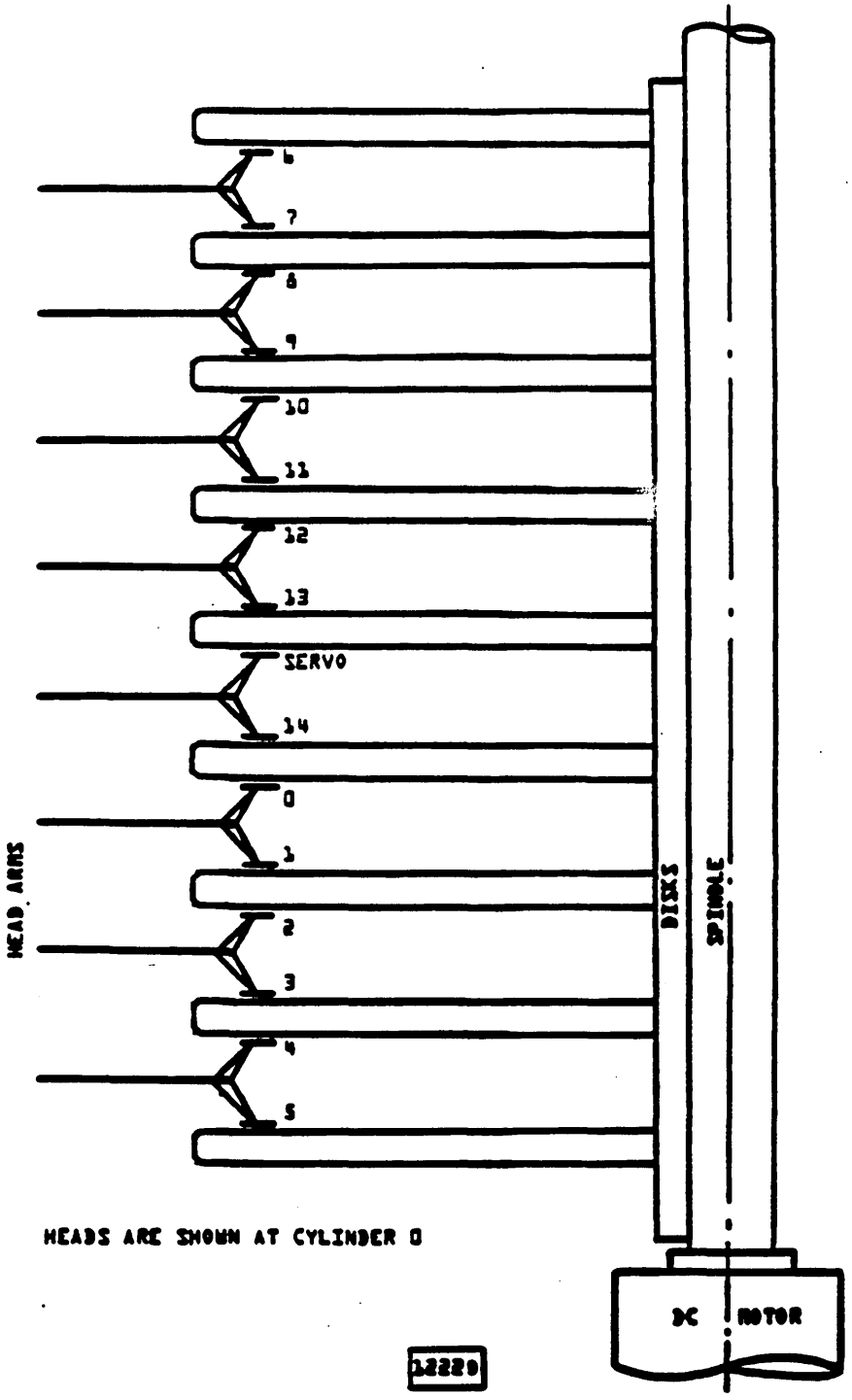

Figure 5-2
Disk Head/Cylinder Organization

Run Format and Verify:

The following procedure describes how to run the format and verify routine.

1. At the OCP keypad, load the data switch register (see section 5.2.5) with nine hexadecimal digits (LOAD 3). These digits constitute a pattern that is written to the drive when it is formatted with ILD 1. If no digits are specified, the data switch register is loaded with zeros by default. We recommend formatting the drives with a worst-case data pattern to assist in detecting marginal drive surfaces while verifying. To accomplish this, load the data switches with the value 333086661.
2. At the OCP keypad, press **ILD 1.**
3. **ILD 1, DR=nn OK?** appears at the OCP display. Note "nn" represents the drive number of the last ILD routine.
4. If the drive number is correct, press **YES** and go to step 8.
5. If the drive number is incorrect, press **NO.**
6. **ENTER DRIVE NO.** appears at the OCP display.
7. Key in a drive number (**0-15**) and press **ENTER.**
8. **START CYL=ccc,END CYL=ccc OK?** appears at the OCP display. Note "ccc" represents the cylinder number. (Possible cylinder numbers are 0-1633.)
9. If the starting and ending cylinders are correct, press **YES** and go to step 15.
10. If the starting and ending cylinders are incorrect, press **NO.**
11. **ENTER STARTING CYL NO.** is displayed at the OCP.
12. Key in the desired starting cylinder number and press **ENTER,** if necessary.
13. **ENTER ENDING CYL NO.** is displayed at the OCP.
14. Key in the desired ending cylinder number and press **ENTER,** if necessary. If the entire drive is being formatted, including alternate tracks, steps 15 through 21 are skipped.
15. **START HEAD=hh, END HEAD=hh OK?** appears at the OCP display. Note that "hh" represents the head number. (Possible head numbers are 0-14.)
16. If the starting and ending head numbers are correct, press **YES** and go to step 32.
17. If the starting and ending head numbers are incorrect press **NO.**
18. **ENTER STARTING HEAD NO.** appears at the OCP display.
19. Key in the desired starting head number and press **ENTER,** if necessary.
20. **ENTER ENDING HEAD NO.** appears at the OCP display.
21. Key in the desired ending head number and press **ENTER,** if necessary.
22. **DO YOU WANT TO FORMAT DRIVE nn?** appears at the OCP display.

23. Press **YES.**

24. **FORMATTING DR.nn,CYL.ccc** is displayed at the OCP. The system formats the drive within the selected parameters. the cylinder (ccc) increments continuously until the drive has finished formatting. At this point, you may specify a mode. To do so, go to step 25; if no mode is to be specified, go to step 28.

25. Press **LOAD B** at the keypad.

26. **LOAD MODE:** appears at the OCP display.

27. Key in **0** to enter mode 0. (Mode 0 is the default mode for the ILDs.)

    To run ILD 1 with mode 2, use the above procedures, but key in **2** rather than 0 in step 27.

    To run ILD 1 with mode 4, use the above procedures, but key in **4** rather than 0 in step 27. Mode 4 will verify ECC, but not data, so there will be no data error message on the OCP display in step 29.

28. After the drive has been formatted, the system automatically begins to verify the drive. **VERIFYING DR.nn,CYLccc** is displayed to indicate that the verify procedure is in progress. As with the formatting procedure, the cylinder (ccc) increments continuously until the drive has finished verifying.

29. **VERIFY COMPLETE** appears at the OCP display if the ILD completes without encountering an error.

    or

    FORMAT ERROR DR.XX,CYL.XXXX, HEAD X appears at the OCP display if an error occurs during the formatting process

    or

    VERIFY ERROR DR.XX,CYL.XXXX, HEAD X appears at the OCP display if an error occurs during the verification process

    or

    DATA ERR:GOOD = XXXXXXXXX, BAD = XXXXXXXXX appears at the OCP display if a data error occurs.

30. If no error was encountered, press **ILD 0** to halt the ILD. If an error was encountered, press any key other than 1 or 2 to halt the ILD.

    or

    Press **1** to retry the error a predetermined number of times.

    or

    Press **2** to continuously retry the error.

NOTE: *If running ILD 1 after replacing disk drive, use procedure in section 10.14.*

Table 5-1
Mode Value Functions

Mode	ILD No.	Function
0,1	1	ILD 1 formats drives, then automatically starts ILD 2. ILD 2 terminates after it has been completed.
0	2	ILD terminates after it has been completed.
1	2	ILD runs continuously until halted by the operator (ILD 0) or until an error is detected that cannot be corrected through retry.
0	5,6,7	Seek operations are performed without verification of header information.
1	5,6,7	Header information is read from head 0 after each seek operation to confirm that the head is properly positioned.
2	1	ILD 1 formats drives, then automatically starts ILD 2. The verify operation in ILD 2 stops when an error is detected or following normal completion. Error retry is not performed.
2	2	The verify operation stops when an error is detected or following normal completion. Error retry is not performed.
3	2	ILD runs continuously until halted by the operator or until an error is detected. Error retry is not performed.
4	1	ILD 1 formats drives, then automatically starts ILD 2. The data verification phase of ILD 2 is disabled. Only ECC is verified.
6	1	ILD 1 formats drives, then automatically starts ILD 2. Mode 2 and mode 4 functions are combined.

5.2.25 Verify a Drive

Key/Code: ILD 2

Clearance: Operator

When ILD 2 is automatically run by starting ILD 1, ILD 2 verifies header information, data, and ECC. When ILD 2 is started alone, it verifies header information and data ECC, but not data. When ILD 2 is running, mode 0, 1, 2, or 3 can be used. See table 5-1 for an explanation of mode functions. The following procedures demonstrate how to run ILD 2 in mode 0:

1. Perform ILD 2 to verify the header and data ECC.
2. Press **LOAD B** at the keypad.
3. **LOAD MODE:** appears at the OCP display.
4. Key in **0** to run one cycle of ILD 2.
5. **VERIFY COMPLETE** appears at the OCP display if the ILD completes without encountering an error.

   or

   VERIFY ERROR DR. XX, CYL. XXXX, HEAD X appears at the OCP display if an error occurs during the verification process.
6. If no error was encountered, press **ILD 0** to halt the ILD; if an error was encountered, press any key other than 1 or 2 to halt the ILD.

   or

   Press **1** to retry the error a predetermined number of times.

   or

   Press **2** to continuously retry the error.

To run ILD 2 in mode 1, modify the above procedures by keying in **1** rather than **0** in step 4. This will enable ILD 2 to run continuously. If ILD 2 does not encounter an error, it can be terminated by entering **ILD 0**.

To run ILD 2 in mode 2, modify the above procedures by keying in **2** rather than **0** in step 4. This will enable ILD 2 to run one time and to stop on all data ECC errors.

To run ILD 2 in mode 3, modify the above procedures by keying in **3** rather than **0** in step 4. This will enable ILD 2 to run continuously. If the ILD does not encounter an error, it can be halted by entering **ILD 0**.

When ILD 2 is running in mode 2 or 3, it halts when it encounters an error and does not retry it automatically. However, if you press **2** when an error occurs, the ILD will no longer halt as soon as it encounters an error. Therefore, we advise you to press **1** rather than **2** when an error occurs in order to retry the error.

5.2.26 Verify One Track

Key/Code: ILD 3

Clearance: Operator

This procedure verifies a single cylinder and head repeatedly.

Conditions: The procedure for entering the drive number, cylinder and head are similar to the verify routine, except that the starting cylinder and head are considered the only cylinder and head.

Perform the following procedure to verify a single track.

1. At the OCP keypad, press **ILD 3.**
2. **ENTER DRIVE NUMBER** appears at the OCP display.
3. Key in a valid drive number.
4. **ENTER STARTING CYL NO.** appears at the OCP display.
5. Key in a valid starting cylinder number.
6. **ENTER STARTING HEAD NO.** appears at the OCP display.
7. Key in a valid starting head number.
8. **VERIFYING DR.nn,CYL.ccc,HEAD.hh** is displayed at the OCP. If the track being verified is defective and has been assigned an alternate track, it will only make one pass and then display **VERIFY COMPLETE ALT. TRK.=cccc h** where cccc h is the alternate cylinder and head assigned for this track. If the track is not defective, it will continuously verify until an error occurs or the routine is halted with ILD 0.

5.2.27 Assigning Alternate Tracks

Key/Code: ILD 4

Clearance: Engineering

ILD 4 automatically assigns an alternate track for a specified defective track. It also flags defective alternate tracks. The ILD prompts for the drive, cylinder, and head number to define the defective track. (This information is obtained from the disk manufacturer's flaw map program.) The ILD formats the alternate tracks, writing header information (including the logical drive number) to each record.

ILD 4 may be used online without downing the disk drive or the system, but ILD 4 will take the drive offline for the brief duration of this function. Data on the cylinder/head should be removed or backed up.

1. At the OCP keypad, load the data switch register (see 5.2.5) with nine hexadecimal digits (LOAD 3). These digits constitute a pattern that is written to the defective and alternate tracks of the drive when ILD 4 is run. We recommend that you format the drives with a worst-case data pattern to assist in detecting marginal disk drive surfaces. To accomplish this, load the data switches with the value 333086661. If no digits are specified, the data switch register is loaded with zeros by default.
2. At the OCP keypad, press **ILD 4.**

3. **ILD 4, DR=nn OK?** ("nn" refers to the drive number.)
4. If the drive number is correct, press **YES** and go to step 8.
5. If the drive number is incorrect, press **NO.**
6. **ENTER DRIVE NO.** appears at the OCP display.
7. Key in a drive number (**0-15**) and press **ENTER,** if necessary.
8. **ENTER DEF. CYL. NO.** appears at the OCP display.
9. Key in the cylinder number of the defective track and press **ENTER,** if necessary.
10. **ENTER DEF. HEAD NO.** appears at the OCP display.
11. Key in the head number of the defective track and press **ENTER,** if necessary.
12. **DO YOU WANT TO FORMAT DR. nn?** appears at the OCP display (where "nn" is the drive number entered in step 7).
13. If you believe you entered the drive, cylinder, and head numbers correctly, press **YES** and go to step 16.
14. If you believe you entered the drive, cylinder, or head number incorrectly, press **NO.**
15. **ILD TERMINATED** appears at the OCP display. To assign an alternate track, start with step 1.
16. If a defective track was identified in the steps above, **VERIFY COMPLETE - ALT. TRK. =** ccccch appears at the OCP display, where "cccc" identifies the alternate cylinder that has been assigned and "h" represents the head number of the alternate track.

    If a defective alternate track was identified in the steps above, **DEFECTIVE ALTERNATE FORMAT COMPLETE** appears at the OCP display.

5.2.28 Oscillating Seek

Key/Code: ILD 5

Clearance: Operator

The oscillating seek test seeks back and forth between two selected tracks; it checks the performance of a drive. The following procedure describes how to run the oscillating seek routine.

NOTE: *With the seek routines, if mode 0 is enabled, a physical seek is done without verifying the header information. If mode 1 is enabled, after a seek is completed to a cylinder, the header information from head 0 is read to verify that the correct cylinder has been reached.*

1. At the OCP keypad, press **ILD 5.**
2. **ILD 5,DR=nn OK?** Note "nn" refers to the drive number.
3. If the drive number is correct, press **YES** and go to step 7.
4. If the drive number is incorrect, press **NO.**
5. **ENTER DRIVE NO.** appears at the OCP display.
6. Key in a drive number (**0-15**) and press **ENTER,** if necessary.
7. **START CYL=ccc,END CYL=ccc OK?** is displayed at the OCP. Note "ccc" represents the cylinder number.
8. If the starting and ending cylinders are correct, press **YES** and go to step 14.
9. If the starting and ending cylinders are incorrect, press **NO.**
10. **ENTER STARTING CYL NO.** appears at the OCP display.
11. Key in the starting cylinder number and press **ENTER,** if necessary.
12. **ENTER ENDING CYL NO.** appears at the OCP display.
13. Key in the ending cylinder number and press **ENTER,** if necessary.
14. **OSCILLATING SEEK, DR.=n OK?** is displayed at the OCP. Press **YES** to start the ILD. Press NO to terminate the ILD at this point.
15. **OSCILLATING SEEK RUNNING, DR nn** is displayed at the OCP. This indicates the system is performing the oscillating seek operation. This seek tests keeps repeating until an error is detected or the ILD halt (ILD 0) routine is run. To stop this procedure press **ILD 0.**
16. Press **LOAD B** at the keypad.
17. **LOAD MODE:** appears at the OCP display.
18. Key in **0** to seek the drives without verifying headers, or key in **1** to enable the ILD to verify the header in addition to seeking the drive.

19. Press **ILD 0** to halt the seek routine.

    or

    If the drive has seeked the wrong cylinder, the following message will appear at the OCP display: **SEEK ERROR, DR. XX, CYL = XXXX, BAD = XXXX.** (CYL refers to the proper location and BAD refers to the actual location.)

    or

    With all other errors, the following message will appear at the OCP display: **SEEK ERROR, DR. XX, CYL XXXX**

20. Press **ILD 0** to halt the routine.

5.2.29 Random Seek

Key/Code: ILD 6

Clearance: Operator

The random seek test seeks from one randomly selected track to another. The following procedure describes how to run the random seek routine.

NOTE: *With the seek routines, if mode 0 is enabled, a physical seek is done without verifying the header information. If mode 1 is enabled, after a seek is completed to a cylinder, the header information from head 0 is read to verify that the correct cylinder has been reached. See 5.2.28 on running ILD 5 for an example of how to set modes with ILD 6.*

1. At the OCP keypad, press **ILD 6.**
2. **ILD 6,DR=nn OK?** appears at the OCP display. Note "nn" refers to the drive number.
3. If the drive number is correct, press **YES** and go to step 7.
4. If the drive number is incorrect, press **NO.**
5. **ENTER DRIVE NO.** is displayed at the OCP.
6. Key in a drive number **(0-15)** and press **ENTER,** if necessary.
7. **RANDOM SEEK, DR.=n OK?** appears at the OCP display. Press **YES** to start the ILD. Press NO to terminate at this time.
8. **RANDOM SEEK RUNNING,DR=nn** is displayed at the OCP. This indicates the system is performing the random seek operation. This seek test keeps repeating until an error is detected or the ILD Halt (ILD 0) routine is run. To stop this test press **ILD 0.**

5.2.30 Sequential Seek

Key/Code: ILD 7

Clearance: Operator

The sequential seek test seeks sequentially to all tracks between a starting track and an ending track, and then seeks sequentially back to the starting track.

NOTE: *With the seek routines, if mode 0 is enabled, a physical seek is done without verifying the header information. If mode 1 is enabled, after a seek is completed to a cylinder, the header information from head 0 is read to verify that the correct cylinder has been reached.*

See section 5.2.28 on running ILD 5 for an example of the way modes are used with ILD 7.

1. At the OCP keypad, press **ILD 7.**
2. **ILD 7,DR=nn OK?** Note "nn" refers to the drive number.
3. If the drive number is correct, press **YES** and go to step 7.
4. If the drive number is incorrect, press **NO.**
5. **ENTER DRIVE NO.** appears at the OCP display.
6. Key in a drive number (**0-15**) and press **ENTER,** if necessary.
7. **START CYL=ccc,END CYL=ccc OK?** is displayed at the OCP. Note "ccc" represents the cylinder number.
8. If the starting and ending cylinders are correct, press **YES** and go to step 14.
9. If the starting and ending cylinders are incorrect, press **NO.**
10. **ENTER STARTING CYL NO.** appears at the OCP display.
11. Key in the starting cylinder number and press **ENTER,** if necessary.
12. **ENTER ENDING CYL NO.** appears at the OCP display.
13. Key in the ending cylinder number and press **ENTER,** if necessary.
14. **SEQUENTIAL SEEK DR=nn OK?** is displayed at the OCP.
15. Press **YES** to run the seek.
16. **SEQUENTIAL SEEK RUNNING, DR nn** is displayed at the OCP. This indicates the system is performing the sequential seek operation.
17. This seek test keeps repeating until an error is detected or the ILD Halt routine is run. To stop this procedure press **ILD 0.**

5.2.31 Clear Disk Drive ECC Display

Key/Code: ILD 8

Clearance: Engineering

The log of the ECC errors for the disk drives may be cleared by following the procedure described below.

1. At the OCP keypad, press **ILD 8.**
2. **ILD 8 DISK ECC DISPLAY CLEAR, OK ?** appears at the OCP display.
3. Press **NO** to abort the routine.
4. Press **YES** to clear all previous disk drive ECC logging.
5. **DISK ECC DISPLAY CLEAR COMPLETE** is displayed at the OCP.

5.3 Error Messages Displayed at the OCP

Below is a list of error messages which may be displayed at the OCP. In most cases, these messages indicate a condition requiring the assistance of customer service.

OCP Messages Description/Response

**** INVALID KEY**

This message appears when an OCP key is pressed illegally. Then the message disappears and the OCP returns to the last valid display or to the current time.

*** BAD COMMAND nn**

This appears when the XMC sends an illegal command to the OCP. "nn" represents the code of the illegal command in 2 hexadecimal characters. The operator should make note of this code, then press **DISP MSG** to display the contents of the message buffer and write down what is displayed for customer service's use in analyzing this problem.

**** BAD MSG ****

This message is displayed when the XMC instructs the OCP to send an illegal message. (The operator should make note of the message for customer service's use in analyzing this problem; the message remains until it is overwritten by another message.)

Or, this message is displayed when the XMC attempts to store a message more than 40 characters long in the OCP message buffer. The message flashes on the display, then the first 40 characters in the OCP message buffer are displayed. (The operator should make note of the message for customer service's use in analyzing this problem; the message remains until the CLEAR key is pushed or until it is overwritten by another message.)

BAD ENTRY.RE-ENTER ILD AND NO.

These messages are displayed when an incorrect ILD number is keyed into the system (for example, ILD F). Press **ILD** and the desired number.

DRIVE NEEDS FORMATTING.ILD TERMINATED

The specified drive type cannot be identified; the operator should contact customer service.

DRIVE NOT READY

This message is displayed if there is an internal fault with the drive, if the drive is powered off, or if the drive's channel ENABLE switches are not depressed. If the drive is powered off, power it up to access the drive. If it is not powered off, verify that its channel enable switches are enabled. If they are, the operator should contact customer service.

VERIFY ERROR DR.nn,CYL.ccc,HEAD.hh

This indicates that an error occurred while performing the verify routine. The operator should contact customer service for assistance.

5.4 7100-30 Offline Diagnostics and Utilities

This section provides information about 7100-30 diagnostics and utilities. Offline diagnostics in the 7100-30 are resident in prom bank 0 of the Amperif 7155 emulation code. These routines can be started from the OCP by issuing an ILD on the Amperif controller. When an error is detected by offline diagnostics which were initiated at the OCP, an error code is returned to the OCP display and the OCP thumbwheel. (See section 5.4.3.)

Diagnostics are run under the following two conditions:

1. At start-up or after a reset. The following three tests are automatically run.

   - o HSP CPU register test
   - o HSP local memory test
   - o U-bus interface FIFO check

   If these tests are run successfully, then thumbwheel switch 4D0 = 81F100000. If they do not run successfully, then thumbwheel switch 4D0 = (error code). Except for a listing of the error codes (see section 5.4.3), these tests are not discussed in this manual.

2. When executed by function. These diagnostics stop on hard errors and there is no ability to continue. These diagnostics are described in this section.

NOTE: *Do not run diagnostics unless thumbwheel switch 4D0 = 81F100000 after a reset.*

5.4.1 Operating Procedures

CAUTION: The diagnostics and the utility that perform writes will destroy customer data. Therefore, be sure that customer data is protected before proceeding.

To run offline diagnostics to a device, a controller must be down. To run the diagnostics/utilities from the OCP, perform the following steps at the OCP keypad:

ENTER: ILD B

DISPLAY: TEST OK?

ENTER: YES (to continue)
NO (to run data restore ILD)

DISPLAY: TEST CODE =

ENTER: Amperif function (in hex) for the appropriate diagnostic/utility
or
FFF (to exit diagnostic mode)

5.4.2 Descriptions of Utility and Diagnostic Functions

This section describes the single utility and the four diagnostic functions which are available on the 7100-30. They are as follows:

- o Write Manufacture Data (utility)
- o Read Data (diagnostic)
- o Write and Read (short) (diagnostic)
- o Write and Read (long) (diagnostic)
- o Write and Read (worst case) (diagnostic)

Write Manufacture Data (utility)

CAUTION: Manufacture data is written prior to shipment and must be present prior to customer use. This data, however, is destroyed by any offline diagnostic which performs a write. Therefore, if you run an offline diagnostic which performs a write, make sure to run this utility afterward, before turning the system back over to the customer.

When this utility is complete, thumbwheel switch 4D0 = 771728.

AMPERIF FUNCTION (in hex) =

0100 1110 XXXX where XXXX is unit number 0-15, in hex (see tables 5-2 and 5-3)

Example: To run to unit 5

0100 1110 0101 = 4E5 (hex)

Read Data (diagnostic)

AMPERIF FUNCTION (in hex) =

0010 1110 XXXX where XXXX is unit number 0-15, in hex (see tables 5-2 and 5-3)

Example: To run to unit 5

0010 1110 0101 = 2E5 (hex)

This function will read the surface of the pack and then check the HP/A position and checksum. For this test to run without errors, the surface must have been written by a diagnostic routine or by customer data. This diagnostic will complete and stop by itself. (See the utility discussion above for an example of parameter entry.)

Write and Read (short) (diagnostic)

NOTE: ***This function is not normally used.***

AMPERIF FUNCTION (in hex) =

0011 1100 XXXX where XXXX is unit number 0-15, in hex (see tables 5-2 and 5-3)

Example: To run to unit 5

0011 1100 0101 = 3C5 (hex)

The surface will be written and read back and data compared. The writes and the reads to the Amperif U-bus will be a single record length, so no truncation will occur. Word lengths will be 116 (74 hex) in the command words. This diagnostic will run until an error occurs or until stopped by another function. (See the utility discussion above for an example of parameter entry.)

Write and Read (long) (diagnostic)

AMPERIF FUNCTION (in hex) =

0100 0000 XXXX where XXXX is unit number 0-15, in hex (see tables 5-2 and 5-3)

Example: To run to unit 5

0100 0000 0101 = 405 (hex)

This diagnostic is the same as Write and Read (short) except the word length issued to the U-bus will be 65,424 (FF90 hex) in the command word and truncation will occur after the first record. This diagnostic will run until an error occurs or until it is stopped by another function. (See the utility discussion above for an example of parameter entry.)

Write and Read (worst case) (diagnostic)

AMPERIF FUNCTION (in hex) =

0101 0000 XXXX where XXXX is unit number 0-15, in hex (see tables 5-2 and 5-3)

Example: To run to unit 5

0101 0000 0101 = 505 (hex)

This diagnostic is the worst case condition found during product development. There are five parts to this diagnostic:

1. The surface is written/read with a long write/read (65,424 for a command word count) and truncated after 500 records with a different data pattern for each record.
2. The surface is written/read with a truncation after 375 records and a different pattern is used.
3. The surface is written with the same pattern as before, but with a truncation after 125 records (read ahead).
4. A complete random mode of truncation length is written/read of the surface.
5. When the entire surface has been written and checked, a complete random write and read is entered which will run until errors occur or until it is stopped by another function. (See the utility discussion above for an example of parameter entry.)

Table 5-2
Device Addresses

Device Address	Unit Bits 0-3	X (Hex)
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Table 5-3
Utility/Diagnostic and Hex Function**

Utility/Diagnostic	Function (Hex)
Write Manufacture Data	4EX*
Read Data	2EX*
Write and Read (Short)	3CX*
Write and Read (Long)	40X*
Write and Read (Worst Case)	50X*

* where X is defined in table 5-2

5.4.3 Error Codes

The following error codes are common to all offline diagnostics/utilities. It is possible to have both upper and lower bit errors at the same time. To verify a valid error, rotate the thumbwheel switch (on the OCP) to 4D0. The right-hand 12 bits should be identical to the error code displayed.

When the diagnostics are initiated from the OCP, the error codes will be displayed on the OCP.

X	X	X	X	X	X	X	X	X	X	X	X
11	10	9	8	7	6	5	4	3	2	1	0

upper bit error lower 5-bit error

upper bit error codes:
In the chart below, if the bit shown is set, the explanation which follows describes the error.

bit set:	explanation:
5	The code is a start-up error.
6	The read data does not compare with the data written.
7	The HP/A detected an error.
8	A write error was detected.
9	A track or record error occurred.
10	A cylinder error occurred.
11	A checkword error occurred.

lower 5-bit error codes:

bits 43210	
00001	No device end before seek command issued
00010	U-bus parity error
00011	No status after a seek command
00100	Command reject status returned status action of 4
00101	Status action of F returned
00110	Issued command aborted
00111	Timeout data on U-bus
01000	Unexpected status present on entry to issue command routine
01001	Unexpected data present on U-bus interface card on entry to issue command routine
01010	Amperif control unit did not take command word
01011	Enable tags not set on entry to issue address word
01100	Amperif control unit did not take address word
01101	Amperif control unit presented status on entry to write routine
01110	HP/A timeout waiting for output data request from Amperif control unit
01111	HP/A timeout in the high-speed write because control unit stopped taking data
10000	HP/A timeout waiting for status after a write operation
10001	Amperif abnormal write termination (see status sent)
10010	Amperif status present on entry to read routine
10011	Amperif status present after read command issued
10100	HP/A timeout waiting for enable tags after read command issued
10101	HP/A timeout waiting for data after control unit enabled tags on read
10110	Amperif terminated read operation before sending data
10111	HP/A timeout in high-speed read loop because Amperif stopped sending data
11000	HP/A timeout waiting for status after a read operation
11001	Amperif abnormal read termination

lower 5-bit error codes: (continued)

bits 43210	
11010	Enable tags not present on entry to truncation routine
11011	HP/A timeout waiting for Amperif to take data before truncation
11100	Amperif input data present on entry to issued command routine

Start-up Diagnostics Error Codes

Bits 543210		FRU
100001	CPU Register Test Failed	HSP
100010	Local memory/address failed	HSP
100100	Not used	---
101000	U-bus interface FIFO failed	UBI

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6. REFERENCE

This section provides a reference for the following:

	page
1. AIO	6.2
2. AIX	6.3
3. BIOE	6.4
4. BIXE	6.5
5. CDCI (CDC interface)	6.6
6. DIFE (disk interface expansion)	6.8
7. EXXP	6.10
8. HSP (high-speed processor)	6.11
9. MDBP	6.12
10. MPCP (microprogram controller plugin)	6.14
11. OCP (operator control panel)	6.16
12. UBI (U-bus interface)	6.17
13. XMCIP (expanded microcontroller interface plugin)	6.18
14. XMC (expanded microcontroller)	6.20
15. XM16KP (expanded memory 16K plugin)	6.25

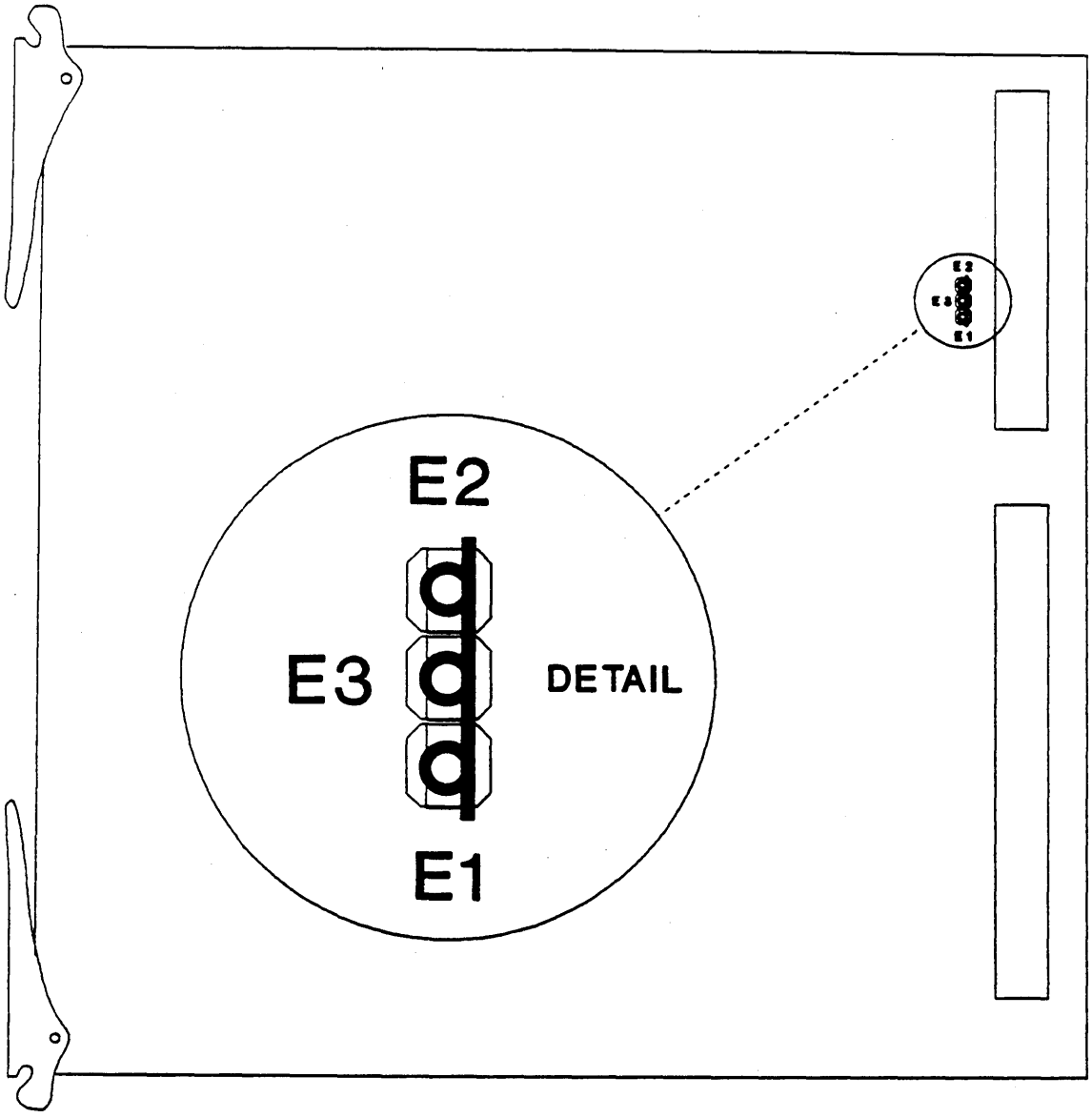


Figure 6-1
AIO Jumpers

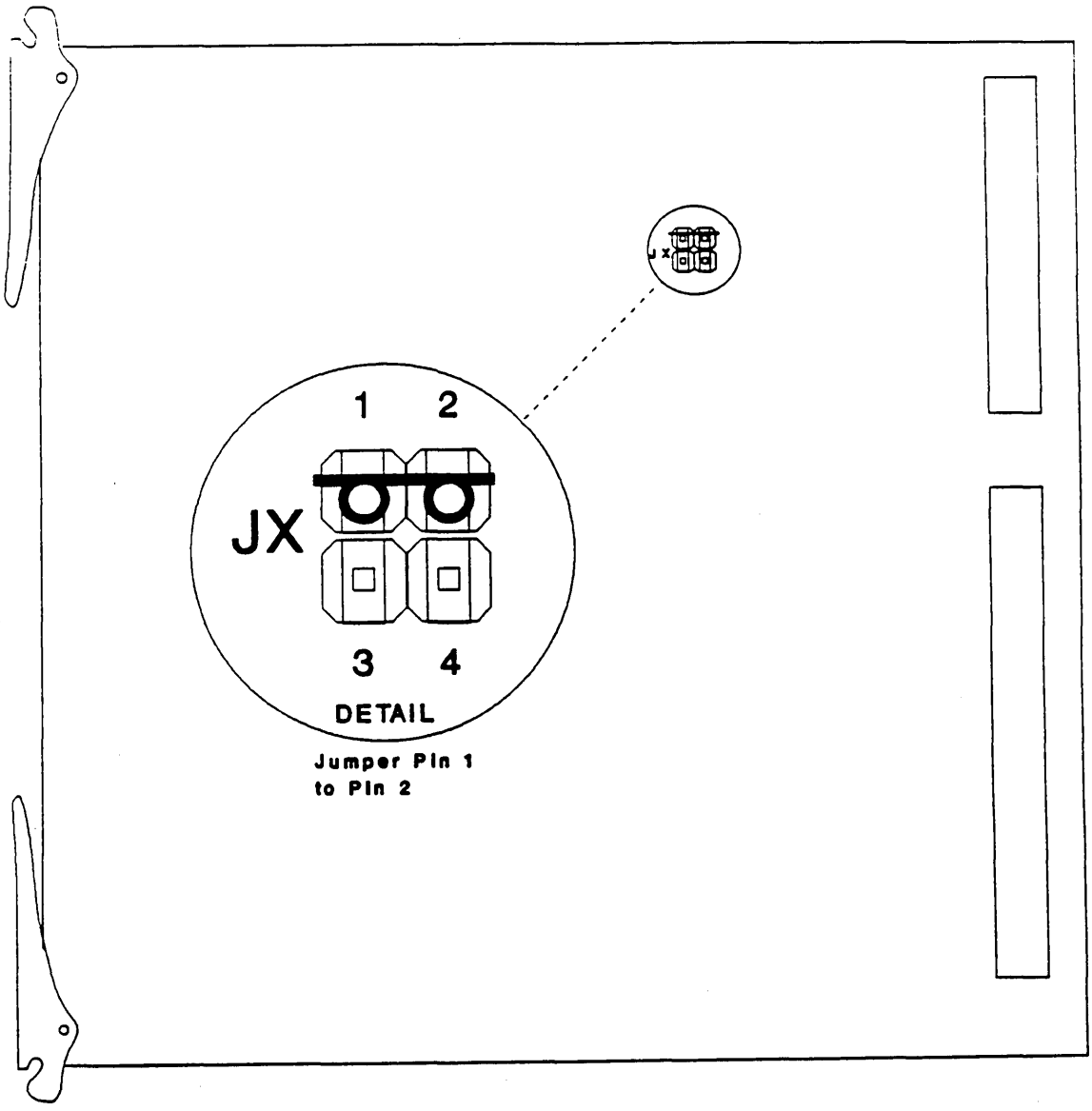
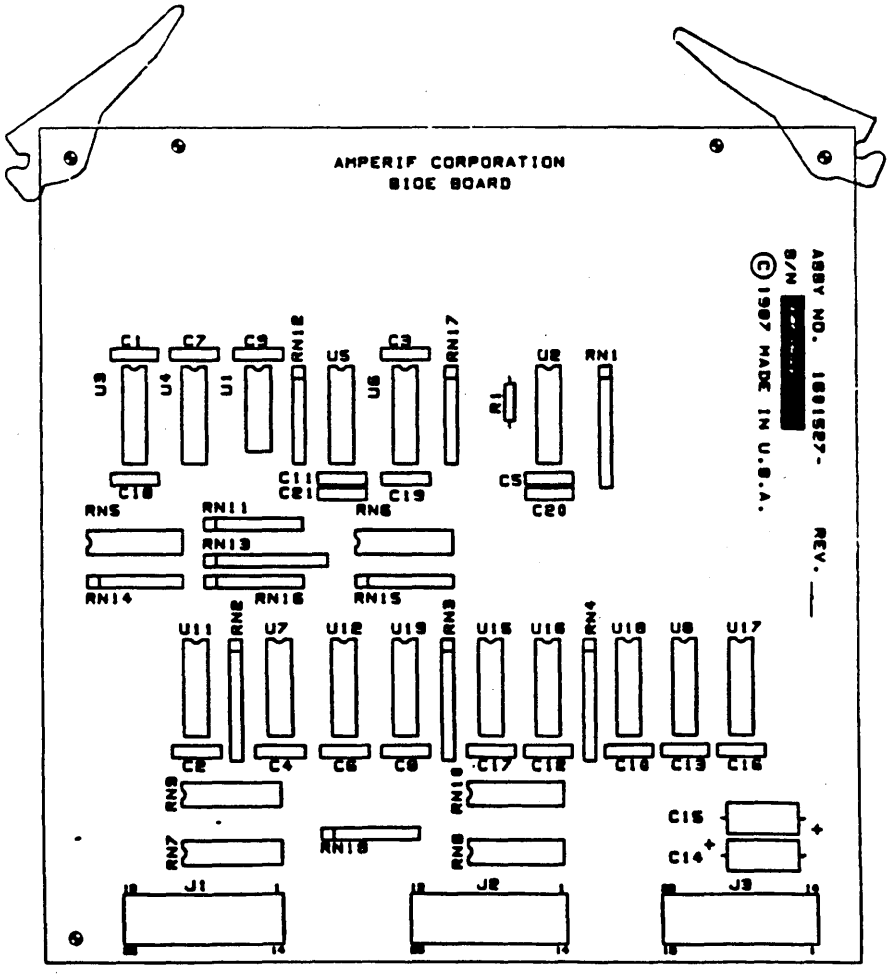


Figure 6-2
AIX Jumpers



COMPONENT SIDE

Figure 6-3
BIOE

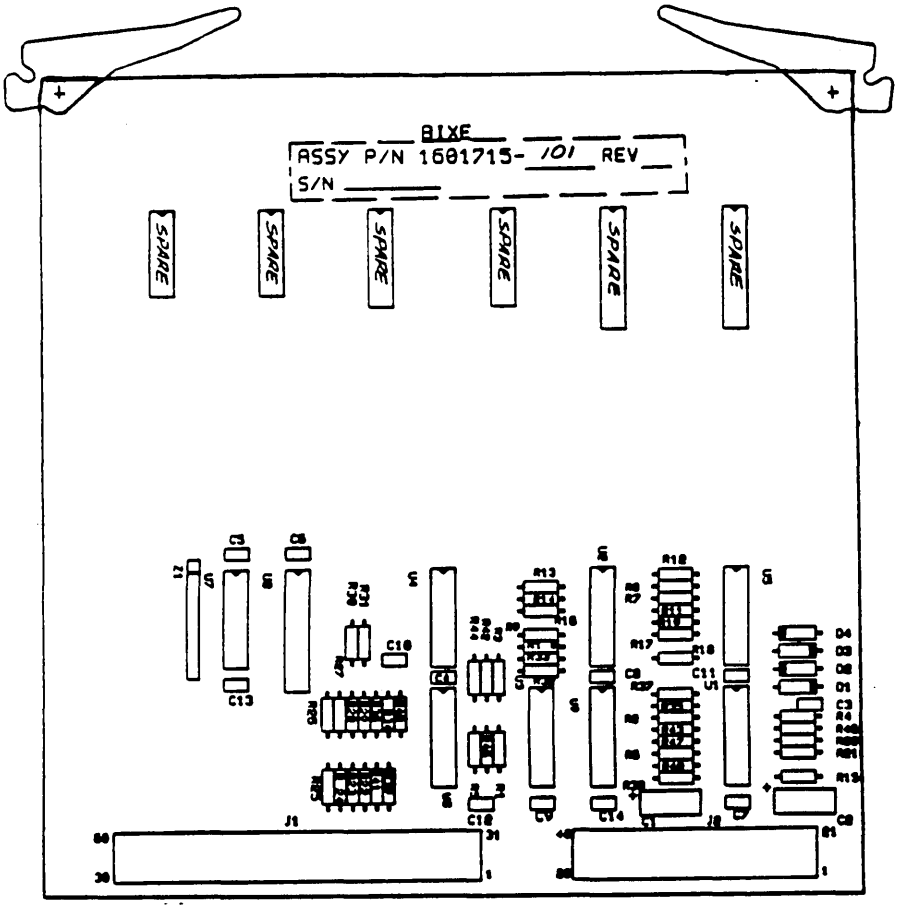


Figure 6-4
BIXE

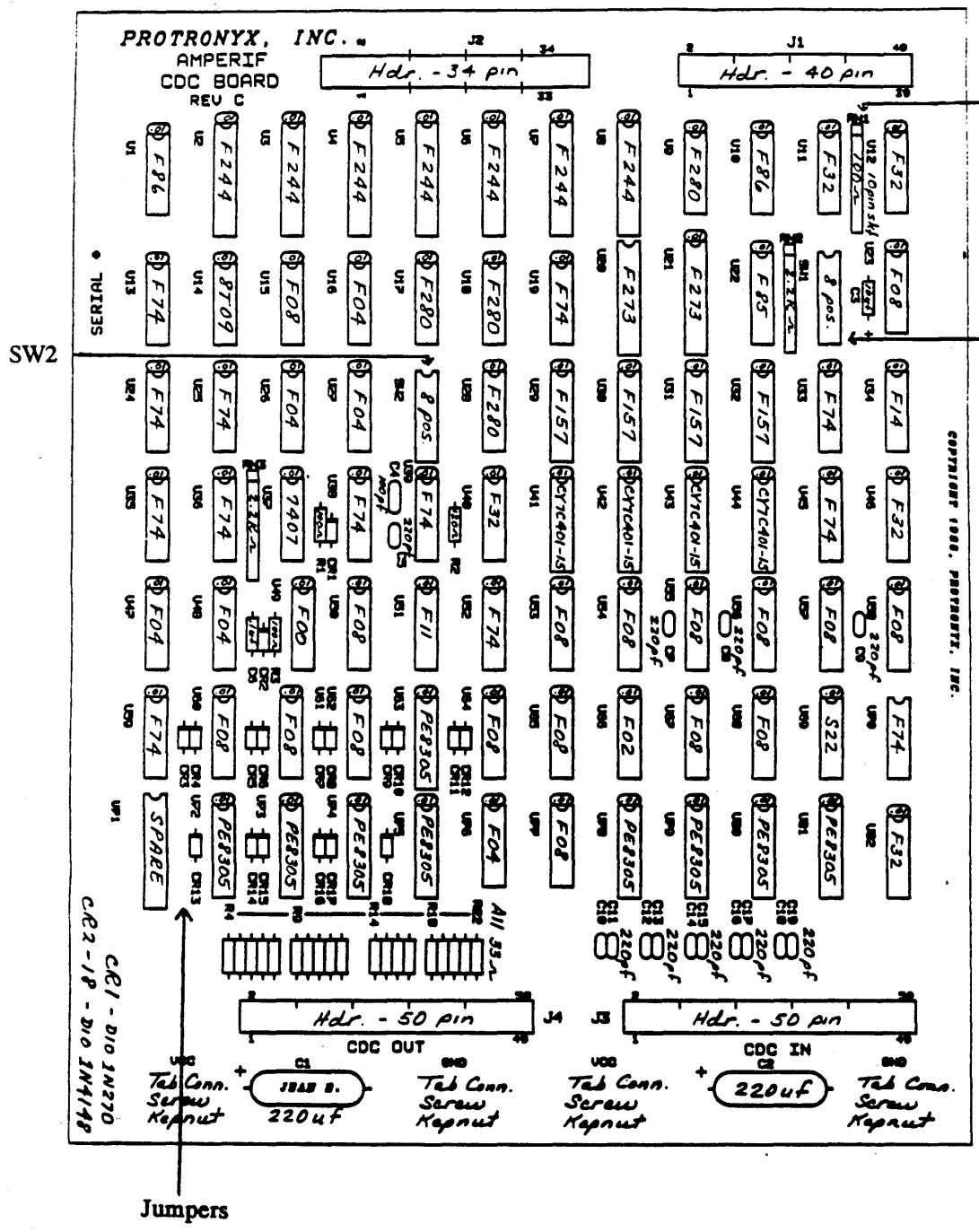
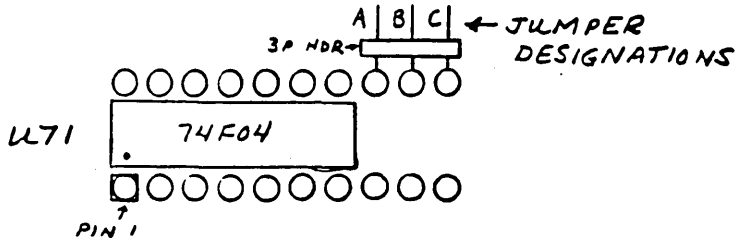


Figure 6-5
CDCI

CDCI Configuration Information

Jumpers

At the upper right of location U71, there is a three-pin header. For correct operation of the 7100-30, install jumper from header pin B to C. Refer to the following drawing.



Terminator

RN1:

This is a ten-pin socket which is unused on all CDCI boards except the CDCI board which has the highest number of all CDCI boards for that controller. For example, if your system has CDCI boards 0 through 3, RN1 will remain unused on CDCI boards 0, 1, and 2, but will have a terminator attached on CDCI board 3.

Switch Settings

SW1: There are eight switches on SW1. Switches 1 through 7 are set differently depending on the number of the CDCI board you are working with. The switch 8 setting indicates which controller the board pertains to. Detailed setting information follows.

SW1 switch settings for CDCI board 0:
switches 1 and 4 are OFF
switches 2,3,5,6, and 7 are ON
switch 8 ON if this board pertains to controller A
OFF if this board pertains to controller B

SW1 switch settings for CDCI board 1:
switches 1,3,5, and 7 are OFF
switches 2,4, and 6 are ON
switch 8 ON if this board pertains to controller A
OFF if this board pertains to controller B

SW1 switch settings for CDCI board 2:
switches 1,3,4,5, and 7 are OFF
switches 2 and 6 are ON
switch 8 ON if this board pertains to controller A
OFF if this board pertains to controller B

SW1 switch settings for CDCI board 3:
switches 1,2,5, and 6 are OFF
switches 3,4, and 7 are ON
switch 8 ON if this board pertains to controller A
OFF if this board pertains to controller B

SW2: There are eight switches on SW2. Switch 1 indicates maintenance mode and should always be set to OFF during normal processing. Switches 2 through 8 are used to adjust CDC channel timing. One and only one of these switches must be on at all times, though it doesn't matter which one you choose for this purpose.

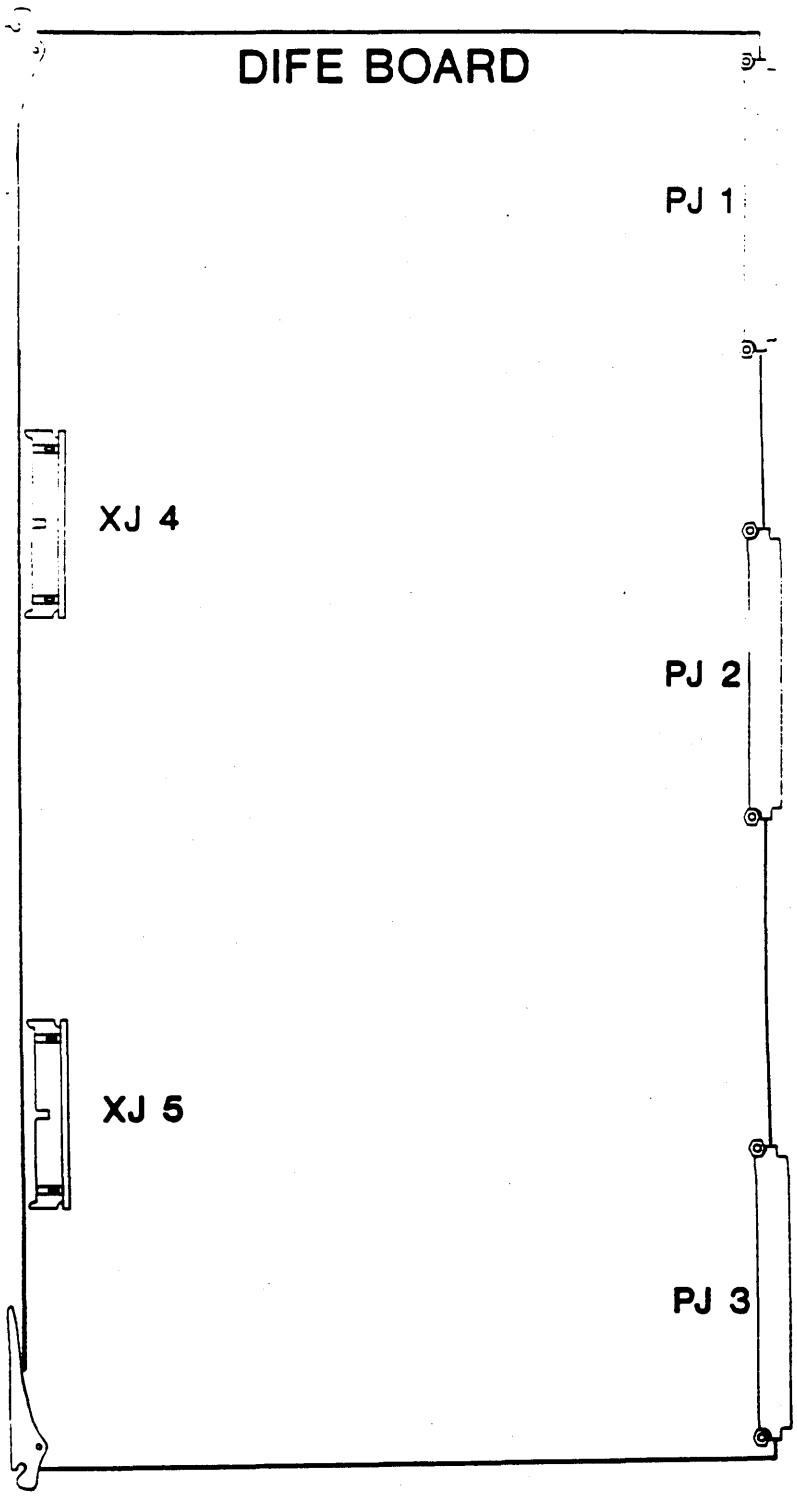


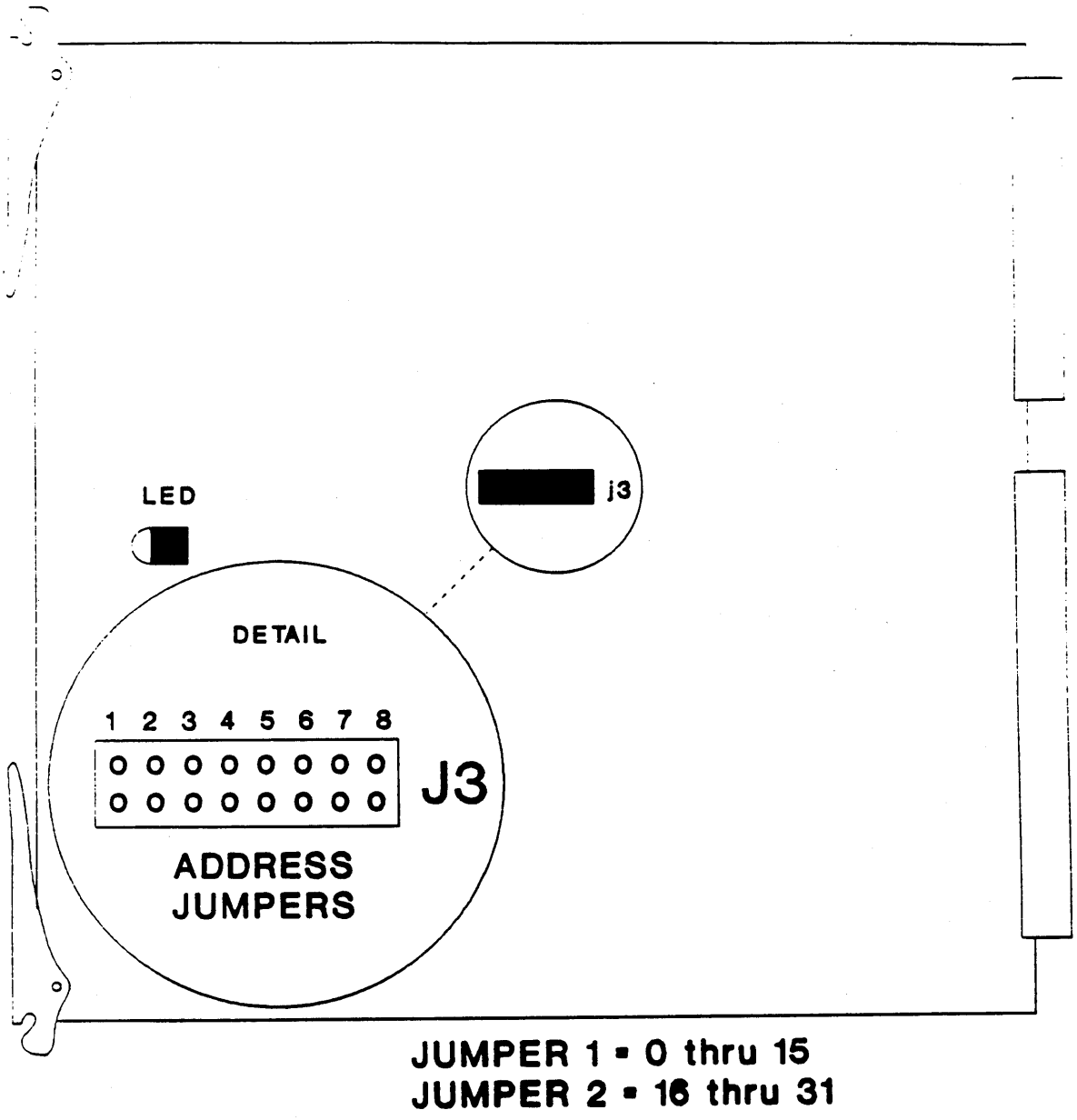
Figure 6-6
DIFE Test Points

DIFE Test Points

Test Points	Signal Name	Purpose
J4A-01	3INDEX	Index mark.
J4A-02	4AMDET	Address mark detected.
J4A-03	4RETRY	
J4A-04	9DIFER	DIFE error - indicates DIFE experienced an error during operation.
J4A-05	9OPCMPL	Operation completed normally.
J4B-01	4FILB00	File bus bits 00-07.
J4B-02	4FILB01	
J4B-03	4FILB02	
J4B-04	4FILB03	
J4B-05	4FILB04	
J4B-06	4FILB05	
J4B-07	4FILB06	
J4B-08	4FILB07	
J5A-01	9DRCLK	Drive clock - can be either read clock or servo clock from drive.
J5A-02	9SMDATI	Storage module data in - serial read data line
J5A-03	9SMDATO	Storage module data out - serial write data line
J5A-04	N/A	
J5A-05	4ENWRTGTE	Enable write gate at drive.
J5A-06	4ENRDGT	Enable read gate at drive.
J5A-07	4ENAM	Enable address mark detect at drive.
J5A-08	9SMDATA	
J5B-01	4FRWST00	
J5B-02	4FRWST01	
J5B-03	4FRWST02	
J5B-04	4FRWST03	
J5B-05	4ABREGEQ	
JB5-06	4ECC100	
JB5-07	4ECC101	
JB5-08	4ECC102	
JB5-09	4ECC103	
JB5-10	3ENFMWT	Enable format write.
JB5-11	3ENRDHDA	Enable read header.

NOTES:

- *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
- *Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.*



The LED is lit when this EXXP board is selected.

There are four EXXP boards in each 7100-30, but only two of these boards include terminators. The EXXP boards which have terminators (two per board) are the ones in slots G and L of the expansion cardcage. The terminators on these EXXP boards are on the lower right-hand portion of the component side of the board.

Figure 6-7
EXXP Jumpers

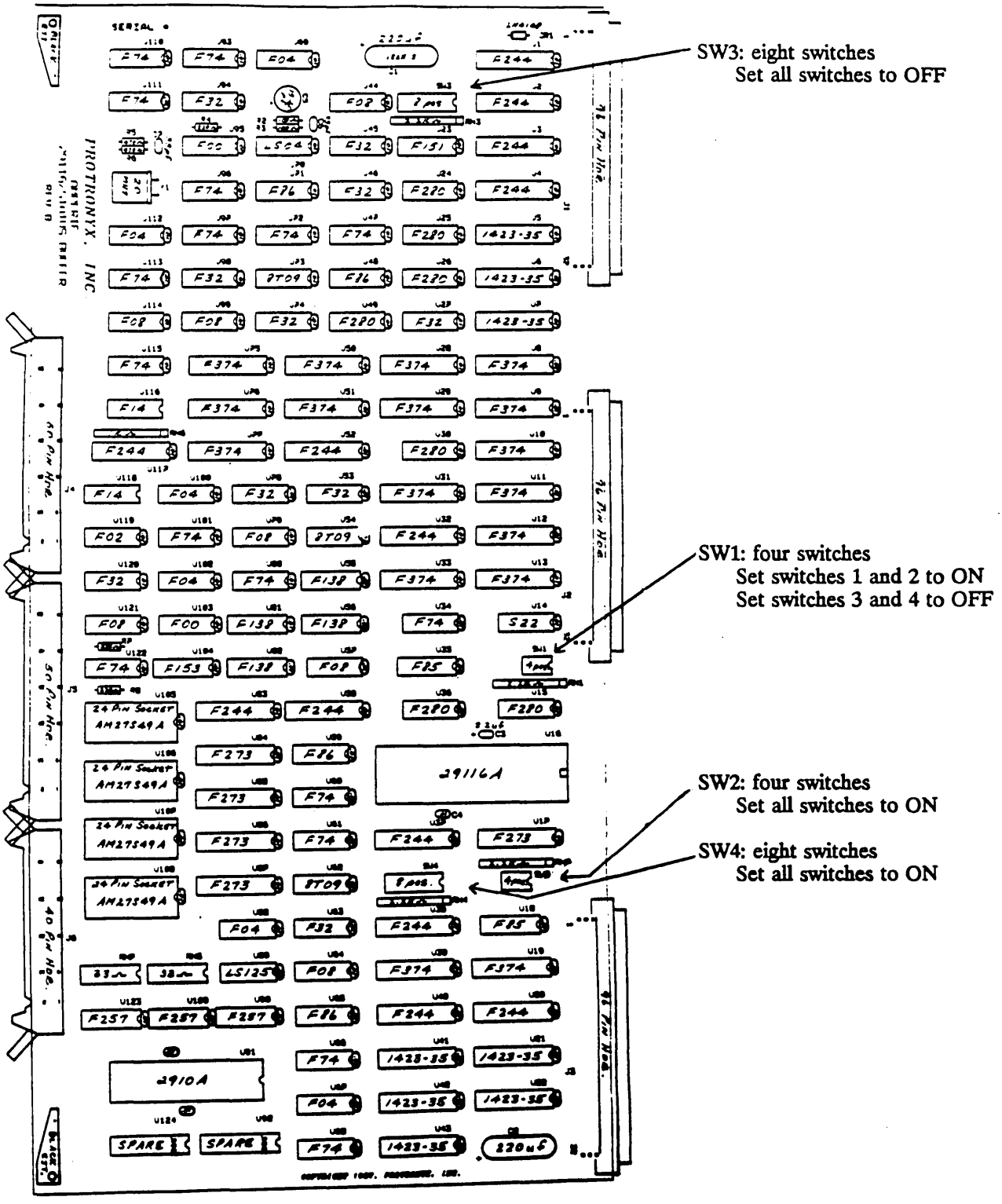


Figure 6-8
HSP

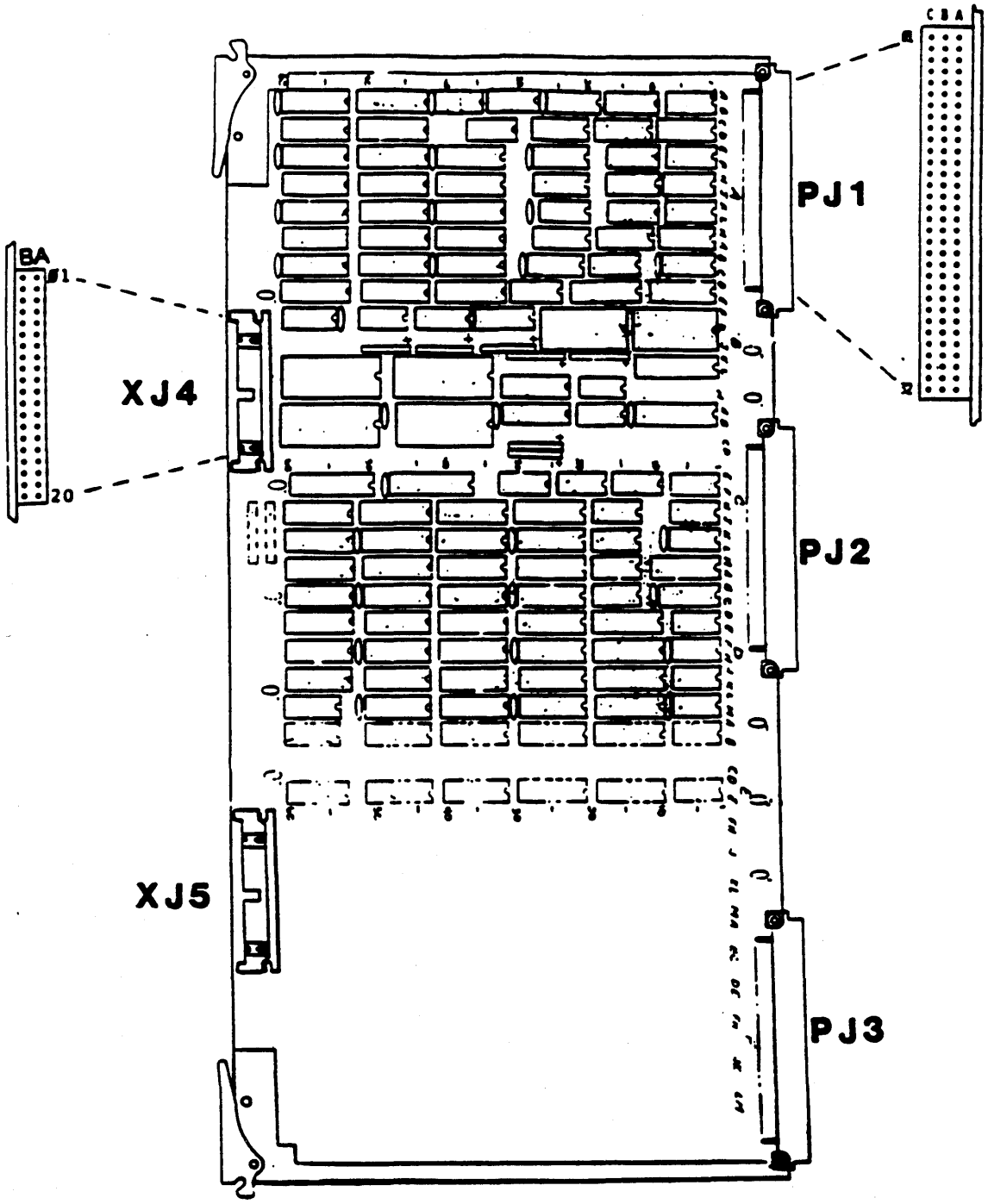


Figure 6-9
MDBP

MDBP TEST POINTS

Test Points	Signal Name	Purpose
J4A-01	7WDCNT00	HSSM Control Signals
J4A-02	7WDCNT01	
J4A-03	2UBREQ	
J4A-04	2BWC100	
J4A-05	2BWC101	
J4A-06	2BWC102	
J4A-07	2BWC103	
J4A-08	2UDONE	
J4A-09	2UCMPL	
J4A-10	7USREQMC	
J4A-11	7DMCTSEQ	
J4A-12	7MDBACK	
J4A-13	9HREQMC	
J4A-14	3MDBMDE0	
J4A-15	3MDBMDE1	
J4A-16	N/A	
J4A-17	N/A	
J4A-18	2SMCMPL	
J4A-19	2SDONE	
J5A-01	2MAR00	Data Buffer Memory Address Lines
J5A-02	2MAR01	
J5A-03	2MAR02	
J5A-04	2MAR03	
J5A-05	2MAR04	
J5A-06	2MAR05	
J5A-07	2MAR06	
J5A-08	2MAR07	
J5A-09	2MAR08	
J5A-10	2MAR19	
J5A-11	2MAR10	
J5A-12	2MAR11	
J5A-13	2MAR12	
J5A-14	2MAR13	
J5A-15	2MAR14	
J5A-16	2MAR15	

Test Points	Signal Name	Purpose
J4B-01	2DMAIO00	DMA Address Generator Input Lines
J4B-02	2DMAIO01	
J4B-03	2DMAIO02	
J4B-04	2DMAIO03	
J4B-05	2DMAIO04	
J4B-06	2DMAIO05	
J4B-07	2DMAIO06	
J4B-08	2DMAIO07	

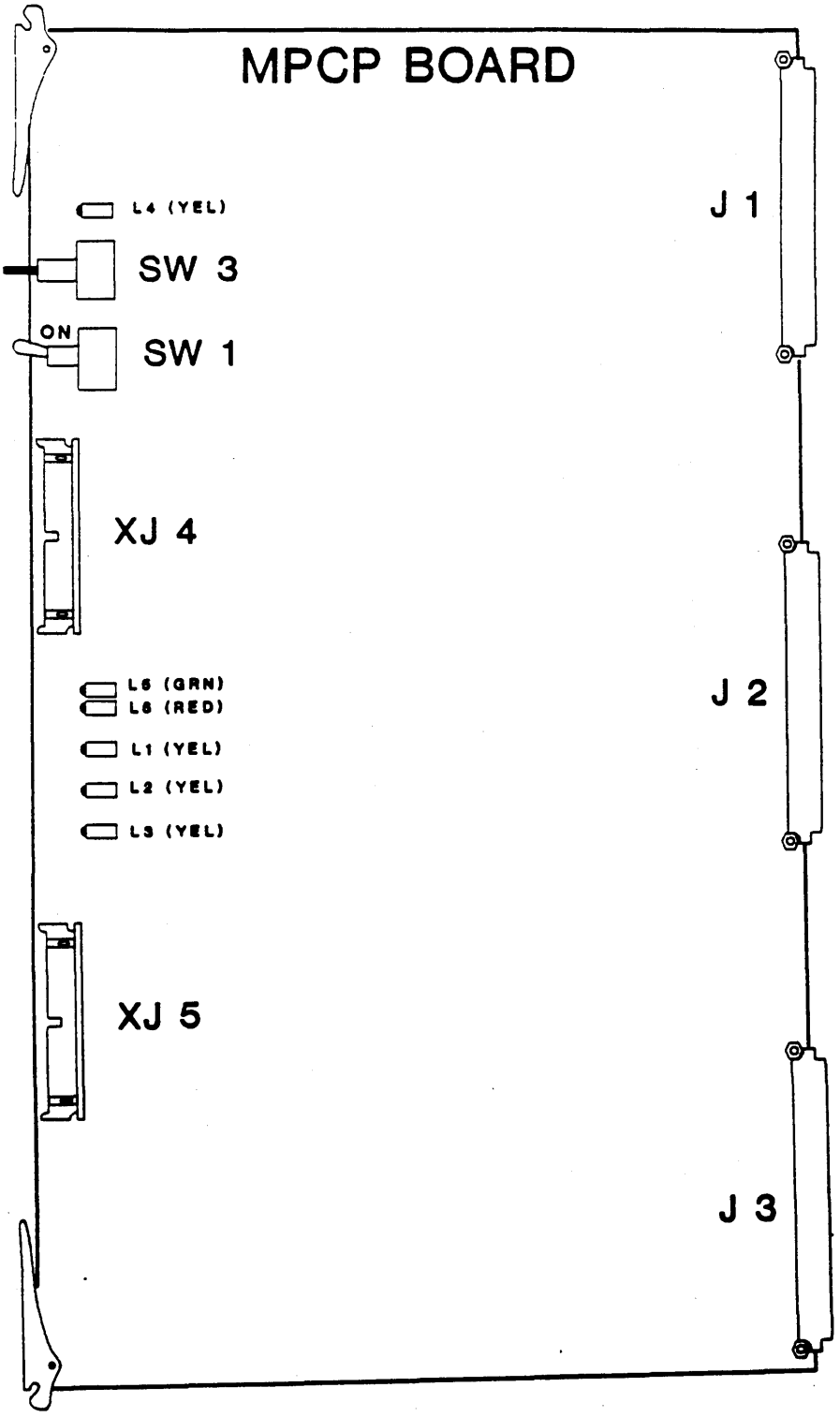


Figure 6-10
MPCP - Layout of Test Points, Switches, and LEDs

MPCP TEST POINTS, SWITCHES, AND LEDs

Test Points	Signal Name	Purpose	Test Points	Signal Name	Purpose
J4A-01	3MPC00	MPCP	J4B-01	3ALUO00	
J4A-02	3MPC01	Microprogram	J4B-02	3ALUO01	
J4A-03	3MPC02	Address	J4B-03	3ALUO02	2901B
J4A-04	3MPC03	Lines	J4B-04	3ALUO03	ALU "Y"
J4A-05	3MPC04		J4B-05	3ALUO04	Outputs
J4A-06	3MPC05		J4B-06	3ALUO05	
J4A-07	3MPC06		J4B-07	3ALUO06	
J4A-08	3MPC07		J4B-08	3ALUO07	
J4A-09	3MPC08		J4B-09	3ALUIO00	
J4A-10	3MPC09		J4B-10	3ALUIO01	
J4A-11	3MPC10		J4B-11	3ALUIO02	2901B ALU
J4A-12	3MPC11		J4B-12	3ALUIO03	I/O BUS
J4A-13	N/A		J4B-13	3ALUIO04	
J4A-14	N/A		J4B-14	3ALUIO05	
J4A-15	N/A		J4B-15	3ALUIO06	
J4A-16	N/A		J4B-16	3ALUIO07	
J4A-17	8MCLKO	MPCP System Clock			

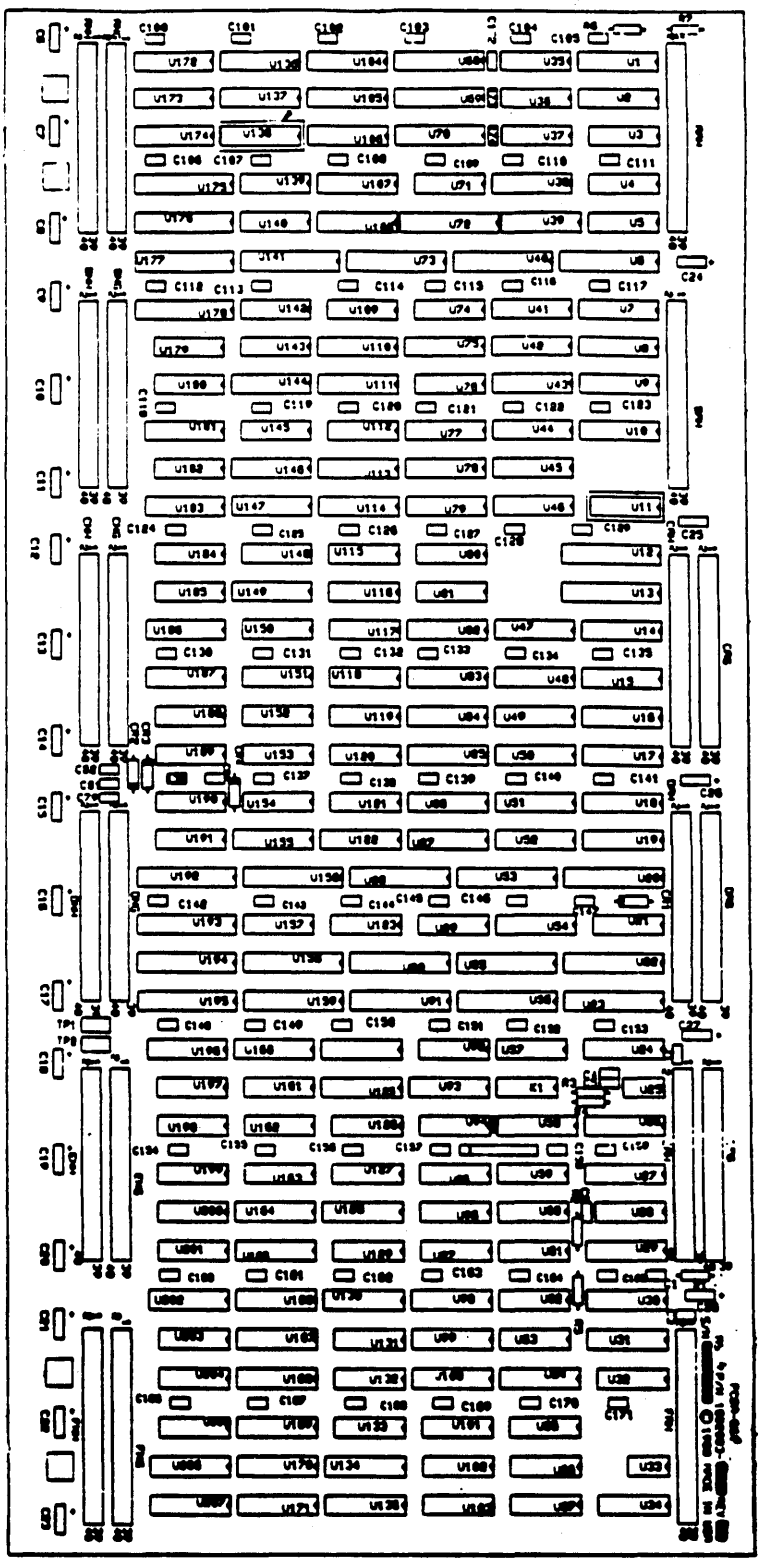
Switches

SW1	BD65	BD65-01...8HALT	MPCP clock start/stop switch
[toggle]	BD65	BE65-01...8RUN	
SW3 (Reset)	AM65	AM65-01...8SWRS0	Clears microsequencer to 0
[momentary push button]	AM65	BA65-03...8SWRS0	

LEDs

LED-4 (YELLOW)	3IDLEL	When on, a wait loop condition exists.
LED-5 (GREEN)	3ERRL	When on, self-test has completed successfully.
LED-6 (RED)	3CMPL	When on, an error has occurred.
LED-1 (YELLOW)	3ENMDRDM	When on, data is being transferred to channel (U-side memory read)
LED-2 (YELLOW)	3ENRDHDA	When on, the read header/read data function is active.
LED-3 (YELLOW)	3ENFMWT	When on, the format write function is active.

LED3	LED2	
0	0	Read Header
0	1	Read Data
1	0	Write Data
1	1	Format



COMPONENT SIDE **Figure 6-11**
OCP

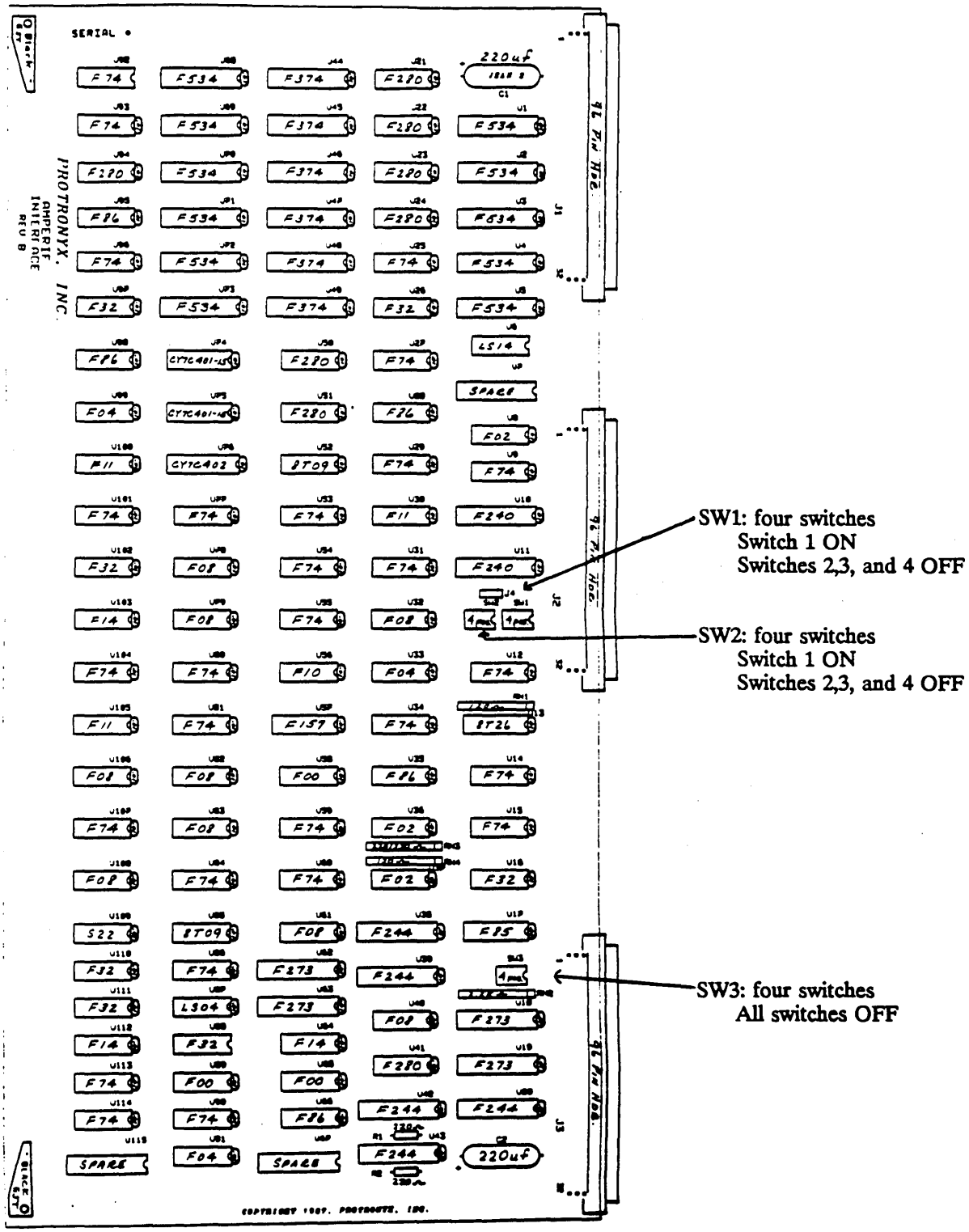


Figure 6-12
UBI

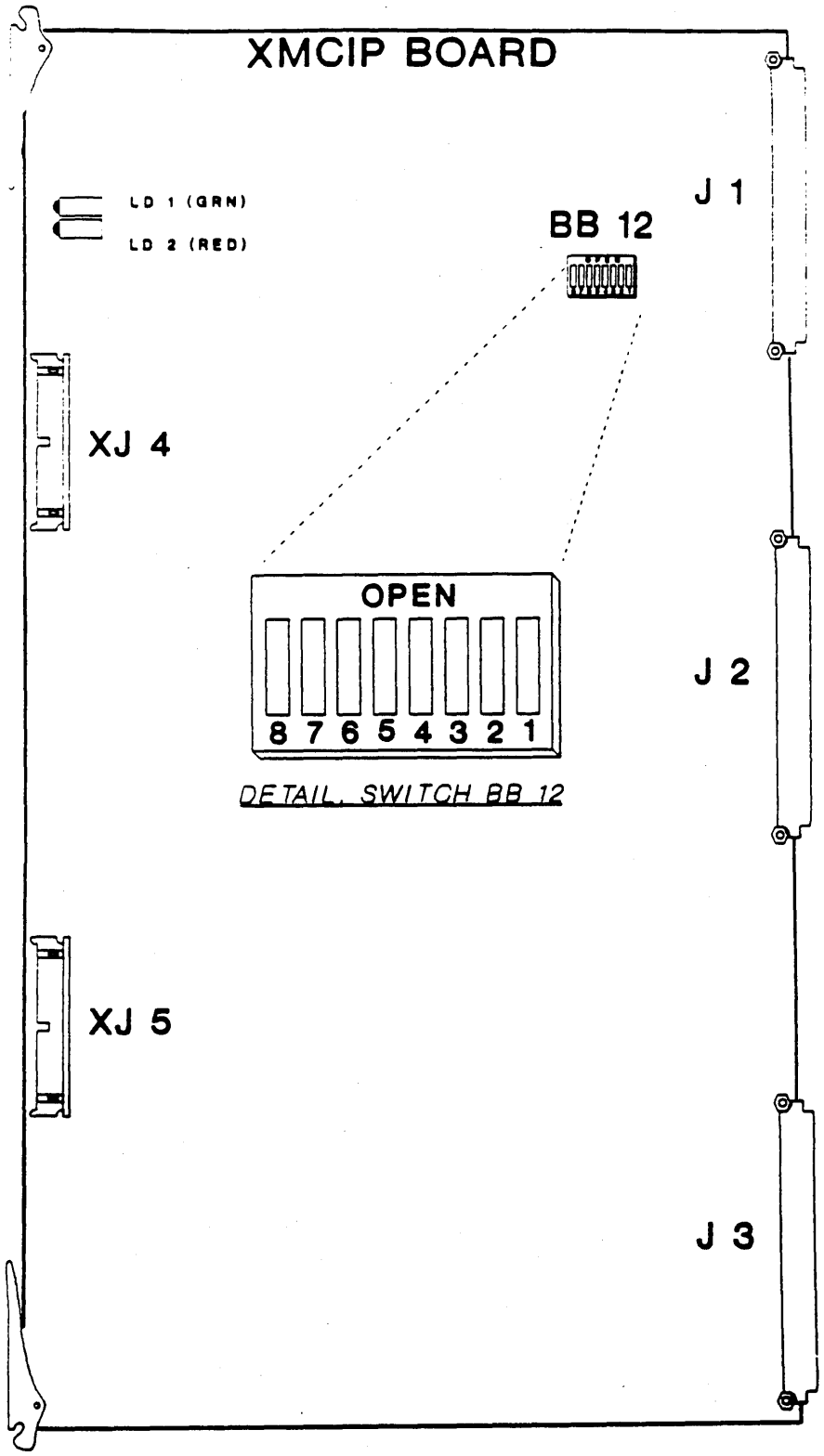


Figure 6-13
XMCIP - Layout of Test Points, Switches, and LEDs

XMCIP TEST POINTS, SWITCHES, LEDs

Test Points	Signal Name	Purpose
J4A-15	10DACK	Output Data Acknowledge Tag for U-bus.
J5A-01	6CMCB00	CMC-bus bits 00-07 + parity.
J5A-02	6CMCB01	
J5A-03	6CMCB02	
J5A-04	6CMCB03	
J5A-05	6CMCB04	
J5A-06	6CMCB05	
J5A-07	6CMCB06	
J5A-08	6CMCB07	
J5A-09	6CMCBP	
J5B-01	6CTB00	CT-bus bits 00-11 + parity.
J5B-02	6CTB01	
J5B-03	6CTB02	
J5B-04	6CTB03	
J5B-05	6CTB04	
J5B-06	6CTB05	
J5B-07	6CTB06	
J5B-08	6CTB07	
J5B-09	6CTB08	
J5B-10	6CTB09	
J5B-11	6CTB10	
J5B-12	6CTB11	
J5B-13	6CTBP	
JB5-17	6CLKIAA	

LEDs

LED-1 (GREEN)	AL62 AL62-01...6XMIFIB	When on, an operation has successfully completed.
LED-2 (RED)	AM62 AM62-01...6XMIFIA	When on, a disk error has occurred.

Switches

BB12-01	BC19-09...1SWXIF7 (BD ADR SW)	Switch 1 and 6 are always open.
BB12-02	BC18-10...1SWXIF6 (BD ADR SW)	Switches 2,3,4,5,7, and 8 are left closed.
BB12-03	BC17-11...1SWXIF5 (BD ADR SW)	
BB12-04	BC16-12...1SWXIF4 (BD ADR SW)	
BB12-05	BC15-13...1SWXIF3 (BD ADR SW)	
BB12-06	BC14-14...1SWXIF2 (BD ADR SW)	
BB12-07	BC13-15...1SWXIF1 (BD ADR SW)	
BB12-08	BC12-16...1SWXIF0 (BD ADR SW)	

NOTES:

- *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
- *Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.*

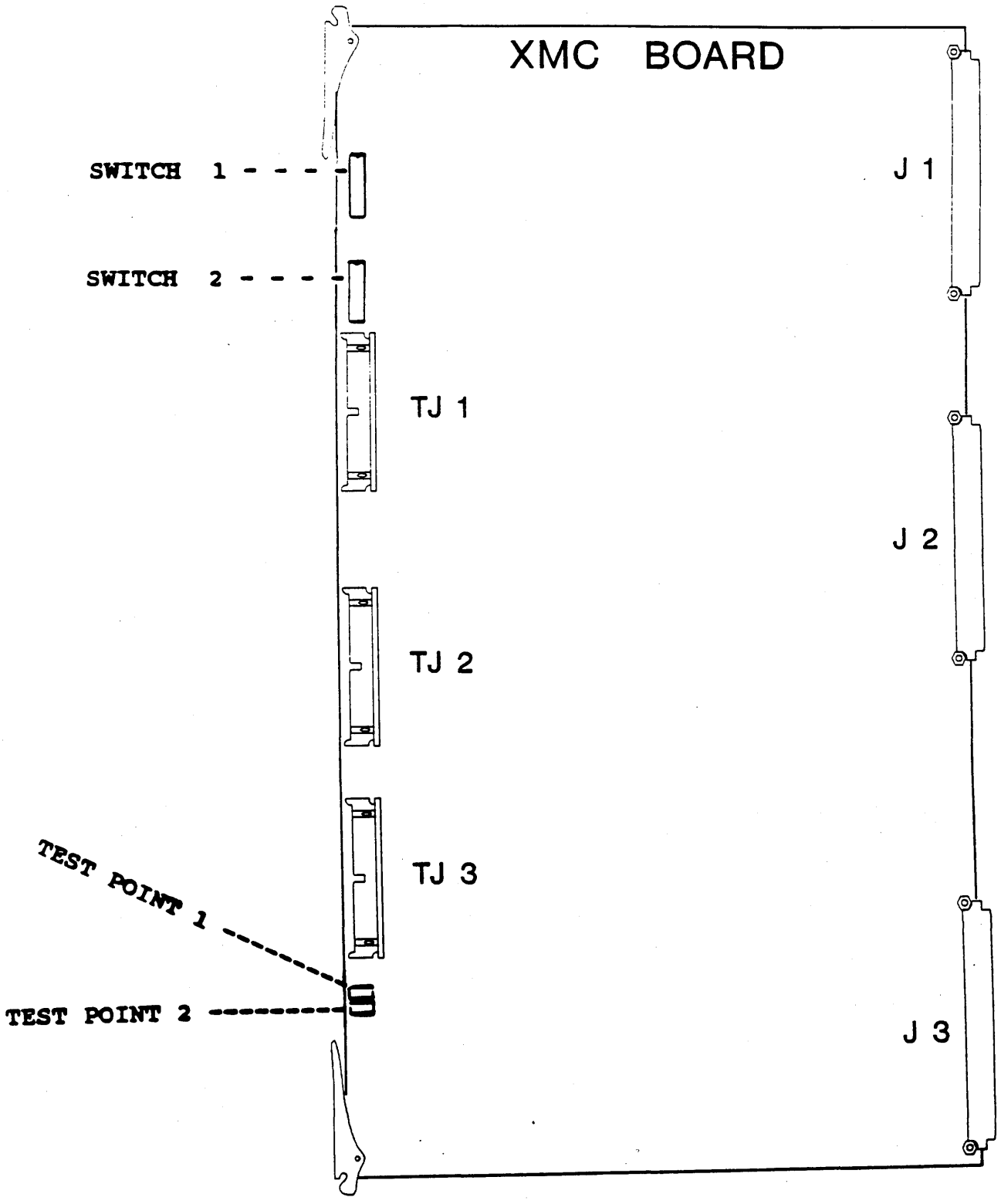


Figure 6-14
XMC - Layout of Jumpers and Test Points

XMC SWITCH OPTIONS

SW1

For the 7100-30, all eight switches which comprise SW1 should be switched to the open position. (The open position is 0.)

SW2

For the 7100-30, the eight switches which comprise SW2 should be set as follows:

switch 1 - closed (1)

switch 2 - closed (1)

switch 3 - open (0)

switch 4 - open (0)

switch 5 - closed (1)

switch 6 - closed (1)

switch 7 - open (0)

switch 8 - open (0)

XMC TEST POINTS

Test Point TJ1	Signal Name	Purpose
TJ1-01	6CTB00	CT-bus bits 00-11 + parity. See XMC block diagram.
TJ1-03	6CTB01	
TJ1-05	6CTB02	
TJ1-07	6CTB03	
TJ1-09	6CTB04	
TJ1-11	6CTB05	
TJ1-13	6CTB06	
TJ1-15	6CTB07	
TJ1-17	6CTB08	
TJ1-19	6CTB09	
TJ1-21	6CTB10	
TJ1-23	6CTB11	
TJ1-25	6CTBP	
TJ1-27	N/A	
TJ1-29	N/A	
TJ1-31	7ODREQB	Output data request \
TJ1-33	6ODACK	Output data acknowledge | U-bus
TJ1-35	7SET1DRB	Set input data request | tags
TJ1-37	51DACKB	Input data acknowledge /
TJ1-02	2SEQAR00	Sequencers address register bits 00-13. This register outputs the current
TJ1-04	2SEQAR01	microprogram address. See XMC block diagram.
TJ1-06	2SEQAR02	
TJ1-08	2SEQAR03	
TJ1-10	2SEQAR04	
TJ1-12	2SEQAR05	
TJ1-14	2SEQAR06	
TJ1-16	2SEQAR07	
TJ1-18	2SEQAR08	
TJ1-20	2SEQAR09	
TJ1-22	2SEQAR10	
TJ1-24	2SEQAR11	
TJ1-26	2SEQAR12	
TJ1-28	2SEQAR13	
TJ1-30	N/A	
TJ1-32	2CLK1	
TJ1-34	6CLK1	
TJ1-36	2CLK2SYE	Clock to other system boards. Generated from XMC master clock circuitry.
TJ1-38	6CLK2SYE	"

NOTE: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.

XMC TEST POINTS (continued)

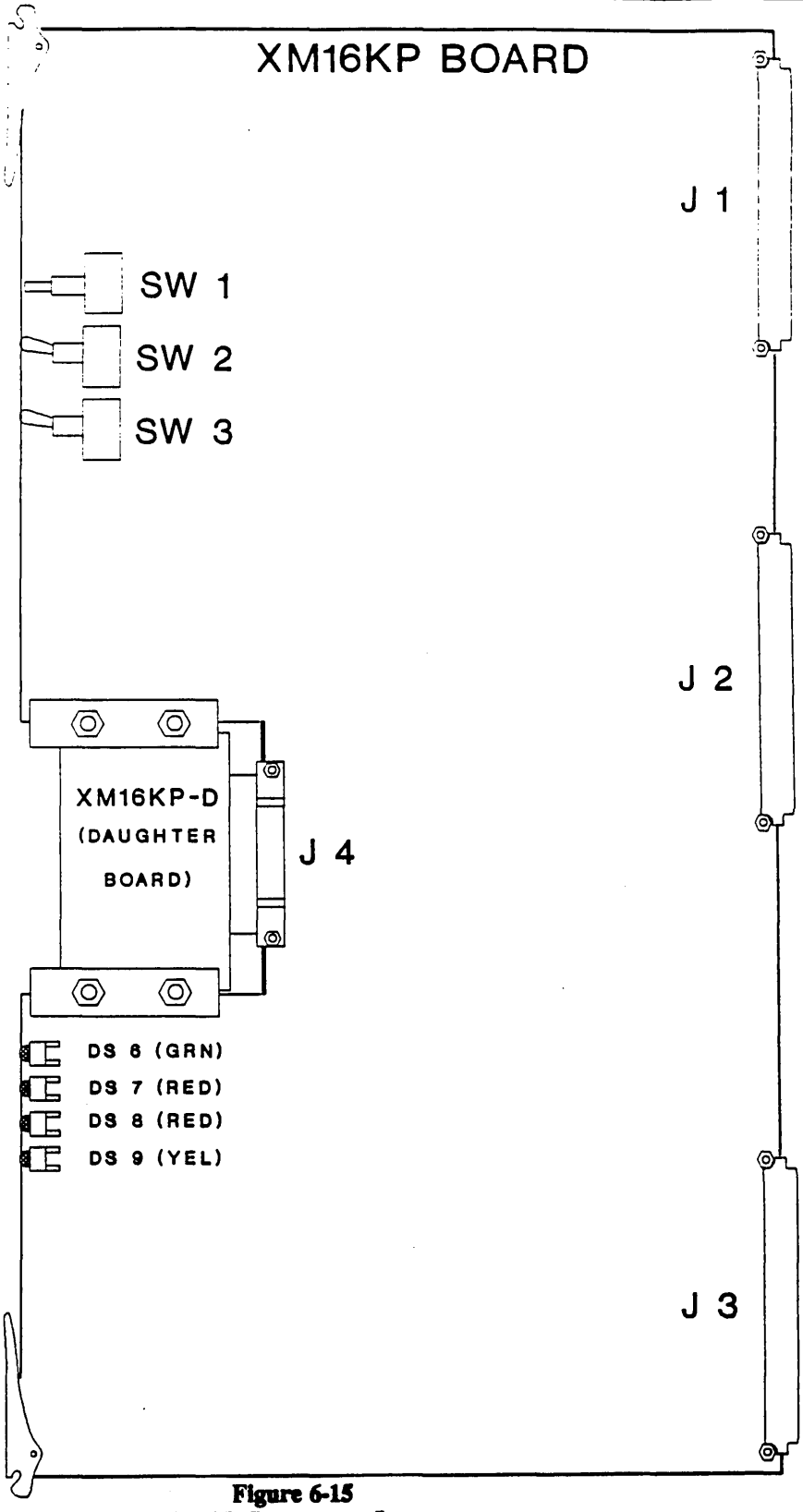
Test Point TJ2	Signal Name	Purpose
TJ2-01	2SPAD00	Scratchpad memory address lines 00-09.
TJ2-03	2SPAD01	
TJ2-05	2SPAD02	
TJ2-07	2SPAD03	
TJ2-09	2SPAD04	
TJ2-11	2SPAD05	
TJ2-13	2SPAD06	
TJ2-15	2SPAD07	
TJ2-17	2SPAD08	
TJ2-19	2SPAD09	
TJ2-21	6RDSPAD	Scratchpad memory read enable.
TJ2-23	6SPWEN	Scratchpad memory write enable.
TJ2-25	2SPAD10	
TJ2-27	2SPAD11	
TJ2-29	N/A	
TJ2-31	N/A	
TJ2-33	N/A	
TJ2-35	N/A	
TJ2-37	N/A	
TJ2-02	2ALUY00	ALU Y-bus bits 00-11 + parity. This bus is the output of the ALU. See XMC block diagram.
TJ2-04	2ALUY01	
TJ2-06	2ALUY02	
TJ2-08	2ALUY03	
TJ2-10	2ALUY04	
TJ2-12	2ALUY05	
TJ2-14	2ALUY06	
TJ2-16	2ALUY07	
TJ2-18	2ALUY08	
TJ2-20	2ALUY09	
TJ2-22	2ALUY10	
TJ2-24	2ALUY11	
TJ2-26	2ALUYP	
TJ2-28	2UCZEROA	
TJ2-30	2CNDTST	Condition test bit to next address control PROM.
TJ2-32	N/A	
TJ2-34	N/A	
TJ2-36	9CPRST	OCP reset signal to XMC. Activated by button on maintenance panel.
TJ2-38	2ADRSYNC	Address sync signal to event count on OCP. Active for 200 nanoseconds when breakpoint address and microprogram address are the same.

NOTE: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8 or 9 are low (0V) when active.

XMC TEST POINTS (continued)

Test Point TJ3	Signal Name	Purpose
TJ3-01	6ALUD00	ALU D-bus bits 00-11. These are the direct data input lines to the ALU. This bus has multiple sources. See XMC block diagram.
TJ3-03	6ALUD01	
TJ3-05	6ALUD02	
TJ3-07	6ALUD03	
TJ3-09	6ALUD04	
TJ3-11	6ALUD05	
TJ3-13	6ALUD06	
TJ3-15	6AL7D07	
TJ3-17	6ALUD08	
TJ3-19	6ALUD09	
TJ3-21	6ALUD10	
TJ3-23	6ALUD11	
TJ3-25	N/A	
TJ3-27	N/A	
TJ3-29	N/A	
TJ3-31	2UPERL	U-bus parity error on lower bits (00-17) of the U-bus.
TJ3-33	2UPERU	U-bus parity error on upper bits (18-36) of the U-bus.
TJ3-35	2SPPER	Scratchpad parity error when reading out of scratchpad memory.
TJ3-37	2CTSDPER	CT-bus parity error when XMC is receiving data on CT-bus.
TJ3-28	3ENCLK1	To halt/run clocks from OCP. Remove jumper when running online.
TJ3-30	3ENCLK1A	
TJ3-36	5USYSCRR	To enable system clear signal from host CPU, jumper TJ3-36 and J3-38 together.
TJ3-38	5USYSCRB	

NOTE: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.



Manual Controls

SW1
push button
which loads microcode

SW2
online/offline toggle

SW3
EPROM enable/disable
toggle

Connectors

J1 \
J2 | backplane
J3 /

J4 - daughter board

Status LEDs

DS 6 (green)
online/offline

DS 7 (red)
load error

DS 8 (red)
SRAM error

DS 9 (yellow)
EPROM
enabled/disabled

Figure 6-15
XM16KP Component Layout

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7. POWER ON/OFF PROCEDURES

This section provides power on and power off procedures for a 7100-30 Mass Storage System.

7.1 7100-30 Power On Procedure

All circuit breakers for the dual controller and disk drives are located at the front of the cabinet in the AC power box. See figure 7-1 for an illustration of the AC power box within the cabinet.

1. Turn on power to the controller. Turn on circuit breakers, located in the AC power box, in the following order: MAIN POWER, FANS, OCP, CHANNEL A, CHANNEL B (CHANNEL refers to each controller), and the drives.

2. The system automatically reinitializes both controllers.

3. Powering on the controller automatically initiates the 7100-30 controller confidence test. If these tests pass, **CHANNEL READY** appears at the OCP display indicating both controllers have been cleared. If a controller confidence test fails, a message is displayed on the function/status display of the OCP or on thumbwheel display 555, bits 35-24. See section 7.2 below for details about the 7100-30 controller confidence tests.

4. Turn on power to all disk drives in the system as follows:

   a. Press the PWR switch for disk drive 0; this switch is located on the drive control panel of the 7100-30 cabinet.

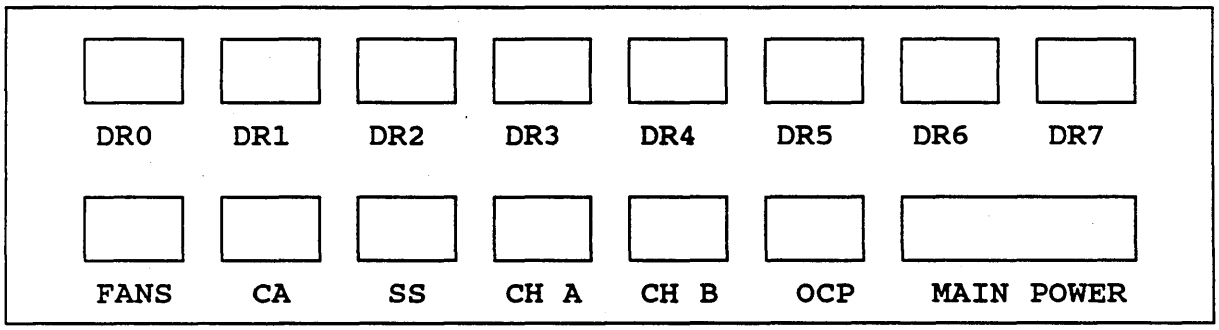
   b. Repeat step a for each disk drive in the system.

   c. Ensure that the RDY indicator is lit for every disk drive. This indicator should light about 15 seconds after the PWR switch is pressed. It indicates that the drive is up to speed and ready for operation.

5. At the OCP keypad, set the current time by pressing **LOAD 0**. Then enter the current time as HH MM SS. See section 5.2.2 for further information.

6. If applicable, set the backup time (press **LOAD 1**) and interval time (press **LOAD 2**) to the desired values. See sections 5.2.3 and 5.2.4 respectively for further information.

7. Remove the drives from write protect. At the drive panel, depress the WRITE PROTECT switch so it is no longer lit; the system is now ready for normal operation.



NOTES:

DR0 controls drives 0 and 1.
DR1 controls drives 2 and 3.
DR2 controls drives 4 and 5.
DR3 controls drives 6 and 7.
DR4 controls drives 8 and 9.
DR5 controls drives 10 and 11.
DR6 controls drives 12 and 13.
DR7 controls drives 14 and 15.
CA and SS are nonfunctional in the 7100-30.

Figure 7-1
AC Power Box in the 7100-30 Cabinet

7.2 7100-30 Controller Confidence Test

The 7100-30 controller confidence test is designed to verify the proper operation of controller hardware. It is automatically executed in the following cases:

- o When powering on the controller
- o When Toggle 7 is issued from the OCP
- o When Toggle 17 is issued from the OCP

7.2.1 How to Monitor Test Results

XMC and XM16KP Tests. To determine the results of the XMC and XM16KP test, set the DISPLAY/SELECT thumbwheel switch on the OCP to EXX, (where XX represents any two hexadecimal characters). If one or both of these tests fail, a binary code significant of the type of error will be displayed on the operations/maintenance display, bits 13-0. The binary codes are listed and explained in section 7.2.2.

Information about the XMC and XM16KP tests and about communication between these boards and other parts of the system is also available from thumbwheel switch setting 555, as described below under "OCP Test."

Note that if the XMC and XM16KP tests pass, the OCP test commences. If an XMC or XM16KP test fails, the 7100-30 confidence test program enters an endless loop, and no further tests are performed.

UBI and HSP Tests. The UBI and HSP tests are run at the same time that the OCP tests are run. To determine the results of the UBI and HSP tests, set the DISPLAY/SELECT thumbwheel switch on the OCP to 4D0. If the tests were successful, the hex display shows 81F100000. If either of the tests produced an error, the following bits are set:

bits 18,19	A NO OP command.
bit 35	An external function has been sent from the host.

Bits 0-11 shows an error code which tells you what the error was. See section 5.4.3 for detailed information about these error codes.

OCP Test. To determine the results of the OCP test, set the DISPLAY/SELECT thumbwheel switch to 555, bits 35-24. This is the display associated with the SMB memory location 3FF, which is used as the controller status word (CSW) for all these tests. Only the five LSBs are meaningful, and each of them is assigned to a particular board or set of boards as follows:

Bit 0: If 0, the XMC and XM16KP boards pass. If 1, the XMC and/or XM16KP board is failing.

Bit 1: If 0, communication between the XMC and the OCP passes. This also indicates that the CT-bus and the INST-bus probably pass, subject to further verification. If 1, communication between the XMC and the OCP is bad.

Bit 2: If 0, communication between the XMC and the XMCIP passes. Also, the CT-bus, and the INST-bus probably pass, subject to further verification. If 1, communication between the XMC and XMCIP is bad.

(Note that the CT-bus and INST-bus cannot be directly tested by the program. However, most test routines use these buses for communication between the XMC and other tested boards. so that the successful completion of these tests indicates high probability of the buses' proper operation.)

In the process of testing the controller boards, the bit corresponding to the board or set of boards under test is reset if the test is passed. If a board is failing, the corresponding bit is left set. The program branches to the next test regardless of the previous test results. (The XMC and XM16KP board tests are exceptions to this rule; see below.)

HSSM Test. Check the function/status display on the OCP; if the HSSM test fails, an error message is shown on this display. Error messages are listed and explained later in section 7.2.

When more than one board fails. When more than one board fails, the message corresponding to the first failure detected is the only one displayed. The order of failure detection is identical to the order of tests:

1. XMC & XM16KP
2. OCP
3. HSSM

7.2.2 XMC and XM16KP Test

This routine checks the proper operation of the various blocks on the XMC and XM16KP boards. Each such block is assigned a bit at SMB location 3FE. Bit definition of SMB memory location 3FE (thumbwheel display location 554, bits 11-0) is as follows:

Bit Number	Definition
0	Push pop stack
1	Event counter related operations
2	Transfer register
3	ALU internal operations (2901s)
4	I REG
5	Vector priority encoder
6	Scratchpad memory (SMB) (including parity check)
7	U-bus driver and receiver (including parity test)
8	Sequencer address register
9	Sequencer/AR related operations
10,11	Not used (always 00)

In the process of testing, the bit corresponding to the block under test is reset if the block passes. If the block fails, execution of the entire program terminates, leaving the corresponding bit and the bits of the untested blocks set, and the program enters an infinite loop. In this case, no further tests are possible.

The type of error is determined by setting the display select thumbwheel switch to EXX and reading the operations/maintenance display. The operations/maintenance display readouts and their associated errors are as follows:

Operations/Maintenance Display Readout	Error Description
2DF0	Push pop stack error
2DF1	Event counter error
2DF2	Transfer register error
2DF3	ALU (2901s) error
2DF4	IREG error
2DF5	Vector priority encoder error
2DF6	SMB error
2DF7	U-bus error
2DF8	Sequencer address register
2DF9	Sequencer AR error

If all the tests are passed, all the bits at memory location 3FE plus bit 0 of memory location 3FF are reset, and the program proceeds to the OCP test.

7.2.3 OCP Test

This routine tests communication between the XMC and the OCP. The following tests are performed in the order indicated:

1. The program attempts to select the OCP for 250ms. If successful, the test continues; if not successful, the test fails.

2. If the OCP is successfully selected in step 1 above, the following tests are performed:

   a. INST-bus parity is checked. If the test is passed, the test continues; if it does not pass, the test fails.
   b. For each of the BUFFER RAM bytes 0-32, the following operations are performed:

      i) The contents are saved.

      ii) The values 15H and 2AH (only the six LSBs are meaningful) are written into each location. Each write operation is verified by a read operation. Each read operation is followed by a CT-bus parity check. If the read and write data match, and parity checks out, the test continues; if not, the test fails.

      iii) The original contents of the memory location under test are restored.

   c. For each of the BUFFER RAM bytes 33-37 and 39, steps i, ii, and iii above are repeated, except the values written into each of those locations are 55H and AAH (all 8 bits are meaningful).

   d. The program deselects the OCP.

   e. The OCP display cursor is set at position 0.

      If all the above tests are passed, bit 1 at SMB location 3FF is reset, indicating that communication with the OCP checks out, and the program proceeds to the HSSM test. This test also indicates that the CT-bus and INST-bus probably pass, subject to further verification.

      If any of the above tests fail, the program branches off to the HSSM test, leaving bit 1 at SMB location 3FF set.

Error Messages. No messages are generated regardless of whether the OCP passes or fails the confidence tests. In case of an OCP failure, no messages will be generated by any subsequent controller confidence tests.

7.2.4 HSSM Test

This routine tests the communication between the XMC and the HSSM boards. The following tasks are performed:

1. The test writes and reads to and from the registers in the XMCIP file register that are accessible to the XMC. The registers accessed are tested as follows:

   The values 55H and AAH are written into each register. Each write operation is verified by a read operation. If read and write data match, the test continues; if not, the test fails.

2. The program writes and reads sequential numbers to and from these registers, beginning with a value of 1, into file register 8.

3. The program checks the parity of the XMC CT-bus, as well as the parity of the HSSM CT-bus and INST-bus.

   If all file register tests are passed, and the parity tests are passed, bit 2 at SMB location 3FF is reset, and the program proceeds to the HSM test. This test also indicates whether the control (CT) and instruction (INST) buses pass, subject to further verification.

   If any of the above tests fail, the program branches to the HSM test, leaving bit 2 at SMB location 3FF set. An appropriate message is generated on the OCP's function/status display. One of the following messages may appear:

   CODE=200 This message indicates that a file register data error was detected on the XMCIP board.

   CODE=201 This message indicates that a CT-bus parity error was detected on the XMC board when data was passed between the XMC and XMCIP boards.

   CODE=202 This message indicates that a CT-bus parity error was detected on the HSSM.

   CODE=203 This message indicates that an INST-bus parity error was detected on the HSSM.

7.2.5 Controller Confidence Test Failure Codes

How to read a failure code table. The failure codes defining a hardware failure consist of three hexadecimal characters. The first (MSB) specifies the subsystem, while the other two specify a failed block within the subsystem.

Subsystem
2HSSM

BLOCK

7.2.6 UBI and HSP Test

These routines test the operation of the UBI and HSP boards.

7.3 7100-30 Power Off Procedure

All circuit breakers for the dual controller and disk drives are located at the front of the cabinet in the AC power box. See figure 7-1 for an illustration of the AC power box within the cabinet.

1. Place the dual controller offline from the CDC system processor.
2. At the OCP keypad, press BYPASS ALL.
3. **BBBBBBBBBBBBBBB PRSNT** should be displayed at the OCP, verifying that all disk drives are in bypass mode.
4. At the disk drive panel, place all drives in write protect mode (that indicator should be illuminated).
5. Power off the disk drives by pressing the PWR switch on the disk drive panel. Allow 30 seconds for the drives to spin down, then turn off the disk drive circuit breakers located in the AC power box.
6. Turn off the circuit breakers located in the AC power box in the following order: drives, CHANNEL B, CHANNEL A, OCP, FANS, and MAIN POWER.

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8. PROBLEM ANALYSIS AND CORRECTION (TROUBLESHOOTING)

This section provides procedures for analyzing and interpreting problems which may occur in the 7100-30.

8.1 Sense Byte Format Interpretation

The sense byte information, both what is transferred to the host and what is available at the thumbwheel display, gives the technician a good understanding of what has transpired in the system if an error has occurred. Introductory information about sense bytes appears below; for detailed sense byte information, see section 8.4.

Sense byte information is separated into two groups:

GROUP A represents error conditions that can exist within the system and that are detectable at the controller/host channel interface level. These are divided into three broad categories:

- o Storage device checks
- o Controller equipment checks
- o Data checks

For these errors, the returned sense byte data can be analyzed and used to determine the failing device(s). Also, the type of failure can be determined along with the required corrective action necessary to return the system to an online status.

GROUP B represents error conditions than can occur in the system, where there is little or no information available at the controller/host channel interface. These are in two basic categories:

- o Channel timeouts
- o Undetected data corruption

8.1.1 Group A Error Conditions

Storage Device Checks. Storage device equipment checks are within the Format 1 Sense error category, as shown in figure 8-4, and can be divided into eight sections as described below.

Format 1	Message 0	NO MESSAGE (see sense bytes 8-23)
Format 1	Message 6	SET CAR ERROR
Format 1	Message 7	SET HAR ERROR
Format 1	Message 9	DRIVE STATUS NOT AS EXPECTED
Format 1	Message A	SEEK ERROR
Format 1	Message C	HSSM SM-INTERRUPT TIMEOUT
Format 1	Message E	UNABLE TO DETERMINE DRIVE TYPE
Format 1	Message F	INITIAL SELECT BUSY TIMEOUT

In addition to the above information, the sense bytes that follow sense byte 7 also contain error information that will assist in determining the failing device(s), as shown in figure 8-4.

Controller Equipment Checks. These checks are in the Format 2 Sense error category, as shown in figure 8-5, and are broken up into two sections as described below.

Format 2	Message 0	EQUIPMENT CHECK
Format 2	Message 5	HSSM U-INTERRUPT TIMEOUT

Most of the error information for Format 2 messages is in the sense bytes following sense byte 7, as shown in figure 8-5. Format 2 sense byte data can be read from the OCP via the thumbwheel display locations 404, 405, 40A through 40C, and 4E8 through 4EB.

Data Checks. Data checks are generally media related, but can also be an indication of a controller or drive problem; for example, a defective head, faulty read/write board, failing memory, or failing ESMD-I/O PCB. The type of error will point to whether there is a media defect or a hardware error in a disk drive or controller. These are described below:

Format 4	Message 1	COUNT ECC UNCORRECTABLE
Format 4	Message 3	DATA ECC UNCORRECTABLE
Format 4	Message 5	HEADER NO SYNC BYTE
Format 4	Message 7	DATA NO SYNC BYTE

Again, sense bytes 8 through 23 contain additional information for these errors, as shown in figure 8-5.

When an error condition occurs, the host operating system requests detailed status and places that information into an error log file. By displaying this information, you can use the format/message decode matrix charts to do a quick analysis to determine in which device the problem is occurring.

The sense byte data can also be read from the controller via the thumbwheel displays. The thumbwheel display locations are listed in the final pages of this section.

8.1.2 Group B Error Conditions

Channel Timeouts. Channel timeouts are generally a result of a failure in communication between the host CPU and the 7100-30. This type of problem will be displayed at the console as a "timeout message."

8.2 Diagnostic Testing

See section 5.4 for information on diagnostic testing.

8.3 Replacing Failing Components

Procedures for replacing a failing component are described in section 10, "Removal and Replacement Procedures."

8.4 Sense Byte Information

Sense information is constructed by the controller whenever unit check status is presented to the I/O channel indicating that an error or unusual condition has occurred on the current command. The sense information is retrieved by issuing a sense I/O command. No unsolicited status is presented for one second following presentation of a unit check unless a sense I/O command is received.

8.4.1 Sense Data Bytes

Twenty-four bytes of sense data are developed by the mass storage system to provide detailed information about error or unusual conditions. (Note that the recovery action field is used for error recovery. Since sense bytes are strictly informational, they are not required for recovery.) Each sense byte contains eight bits to reflect the error or unusual conditions associated with the current command. Figure 8-1 shows this format for the 24 sense bytes.

Sense bytes 0-6	Provide information about error or unusual conditions.
Sense byte 7	Indicates the format of bytes 8-23.
Sense bytes 8-23	Provide detailed information on the type of error or unusual condition.

The interpretation of bytes 8 through 23 varies according to the format presented (in sense byte 7). The sense bytes and formats are described in the following sections.

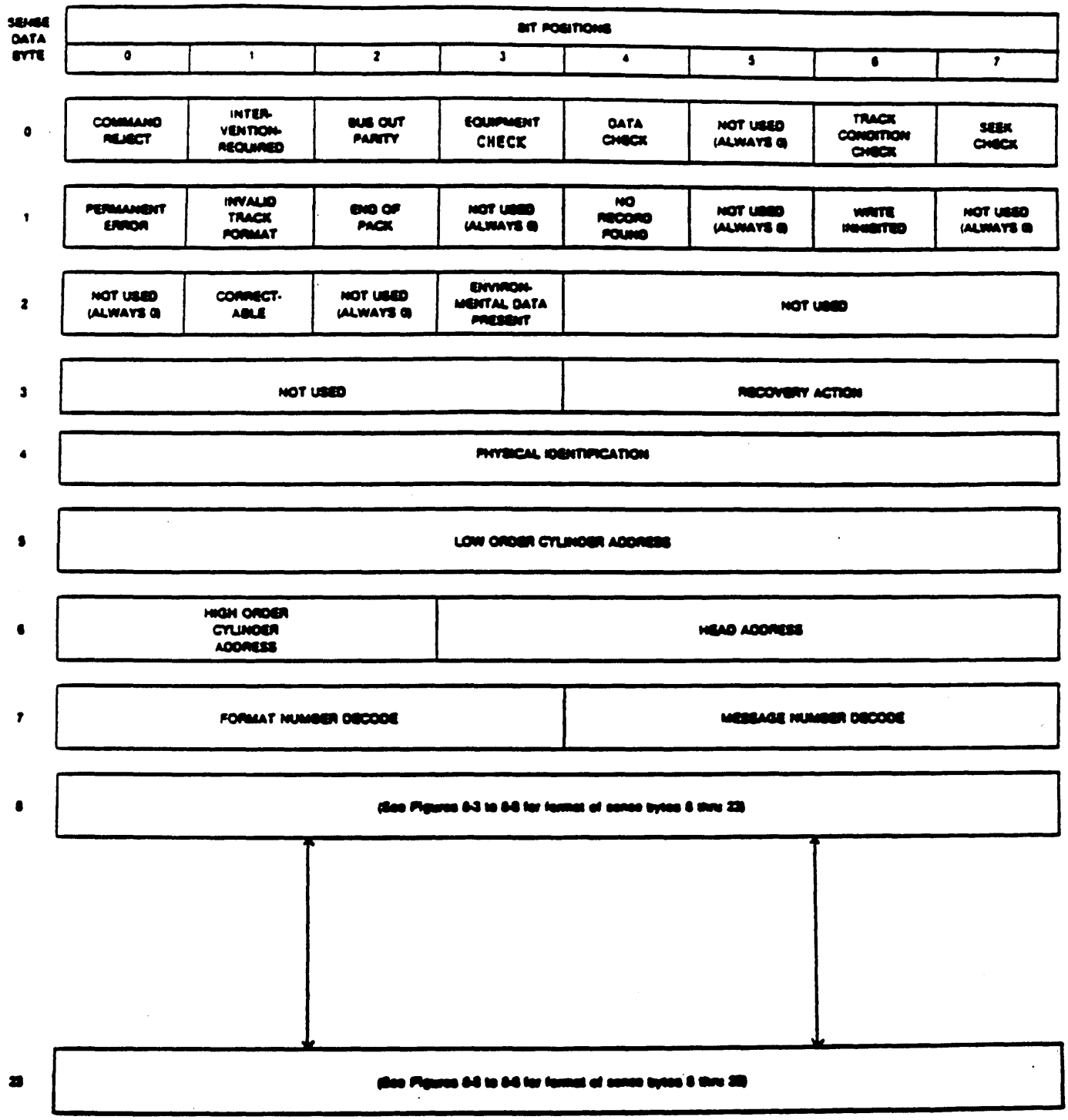


Figure 8-1
Sense Data Bytes Format

8.4.2 Message Number Decode

The message number decode sense bits indicate a message number (hexadecimal). The meaning of each message number depends on the format number. Figure 8-2 shows the format and message number decode and gives the error type.

Format	Description
0	Programming and controller errors
1	Disk drive errors
2	Controller errors
3	Not used
4	ECC uncorrectable data errors
5	ECC correctable data errors
6	Error and usage counts
7	Not used
8	Read configuration
9	Drive error counters
A -> F	Not used

Figure 8-2
Message Number Decode

Format Number
(Hexadecimal)
Decoded by bits 0 through 3 of Sense byte 7

Message number (Hexadecimal) Decoded by bits 4 through 7 of Sense byte 7

	FORMAT 0	FORMAT 1	FORMAT 2	FORMAT 3	FORMAT 4	FORMAT 5	FORMAT 6	FORMAT 8	FORMAT 9
0	NO MESSAGE	NO MESSAGE	NO MESSAGE				ERROR & USAGE COUNTS	CONFIG-URATION	DEVICE ERROR COUNTERS
1	INVALID COMMAND				COUNT ECC UNCOR	COUNT CORR			
2	INVALID SEQUENCE								
3	WORD COUNT LESS THAN REQUIRED				DATA ECC UNCOR	DATA CORR			
4	DATA VALUE NOT AS REQUIRED								
5	INVALID PREP KL = 0 DL > 512		HSSM U-INTERRUPT TIME-OUT		HEADER NO SYNC BYTE				
6	BUSY TO OTHER CHANNEL	SET CAR ERROR							
7	CANNOT SET PREP LENGTH	SET HAR ERROR							
8	WRONG PREP LENGTH				CACHE ECC UNCOR				
9	TERMINA-TION BY FORCED EF	DRIVE STATUS NOT AS EXPECTED							
A	READ LABEL REQUIRED	SEEK ERROR							
B	IMPRO ALTER-NATE TRACK POINTER								
C		HSSM SM-INTERRUPT TIME-OUT							
D									
E		UNABLE TO DETERMINE DRIVE TYPE							
F		INITIAL SELECT BUSY TIME-OUT							

Figure 8-3
Format and Message Number Decode Matrix

8.4.3 Recovery Action Table

The recovery action table, table 8-1, describes the values of bits 18 through 21 of the external interrupt. These values are returned in the EI word as well as in bits 4 through 7 of sense data byte 3.

Table 8-1
Recovery Action Table

Recovery Action	Meaning
1	Write inhibited
2	Seek in progress for another channel, correctable data check, or data check (not permanent)
3	Improper alternate track pointer
4	Command reject (except special cases) or end of pack
5	Read label command required
6	Intervention required
7	Bus out parity error
8	Equipment check
9	Permanent data check
10	Invalid track format or no record found
11	Environmental data present
12	Only valid copy latch set for first record partially updated on write data or write data and pad zeros
13	Only valid copy latch set for last record partially updated on write data

8.4.4 Format 1 Sense

Format 1 sense provides details of storage device errors. Figure 8-4 shows the significance of Format 1 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	NOT USED		SEEK INCOMPLETE	SEEK COMPLETE	ON-LINE	PACK CHANGE	BUSY	NOT USED
9		HSSM TEST FAILURE	ALL ZEROS					
10	ZEROS		ACCESS READY	ZEROS				HEAD LOAD
11	PERMANENT SEEK ERROR AND FAULT	ZEROS						
12	NOT USED		READ ONLY	ZEROS		NO DRIVE CLOCKS	ZEROS	
13	NOT USED		PHYSICAL DRIVE NUMBER					
14	SEEK END	BUSY	SELECTED	WRITE PROTECT	FAULT	SEEK ERROR	ON CYLINDER	READY
15	MODULE SELECT	TAG GATE	ENABLED TAG-VALID CHECK	NOT USED	TAG 8	TAG 4	TAG 2	TAG 1
16	ALL ZEROS							
17	ALL ZEROS							
18	ALL ZEROS							
19	ALL ZEROS							
20	ALL ZEROS							
21	ZEROS		DISK UNIT FAULT	ZEROS		NO DISK UNIT CLOCKS	ZEROS	
22	ALL ZEROS							
23	ALL ZEROS							

Figure 8-4
Format 1--Device Errors

8.4.5 Format 2 Sense

Format 2 sense provides details of controller errors. Figure 8-5 shows the significance of Format 2 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	HAIO 1 PARITY	HAIO 2 PARITY	HAIO 3 PARITY	HAIO 4 PARITY	U-BUS-HAIO PARITY	WMA TEST FAILURE	HOB U-DMA CHECK	UNABLE TO SELECT HAIO
9	ALU FAILURE	HSSM TEST FAILURE	HAIO SEQUENCER ERROR	DIF FIFO CHECK	HOB SM-DMA CHECK	WMA/HSSM TEST FAILURE CODE		
10	U-BUS-XMC PARITY 0-17	U-BUS-XMC PARITY 18-35	CT BUS-XMC PARITY	FRB SEARCH NO FIND	HSSM U-BUS PARITY	SMB-XMC PARITY	HSSM-WMA INST. PARITY	DIF PARITY
11	XRB MEM PARITY	CT-XRB PARITY	XRB INST. PARITY	XRB NOT AVAILABLE	HSSM BUSY TIMEOUT	CT-HSSM PARITY	HSSM INTERNAL PARITY	HSSM BUFFER MEM PARITY
12	XRB INVALID CACHE ADDR.	OCP PARITY	OCP NOT AVAILABLE	WMC SELECT ERROR	WMA PARITY	WMC PARITY	WMA CT-BUS PARITY	WMA U-BUS PARITY
13	NOT USED			DRIVE NUMBER				
14	SEEK END	BUSY	SELECTED	WRITE PROTECT	FAULT	SEEK ERROR	ON CYLINDER	READY
15	MODULE SELECT	TAG GATE	ENABLE TAG-VALID CHECK	NOT USED	TAG 8	TAG 4	TAG 2	TAG 1
16	ZERO	READ DATA TRANSFER	ZEROS		WRITE DATA TRANSFER	ZERO	READ HEADERS	READ VERIFY
17	ALL ZEROS							
18	ALL ZEROS							
19	ALL ZEROS							
20	ALL ZEROS							
21	ZEROS		DISK UNIT FAULT	ZEROS		NO DISK UNIT CLOCKS	ZERO	WMA ADDRESS CHECK
22	ALL ZEROS							
23	ALL ZEROS							

Figure 8-5
Format 2--Controller Errors

8.4.6 Format 4 Sense

Format 4 sense provides details of ECC uncorrectable data errors on disk drives. Figure 8-6 shows the significance of Format 4 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	CYLINDER HIGH ORDER BYTE							
9	CYLINDER LOW ORDER BYTE							
10	ALL ZEROS							
11	ZEROS				AMPERIF HEAD NO.			
12	ZERO	RECORD NO.						
13	ALL ZEROS							
14	ALL ZEROS							
15	ZEROS						ERROR RECOVERY RETRY COUNT	
16	STRING NO. 00 = Units 0-7 01 = Units 8-15 10 = Units 16-23 11 = Units 24-31		DISK UNIT NO. (COMPLEMENTED)				DISK UNIT NO.	
17	ALL ZEROS							
18	ALL ZEROS							
19	ALL ZEROS							
20	ALL ZEROS							
21	ALL ZEROS							
22	ALL ZEROS							
23	ALL ZEROS							

Figure 8-6
Format 4--ECC Uncorrectable

8.4.7 Format 5 Sense

Format 5 sense is not used in the 7100-30.

8.4.8 Format 6 Sense

Format 6 sense is not used in the 7100-30.

8.4.9 Format 8 Sense

Format 8 sense is not used in the 7100-30.

8.4.10 Thumbwheel Display Locations

The following pages contain thumbwheel setting information for other systems as well as the 7100-30. Therefore, you will see references to items (cache, for example) which are not part of the 7100-30. In these cases, refer to the items which are part of the 7100-30 and ignore any others.

The DISPLAY/SELECT thumbwheel switches, located at the upper right of the OCP, are used in conjunction with the operations/maintenance data display. The thumbwheel switch setting selected determines the data which is displayed at the operations/maintenance data display. This display is used for diagnostic purposes.

The thumbwheel settings are as follows:

000-3FF MDBP memory data, using a single 36-bit word format

400-555 XMC scratchpad memory data, using three 12-bit characters as a format

E00-EFF XMC microcode address

Display settings between 400 and 555 are listed below; the sense byte data described earlier in this section may be read from these displays. For each of these descriptions, only those bits which are used are displayed; if a bit does not appear in the display location description, then it is not being used.

THUMBWHEEL DISPLAY LOCATION 400: Channel Sense Bytes

```
|           |           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 00 ----------|---------- Sense Byte 01 ----------|----- Sense Byte 02 -----|
```

Bit	Bit	Bit
31 - Command Reject	19 - Permanent Error	06 - Correctable ECC
30 - Intervention Required	18 - Invalid Track Format	04 - Env. Data Present
29 - Bus Out Parity	17 - End of Pack	
28 - Equipment Check	15 - No Record Found	
27 - Data Check	13 - Write Inhibited	
25 - Track Condition Check		
24 - Seek Check		

THUMBWHEEL DISPLAY LOCATION 401: Channel Sense Bytes

```
|           |           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 03 ----------|---------- Sense Byte 04 ----------|----- Sense Byte 05------|
          Recovery Action                    Physical Drive ID              Emulated Cylinder LSBs
```

Recovery Action
0 - No Error
1 - Write Inhibited
2 - Data Check (Correctable)
3 - Bad Track Pointer
4 - Command Reject
5 - Read Label Required
6 - Intervention Required
7 - Bus Out Parity
8 - Equipment Check
9 - Permanent Data Check
A - No Record Found
B - Env. Data Present
C - Only Valid Copy First
D - Only Valid Copy Last

Bits 19	Bits 18:	Drive Group
0	0	Drives 0-7
0	1	Drives 8-15
1	0	Drives 16-23
1	1	Drives 24-31

Drive Number

	Complemented			Actual		
Bit:	17	16	15	14	13	12
Unit						
0	1	1	1	0	0	0
1	1	1	0	0	0	1
2	1	0	1	0	1	0
3	1	0	0	0	1	1
4	0	1	1	1	0	0
5	0	1	0	1	0	1
6	0	0	1	1	1	0
7	0	0	0	1	1	1

THUMBWHEEL DISPLAY LOCATION 402: Channel Sense Bytes

```
|        |        |        |        |        |        |        |        |        |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 06 ----------|---------- Sense Byte 07 ----------|----- Sense Byte 08 -----|
|        |        |                 |          | Format  | Message |          Format 1
  Emulated Emulated Head              Format    Message
  Cyl.MSBs Number                   Decode    Decode
                                  (Format/Message Decoder - See Figure 8-2)
```

Bit	Bit
05 - Seek Incomplete	02 - Pack Change
04 - Seek Complete	01 - Busy
03 - Online	

THUMBWHEEL DISPLAY LOCATION 403: Channel Sense Bytes

```
|        |        |        |        |        |        |        |        |        |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 09, Format 1 -----|----- Sense Byte 10, Format 1 -----|-Sense Byte 11, Format 1-|
```

Bit	Bit	Bit
30 - HSSM Test Failure	17 - Access Ready	07 - Permanent Seek Error/Fault
	12 - Head Load	

THUMBWHEEL DISPLAY LOCATION 404: Channel Sense Bytes

```
|        |        |        |        |        |        |        |        |        |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 12, Format 1 -----|----- Sense Byte 13, Format 1 -----|Sense Byte 14, Format 1,2|
                                      Physical Drive #                    Current Drive Status
```

Bit	Bit	Bit
29 - Read Only	07 - Seek End	03 - Fault
26 - No Drive Clocks	06 - Busy	02 - Seek Error
	05 - Selected	01 - On Cylinder
	04 - Write Protected	00 - Ready

THUMBWHEEL DISPLAY LOCATION 405: Channel Sense Bytes

```
|        |        |        |        |        |        |        |        |        |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---- Sense Byte 15, Format 1,2 ----|---- Sense Byte 21, Format 1,2 ----|Sense Byte 8, Format 4,5 |
                                                                         Actual Cyl. MSBs
```

Bit	Bit	Bit
31 - Mod. Select	27 - Tag 8	17 - Drive Fault
30 - Tag Gate	26 - Tag 4	13 - Write Inhibit
29 - Valid Check	25 - Tag 2	
28 - Enable Tag	24 - Tag 1	

THUMBWHEEL DISPLAY LOCATIONS 406 through 409: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Display Location								
406	Sense Byte 9, Format 4,5 Actual Cyl. LSBs		Sense Byte 10, Format 4,5			Sense Byte 11, Format 4,5 Actual Head #		
407	Sense Byte 12, Format 4,5 Actual Record		Sense Byte 13, Format 4,5			Sense Byte 14, Format 4,5		
408	Sense Byte 15, Format 4 SM Error Retry Count		Sense Byte 16, Format 4 See Sense Byte 4 breakdown			Sense Byte 15, Format 5		
409	Sense Byte 16, Format 5 Record Length MSB		Sense Byte 17, Format 5 Record Length LSB			Sense Byte 21, Format 5 ECC Correction MSB		

THUMBWHEEL DISPLAY LOCATION 40A: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 22, Frmt 5 ECC Correction LSBs			Sense Byte 21, Format 6			Sense Byte 8, Format 2		

Bit		Bit	
07	HAIO Parity Error 1	03	HAIO Detected U Bus Parity Error
06	HAIO Parity Error 2	02	WMA Test Failure (See Display Location 408)
05	HAIO Parity Error 3	01	MDB U-DMA Check
04	HAIO Parity Error 4	00	Unable to Select HAIO

THUMBWHEEL DISPLAY LOCATION 408: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 9, Format 2			Sense Byte 10, Format 2			Sense Byte 11, Format 2		

Bit		Bit		Bit	
31	ALU Failure	19	XMCP Detected U Bus PE (0-17)	07	XRB Memory PE
30	HSSM Test Failure	18	XMCP Detected U Bus PE (18-35)	06	XRB Detected CT Bus PE
29	HAIO Sequencer Error	17	XMCP Detected CT Bus PE	05	XRB Inst. PE
28	DIFP FIFO Check	16	XRB No Find	04	XRB Not Available
27	MDBP SM-DMA Check	15	HSSM Detected U Bus PE	03	HSSM Busy Timeout
26	WMA/HSSM Test Failure Code*	14	SMB to XMCP PE	02	HSSM Detected CT Bus PE
25		13	HSSM/WMA Inst. PE	01	HSSM Internal PE
24		12	DIFP PE	00	HSSM Buffer Memory PE

* If Display Location 40A bit 2=1, use WMA Test Failure Codes; not applicable to the 7100-30.
If Display Location 408 bit 30=1, use HSSM Test Failure Codes.

HSSM Test Failure Code

0 - See other bytes
1 - Word-to-byte miscompare
2 - Byte-to-word miscompare
3 - DMA failure (early complete)
4 - U-side DMA failure (no complete)
5 - Header flag miscompare
6 - ODR or IDR tag missing
7 - Undefined error

THUMBWHEEL DISPLAY LOCATION 40C: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0

Sense Byte 12, Format 2	Sense Byte 16, Format 2	Next Cylinder

Bit	Bit	Bit
31 - XRB Invalid Data or Address	27 - WMAP PE	18 - Read Data Transfer
30 - OCP PE	26 - WMCM PE	15 - Write Data Transfer
29 - OCP Not Available	25 - WMAP CT-Bus PE	13 - Read Header
28 - WMC Select Error	24 - WMAP U-Bus PE	12 - Read Verify

THUMBWHEEL DISPLAY LOCATION 40D

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0

Next Head	Next Record	Relative Record No.

THUMBWHEEL DISPLAY LOCATION 40E

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0

RSSave	Starting Word No.	Seek Error Retry Count

THUMBWHEEL DISPLAY LOCATION 40F

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0

E.F.Allowed Mask, MAIO #:4--3--2--1	Last EI on MAIO #:----4--3--2--1	Attention MAIO #:-4-3-2-1

THUMBWHEEL DISPLAY LOCATIONS 410 through 41A

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Current Drive Cylinder (see below)	Current Drive Cylinder (see below)	Current Drive Cylinder (see below)

Display Location			
410	00	01	02
411	03	04	05
412	06	07	08
413	09	10	11
414	12	13	14
415	15	16	17
416	18	19	20
417	21	22	23
418	24	24	26
419	27	28	29
41A	30	31	(Spare)

THUMBWHEEL DISPLAY LOCATIONS 418 through 421

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
0 0	31 ..... Bit Position = Logical Drive #							0

Display Location	
418	Seek Complete Pending Mask
41C	Seek Complete Pending this Drive
41D	Seek Complete Pending on HAIO-1
41E	Seek Complete Pending on HAIO-2
41F	Seek Complete Pending on HAIO-3
420	Seek Complete Pending on HAIO-4
421	Seek Complete Pending for an ILD Drive

THUMBWHEEL DISPLAY LOCATIONS 422 through 424

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sector Timer for Drives (see below)			Sector Timer for Drives (see below)			Sector Timer for Drives (see below)		

Display Location			
422	0,8,16,24	1,9,17,25	2,10,18,26
423	3,11,19,27	4,12,20,28	5,13,21,29
424	6,14,22,30	7,15,23,31	Not Used

THUMBWHEEL DISPLAY LOCATIONS 425 through 430

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|
|                                   |                       |
|0 ------- 0|31---------------------- Bit Position = Logical Drive # ----------------------0|
```

Display Location	
425	Bit for the ILD Drive
426	Attention Pending to HAIO-1
427	Attention Pending HAIO-1 Mask
428	Attention Pending to HAIO-2
429	Attention Pending HAIO-2 Mask
42A	Attention Pending to HAIO-3
42B	Attention Pending HAIO-3 Mask
42C	Attention Pending to HAIO-4
42D	Attention Pending HAIO-4 Mask
42E	Bit for the Current Drive (only one bit at a time can be set)
42F	Bit for Seek Error While Polling (one bit per drive)
430	Error/Usage Log Flow (one bit per drive)

THUMBWHEEL DISPLAY LOCATIONS 431, 432, 434 and 435

```
|                                   |           |           |           |           |           |
|35 34 33 32 31 30 29 28 27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8 7 6|5 4 3 2 1 0|

|------------ Cylinder ------------|--Head Number-|--- Record Number --|-Error Count-|- Physical-|
                                                                                    Drive No.
```

Display Locations:

431: Correctable ECC Error - History #1
432: Correctable ECC Display - History #2
434: Uncorrectable ECC Display - History #1
435: Uncorrectable ECC Display - History #2

THUMBWHEEL DISPLAY LOCATIONS 433 and 436

```
|                                   |                                                       |
|35 34 33 32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0|

|0 ------------------------------ 0|------------- ECC Error Count For All Drives --------------|
```

Display Locations:

433: Count of Correctable ECC Errors
436: Count of Uncorrectable ECC Errors

THUMBWHEEL DISPLAY LOCATION 437: ECC Correction Pattern

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|........R 5-Upper-Temp. Save ......|.. XMC Parity Error Retry Count ...|--ECC Error Correction--|
                                                                        Pattern
```

THUMBWHEEL DISPLAY LOCATION 438

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|--SM Error Return Location (MSBs)--|0....................0|--- Initial Read Transfer Length ----|
```

THUMBWHEEL DISPLAY LOCATION 439

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|--SM Error Return Location (LSBs)--|----------------Record Byte Address (Write)----------------|
```

THUMBWHEEL DISPLAY LOCATION 43A

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|........ Pad Zeros Length .........|....... Alternate Cylinder .........|----------Alt. Head------|
        (Write Data and Pad Zeros Function)
```

THUMBWHEEL DISPLAY LOCATION 438 - 43D: ILD Displays

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|
```

Display Location

438 Main ILD Display: variable depending on state of ILD

```
43C ....... Drive Number ...........| ......... Current Cylinder .......|----- Current Head ------|
43D ........ (Not Used) ............| ........ Starting Cylinder .......|---- Ending Cylinder ----|
```

THUMBWHEEL DISPLAY LOCATION 43E: ILD Display

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17	16 15 14 13 12	11 10 9 8 7 6 5	4 3 2 1 0
ILD Flags		Starting Head		Ending Head

Bit		Bit	
35	Online Format Defective	29	Last Operation
34	Format Defective	28	Format-to-Verify
33	Defective Alternate	27	Seek Initiated
32	Alt. Cyl/Reverse Seek Flag	26	ILD Running
31	Power Fail Timer Running	25	Seek Comp. Pending
30	Data Copy/Restore Running	24	ILD Active

THUMBWHEEL DISPLAY LOCATION 43F

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
ILD Test No				ILD Return from Wait Loop				

THUMBWHEEL DISPLAY LOCATIONS 440-49F: Drives 0-31 Error/Usage Log

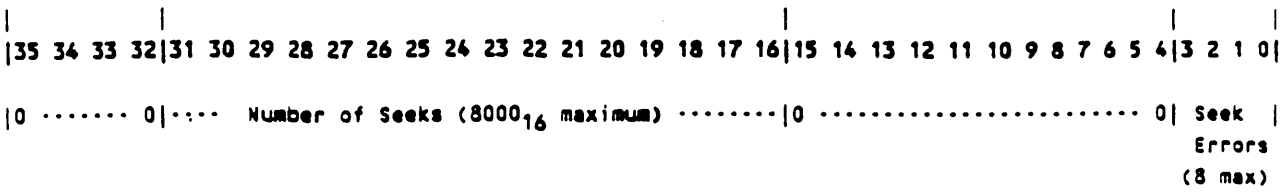
35 34 33 32	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 ... 0	Error/Usage Log Bytes Read This Drive ($80,000,000_{16}$ maximum)

Drive	Display	Drive	Display	Drive	Display	Drive	Display	Drive	Display
0	440	7	455	13	467	19	479	25	488
1	443	8	458	14	46A	20	47C	26	48E
2	446	9	45B	15	46D	21	47F	27	491
3	449	10	45E	16	470	22	482	28	494
4	44C	11	461	17	473	23	485	29	497
5	44F	12	464	18	476	24	488	30	49A
6	452							31	490

35 34 33 32 31 30 29 28	27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
0 ... 0	Correctable ECC (200_{16} maximum)	0 ... 0	Uncorrectable ECC Errors (40_{16} maximum)

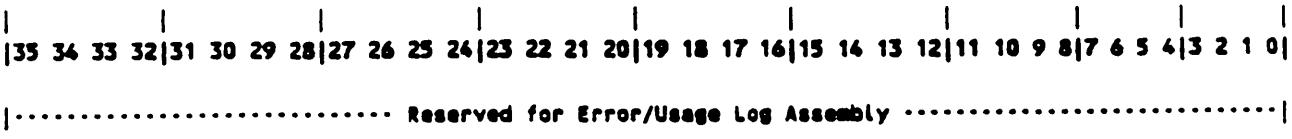
Drive	Display	Drive	Display	Drive	Display	Drive	Display	Drive	Display
0	441	7	456	13	468	19	47A	25	48C
1	444	8	459	14	46B	20	47D	26	48F
2	447	9	45C	15	46E	21	480	27	492
3	44A	10	45F	16	471	22	483	28	495
4	44D	11	462	17	474	23	486	29	498
5	450	12	465	18	477	24	489	30	49B
6	453							31	49E

THUMBWHEEL DISPLAY LOCATIONS 440-49F: Drives 0-31 Error/Usage Log (continued)

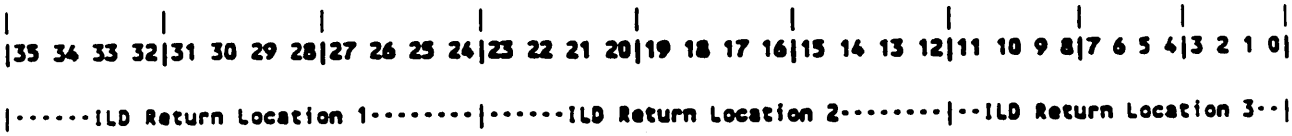


Drive	Display	Drive	Display	Drive	Display	Drive	Display	Drive	Display
0	442	7	457	13	467	19	478	25	480
1	445	8	45A	14	46A	20	47E	26	490
2	448	9	450	15	460	21	481	27	493
3	44B	10	460	16	470	22	484	28	496
4	44E	11	463	17	473	23	487	29	499
5	451	12	466	18	476	24	48A	30	49C
6	454							31	49F

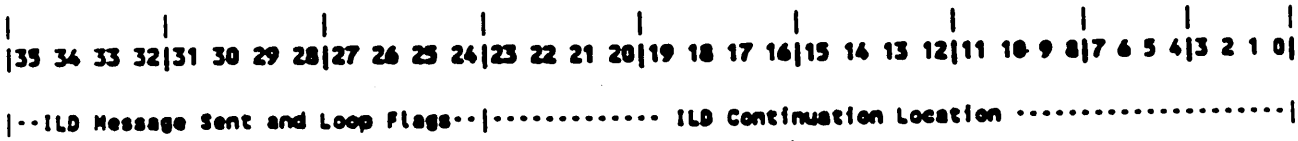
THUMBWHEEL DISPLAY LOCATION 4A0-4A3



THUMBWHEEL DISPLAY LOCATION 4A4



THUMBWHEEL DISPLAY LOCATION 4A5



THUMBWHEEL DISPLAY LOCATIONS 4A6 THROUGH 4AF

Display Location	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
4A6	R14 Temporary Save	R15 Upper Temporary Save	R15 Lower Temporary Save	
4A7	ILD OCP Command[1]	ILD/OCP Parameter 1	ILD/OCP Parameter 2	
4A8	ILD Return 1 MSB	ILD Return 2 MSB	ILD Return 3 MSB	
4A9	..... Wait Loop Pass Counter		Random Seek Seed Word	
4AA	ILD Next Cylinder Save	ILD Next Head Save	R5 Temporary Save	
4AB	Not Used	Cache Read Drive Number	Drive No. for Pushed Track	
4AC	Cache Operating Status Flags[2]	Last Drive Selected	MOB U-Side Relative Record Number	
4AD	XRB Error Call to FRB Hand	No. of Tracks Unable to Write Back	Backscan Hold Off Counter (Primary)	
4AE	ILD Max Usable Cylinder	..... Count of Pushed-Off Tracks		
4AF	ILD Max Head	..... Count of Backscan Tracks Written		

[1] ILD OCP Command information appears below:

Octal Command	Description	Parameter 1	Parameter 2
01	Print Message	Message Number	
02	Reset Clock Interrupt		
03	Load Hit Ratio	Drive (0-31)	1 = Hit; 0 = Miss
04	Reset State Change Interrupt		
85	Wait for "YES/NO"	0 = no; 1 = yes	
86	Enter number (hex)	No. of Digits Data Max	
87	Enter number (decimal)	No. of Digits Data Max	
08	Print Hex Number	Data	No. of Digits to Print
09	Print Decimal Number	Data	No. of Digits to Print
0A	Set Cursor Position	Position (0-39)	
0B	Store Current Message		
0C	Reset Interrupts & State Change Requests		
8E	Enter number (0-F) and Print Alternate Message	Message Number	
0F	Clear Message Buffers		
10	Initiate Timer	No. of Seconds	
11	Reset Timer Done Flag		

[2] 4AC Cache Operating Status Flags: Bit 27 = Force down all
Bit 26 = Force Bypass all
Bit 25 = XRB down
Bit 24 = Seek only

THUMBWHEEL DISPLAY LOCATIONS 480: ILD Sense Bytes

```
|          |          |          |          |          |          |          |          |          |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 00 ----------|---------- Sense Byte 01 ----------|----- Sense Byte 02 -----|
```

Bit	Bit	Bit
31 · Command Reject	19 · Permanent Error	06 · Correctable ECC
30 · Intervention Required	18 · Invalid Track Format	04 · Env. Data Present
29 · Bus Out Parity	17 · End of Pack	
28 · Equipment Check	15 · No Record Found	
27 · Data Check	13 · Write Inhibited	
25 · Track Condition Check		
24 · Seek Check		

THUMBWHEEL DISPLAY LOCATION 481: ILD Sense Bytes

```
|          |          |          |          |          |          |          |          |          |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 03 ----------|---------- Sense Byte 04 ----------|----- Sense Byte 05------|
          Recovery Action                    Physical Drive ID                Emulated Cylinder LSBs
```

Recovery Action
0 · No Error
1 · Write Inhibited
2 · Data Check (Correctable)
3 · Bad Track Pointer
4 · Command Reject
5 · Read Label Required
6 · Intervention Required
7 · Bus Out Parity
8 · Equipment Check
9 · Permanent Data Check
A · No Record Found
B · Env. Data Present
C · Only Valid Copy First
D · Only Valid Copy Last

Bits 19	Bits 18:	Drive Group
0	0	Drives 0-7
0	1	Drives 8-15
1	0	Drives 16-23
1	1	Drives 24-31

Drive Number

	Complemented			Actual		
Bit:	17	16	15	14	13	12
Unit						
0	1	1	1	0	0	0
1	1	1	0	0	0	1
2	1	0	1	0	1	0
3	1	0	0	0	1	1
4	0	1	1	1	0	0
5	0	1	0	1	0	1
6	0	0	1	1	1	0
7	0	0	0	1	1	1

THUMBWHEEL DISPLAY LOCATION 482: ILD Sense Bytes (if ILD Error)

```
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 06 ----------|---------- Sense Byte 07 ----------|----- Sense Byte 08 -----|
                                     |  Format  |  Message  |              Format 1
 Emulated  Emulated Head             |  Decode  |  Decode   |
 Cyl.MSBs      Number                |(Format/Message Decode - See Figure 8-2)
```

Bit	Bit
05 - Seek Incomplete	02 - Pack Change
04 - Seek Complete	01 - Busy
03 - Online	

THUMBWHEEL DISPLAY LOCATION 483: ILD Sense Bytes (if ILD Error)

```
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 09, Format 1 -----|----- Sense Byte 10, Format 1 -----|-Sense Byte 11, Format 1-|
                                                                          Drive Status at Error Time
```

Bit	Bit	Bit
30 - HSSM Test Failure	17 - Access Ready	07 - Permanent Seek Error/Fault
	12 - Head Load	

THUMBWHEEL DISPLAY LOCATION 484: ILD Sense Bytes (if ILD Error)

```
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 12, Format 1 -----|----- Sense Byte 13, Format 1 -----|Sense Byte 14, Format 1,2|
                                      Physical Drive #
```

Bit	Bit	Bit
29 - Read Only	07 - Seek End	03 - Fault
26 - No Drive Clocks	06 - Busy	02 - Seek Error
	05 - Selected	01 - On Cylinder
	04 - Write Protected	00 - Ready

THUMBWHEEL DISPLAY LOCATION 485: ILD Sense Bytes (if ILD Error)

```
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---- Sense Byte 15, Format 1,2 ----|---- Sense Byte 21, Format 1,2 ----|Sense Byte 8, Format 4,5 |
                                                                          Actual Cyl. MSBs
```

Bit	Bit	Bit
31 - Mod. Select	27 - Tag 8	17 - Drive Fault
30 - Tag Gate	26 - Tag 4	13 - Write Inhibit
29 - Valid Check	25 - Tag 2	
28 - Enable Tag	24 - Tag 1	

THUMBWHEEL DISPLAY LOCATIONS 486 through 489: ILD Sense Bytes (if ILD Error)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0

Display Location			
486	Sense Byte 9, Format 4,5 Actual Cyl. LSBs	Sense Byte 10, Format 4,5	Sense Byte 11, Format 4,5 Actual Head #
487	Sense Byte 12, Format 4,5 Actual Record	Sense Byte 13, Format 4,5	Sense Byte 14, Format 4,5
488	Sense Byte 15, Format 4 SM Error Retry Count	Sense Byte 16, Format 4 See Sense Byte 4 breakdown	Sense Byte 15, Format 5
489	Sense Byte 16, Format 5 Record Length MSB	Sense Byte 17, Format 5 Record Length LSB	Sense Byte 21, Format 5 ECC Correction MSB

THUMBWHEEL DISPLAY LOCATION 48A: ILD Sense Bytes (if ILD Error)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 22, Frmt 5 ECC Correction LSBs			Sense Byte 21, Format 6			Sense Byte 8, Format 2		

Bit		Bit	
07	HAIO Parity Error 1	03	U Bus -- HAIO Parity
06	HAIO Parity Error 2	02	WMA Test Failure (See Display Location 488)
05	HAIO Parity Error 3	01	MDB U-DMA Check
04	HAIO Parity Error 4	00	Unable to Select HAIO

THUMBWHEEL DISPLAY LOCATION 488: ILD Sense Bytes (if ILD Error)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 9, Format 2			Sense Byte 10, Format 2			Sense Byte 11, Format 2		

Bit		Bit		Bit	
31	ALU Failure	19	XMCP Detected U Bus PE (0-17)	07	XRB Memory PE
30	HSSM Test Failure	18	XMCP Detected U Bus PE (18-35)	06	XRB Detected CT Bus PE
29	HAIO Sequencer Error	17	XMCP Detected CT Bus PE	05	XRB Inst. PE
28	DIFP FIFO Check	16	XRB No Find	04	XRB Not Available
27	MDBP SM-DMA Check	15	HSSM Detected U Bus PE	03	HSSM Busy Timeout
26		14	SMB to XMCP PE	02	HSSM Detected CT Bus PE
25	WMA/HSSM Test	13	HSSM/WMA Inst. PE	01	HSSM Internal PE
24	Failure Code*	12	DIFP PE	00	HSSM Buffer Memory PE

* If Display Location 48A bit 2=1, use WMA Test Failure Codes; not applicable to the 7100-30.
If Display Location 488 bit 30=1, use HSSM Test Failure Codes.

HSSM Test Failure Code

0 - See other bytes
1 - Word-to-byte miscompare
2 - Byte-to-word miscompare
3 - DMA failure (early complete)
4 - U-side DMA failure (no complete)
5 - Header flag miscompare
6 - ODR or IDR tag missing
7 - Undefined error

THUMBWHEEL DISPLAY LOCATION 48C: ILD Sense Bytes (if ILD Error)

35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
3	2	1	0												
·····Sense Byte 12, Format 2·····								·····Sense Byte 16, Format 2·····							
·····Next Cylinder·····															

Bit		Bit		Bit	
31	XRB Invalid Cache Address	27	WMAP PE	18	Read Data Transfer
30	OCP PE	26	WMCM PE	15	Write Data Transfer
29	OCP Not Available	25	WMAP CT-Bus PE	13	Read Header
28	WMC Select Error	24	WMAP U-Bus PE	12	Read Verify

THUMBWHEEL DISPLAY LOCATIONS 48D - 48F

35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4
3	2	1	0												

Display Locations			
48D	Pushed-Off Track Upper Address	Pushed-Off Track Lower Address	Seek-Only Flag
48E	ILD Next Record Save	ILD Return 4 MSB	ILD Return 4 LSB
48F	····· R5 Save If ILD Error ·····		ILD Error Retry Count

THUMBWHEEL DISPLAY LOCATIONS 4C0 through 4CF

Display Locations	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
4C0	---------- READ1TRK & WRIT1TRK Main Return Location ----------			Caching Status[1]
4C1	---------- Caching Read/Write Return Location ----------			ILD Max Drive Cylinder
4C2	Save Cylinder Before Caching		Save Head Before Caching	Save Starting Word Before Caching
4C3	R15 Save RD & WR 1TRK	---------- Save Transfer Length Before Caching ----------		
4C4	Seek Started Flag		Save Record Before Caching	Caching Retry Counter
4C5	---------- R14 Save Before Caching ----------			Not Used
4C6	Save Cache Cylinder Before Caching		Save Cache Unit/Head Before Caching	Save Cache Track Number Before Caching
4C7	WMA ECC Status[2]		Save Cylinder for Track to Cache	Save Unit/Head for Track to Cache
4C8	Emulated Cylinder Save LSB		Emulated Cylinder (MSB) and Head Save	Emulated Record Save
4C9	WAITSEEK Return Location MSBs	---------- Initial Cache/SSS Address ----------		
4CA	Saved Emulated Record Number		RIO Temporary Save	OCP Command[3]
4CB	Requested Unit (State Change)		Requested State (State Change)	Present State
4CC	1/8 Cache Disk Lowest Address(MSB) ----------	Command Relative Address ----------		
4CD	Not Used	---------- Saved Next U-Start Address ----------		
4CE	---------- Format & Cache Prep Date ----------			
4CF	---------- Data Miscompare Bad Data ----------			

[1] 4C0 Caching Status
Bit 6 Caching Error
Bit 5 WMA ECC Error
Bit 4 Push Off Track
Bit 3 Intermediate Bypass Track
Bit 2 Write-Through
Bit 1 Cache to/from HAIO
Bit 0 Caching Mode

[2] 4C7 WMA ECC Status
Bit 1: ECC Uncorrectable
Bit 0: ECC Two-bit Correctable

[3] 4CA OCP Command: See breakdown for Display Location 4A7

THUMBWHEEL DISPLAY LOCATION 400 - 406: External Functions

	35	34 33 32 31 30 29	28 27 26 25 24	23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	1	0----------	0	--Disk Unit---	- Command Code---	0 0 --------Word Transfer Length -------- OR Backing Factor

THUMBWHEEL DISPLAY LOCATION 407: Total E.F. Count (Reset by sub-system clear)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Count of External Function Commands								

THUMBWHEEL DISPLAY LOCATION 408 - 40E: Relative Word Address

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18	17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
0	0	Relative Word Address				
		OR				
	Cylinder (Absolute Address)			0	0 Head	(See Note)

Note: Normally zero except: Seek and Set Sector = Sector Number
Space Count and Read Data = Record Number

THUMBWHEEL DISPLAY LOCATION 4E0 - 4E6: Last External Interrupt Words

35 34 33 32	31	30	29 28 27 26	25 24 23 22	21 20 19 18	17 16	15 14 13 12 11 10 9 8	7 6 5	4 3 2 1 0
0 ... 0 If all ones = EI Time Out	CT *	0	Status - Action (see below)	0 ... 0	Recovery - Action (see Display Location 401, bits 24-35)	0 - 0	Device Status (see below)	0 0 0	Drive No.

*CT = Channel Truncation

Status Action Codes		Status Action Codes		Device Status
0	Invalid Code	7	Sense Completed	15 - Attention
1	Pack Change	8	Sense I/O Completed	14 - Status Modifier
2	Read Label Command	9	C.T. on Sense Command	13 - Control Unit End
3	EF/EI Collision	A	Channel Truncation	12 - Busy
4	Seek Initiated	B	Acquire Sense Bytes for Unit Check	11 - Channel End
5	Seek Completed	D	Bus Out Parity Error	10 - Device End
6	Read or Write Completed	E	Correctable Data Check	9 - Unit Check
		F	Forced EF Termination	8 - Unit Exception (Not Used)

THUMBWHEEL DISPLAY LOCATION 4E7

35	34 33 32 31 30 29 28 27	26	25 24 23 22 21 20 19 18	17	16 15 14 13 12 11 10 9	8	7 6 5 4 3 2 1 0
0 ... 0	31	Drives on Cylinder					0

Bit Position Equals Logical Drive Number

THUMBWHEEL DISPLAY LOCATION 4E8: Last Channel Sense Bytes

```
|  |                        |  |                        |  |                        | |              |
|35|34 33 32 31 30 29 28 27|26|25 24 23 22 21 20 19 18|17|16 15 14 13 12 11 10 9|8|7 6 5 4 3 2 1 0|

|0 |···· Sense Byte 0 ·····| 0|···· Sense Byte 1 ·····| 0|··· Sense Byte 2 ·····|0|  Sense Byte 3 |
```

Bit	Bit	Bit
34 - Command Reject	28 - Track Cond. Check	21 - No Record Found
33 - Intervention Required	27 - Seek Check	19 - Write Inhibited
32 - Bus Out Parity	25 - Permanent Error	15 - Correctable Data Check
31 - Equipment Check	24 - Invalid Track Format	13 - Environ. Data Present
30 - Data Check	23 - End of Pack	3-0- Recovery Action[1]

[1]Same as Display Location 401, bits 24-35.

THUMBWHEEL DISPLAY LOCATION 4E9: Last Channel Sense Bytes

```
|  |                        |  |                        |  |                        | |              |
|35|34 33 32 31 30 29 28 27|26|25 24 23 22 21 20 19 18|17|16 15 14 13 12 11 10 9|8|7 6 5 4 3 2 1 0|

|0 |···· Sense Byte 4 ·····| 0|···· Sense Byte 5 ·····| 0|··· Sense Byte 6 ·····|0|  Sense Byte 7 |
                             Emulated Cyl. LSB
```

Bit	Bit	Bit
34-33 - String Number	32-30 Drive # (Complemented)	7-4 Format Decode[2]
00 = Drives 0-7	29-27 Drive #	3-0 Message Decode
01 = Drives 8-15	16-14 Emulated Cyl. 3 MSB	
10 = Drives 16-23	13-9 Emulated Head	[2] The format decode determines
11 = Drives 24-31		the meaning of sense bytes 18-23.

THUMBWHEEL DISPLAY LOCATIONS 4EA, B, C, and D: Last Channel Sense Bytes

```
|  |                        |  |                        |  |                        | |              |
|35|34 33 32 31 30 29 28 27|26|25 24 23 22 21 20 19 18|17|16 15 14 13 12 11 10 9|8|7 6 5 4 3 2 1 0|

|0 |···· Sense Byte ·····|0 |····· Sense Byte ·····|0 |····· Sense Byte ····|0|··Sense Byte ··|
|      (see # below)          (see # below)             (see # below)       (see below)
```

Display Location				
4EA	8	9	10	11
4EB	12	13	14	15
4EC	16	17	18	19
4ED	20	21	22	23

THUMBWHEEL DISPLAY LOCATIONS 4EE through 4FF

Display Locations	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
4EE	Max Emulated Cylinder	Max Emulated Head	Max Emulated Record	
4EF	Record Length	1/4 Emulated Head Multiplier	1/4 HSSM Buffer Capacity	
4F0	Max Record Number in MDB	1/4 Emulated Cylinder Divisor		
4F1	Max Actual Usable Cylinder	Max Actual Cylinder	Max Actual Head	
4F2	Max Actual Record	1/4 Actual Cylinder Divisor		
4F3	1/4 Words Per Track	1/4 Max Words Per Track	Records Read/Written	
4F4	SM-Timer LSBs	U-Timer LSBs	Emulated Record Number	
4F5	..... Max Relative Word Number			
4F6	SM-Timer MSBs	U-Timer LSBs	SM Done Interrupt Prcsng. Return Location (MSB)	
4F7	SM Done Interrupt Processing Return Location LSBs	Advance to Next Record Jump Location	Saved Next XMCI Jump Location	
4F8	..... R1 Temporary Save		R2 Temporary Save	
4F9	R3 Temporary Save	..... R5 Temporary Save		
4FA	..... Q Register Temporary Save		INITSEEK Return MSB	
4FB	WAITSEEK Return LSB	R6 Temporary Save	Track-Hold Counter	
4FC	2-Drives-Per-Unit Flag	UMA ECC Test Flags	INITSEEK Return LSB	
4FD	Initial Emulated Cylinder LSB	Initial Emulated Cylinder (MSB) & Head Initial Word Number		
4FE	..... Initial Actual Cylinder		Initial Actual Head	
4FF	Initial Actual Record	..... ILD Return 5		

THUMBWHEEL DISPLAY LOCATIONS 500 THROUGH 50F (except 502,503,504, and 507 which follow)

These thumbwheel display locations are not applicable to the 7100-30.

Thumbwheel Display Locations 502 through 504

These thumbwheel display locations are not applicable to the 7100-30.

Thumbwheel Display Location 507

This thumbwheel display location is not applicable to the 7100-30.

Thumbwheel Display Locations 510 through 516

These thumbwheel display locations are not applicable to the 7100-30.

Thumbwheel Display Locations 517 through 519 and 51A

These thumbwheel display locations are not applicable to the 7100-30.

Thumbwheel Display Locations 51B through 51F

Display Location	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
51B	Next SM DMA Address MSB	Next SM DMA Address LSB	Not Used	
51C	Bad SM DMA Address MSB	Bad SM DMA Address LSB	Not Used	
51D	Expected U DMA Address MSB	Expected U DMA Address LSB	Only Valid Copy Flag	
51E	Bad U DMA Address MSB	Bad U DMA Address LSB	End U DMA MSBs (Read)	
51F	Good U DMA Address MSB	Good U DMA Address LSB	End U DMA LSBs (Read)	

Thumbwheel Display Locations 520 through 527

These thumbwheel display locations are not applicable to the 7100-30.

THUMBWHEEL DISPLAY LOCATIONS 528 THROUGH 532

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Drive Flags Unit (see # below)	Drive Flags Unit (see # below)	Drive Flags Unit (see # below)

Display Location			
528	0	1	2
529	3	4	5
52A	6	7	8
52B	9	10	11
52C	12	13	14
52D	15	16	17
52E	18	19	20
52F	21	22	23
530	24	25	26
531	27	28	29
532	30	31	Data Copy Unit

For each display there are 12 bits which describe the characteristics of the drive. They are broken down as follows:

Bits 1-3 comprise an octal digit which indicates drive type:

0 = Undefined
1 = Fujitsu Eagle
2 = CDC513
3 = M2333
4 = M2382 (Swallow 5)
5 = M2344 (Swallow 4)
6 = MPI9720
7 = MPI 9720 with Defect Tracks

Bits 4 and 5 comprise an octal digit which indicates record length:

0 = Undefined
1 = 112-word prep
2 = 448-word prep
3 = 1792-word prep

Bit 10: if bit 10 = 0, there is one physical drive per logical unit;
if bit 10 = 1, there are two physical drives per logical unit.

THUMBWHEEL DISPLAY LOCATION 533

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
SSS Unit Size (megawords)	Not Used	Not Used	

Thumbwheel Display Locations 534 and 535

Reserved for Future Use.

Thumbwheel Display Locations 536 through 540

These thumbwheel display locations are not applicable to the 7100-30.

Thumbwheel Display Locations 541 through 54F

These thumbwheel display locations are not applicable to the 7100-30.

THUMBWHEEL DISPLAY LOCATIONS 550 - 553: HSSM Confidence Test

| 35 34 33 32 31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 15 14 13 12 | 11 10 9 8 7 6 5 4 | 3 2 1 0 |

Display Location	
550	Reference Word 0
551	Reference Word 1
552	Reference Word 2
553	Reference Word 3

THUMBWHEEL DISPLAY LOCATION 554

Reserved for Future Use

THUMBWHEEL DISPLAY LOCATION 555: Confidence Test Error Display

| 35 34 33 32 31 30 29 28 27 26 25 24 | 23 22 21 20 19 18 17 16 15 14 13 12 | 11 10 9 8 7 6 5 4 | 3 2 1 0 |

Bit	
28	XRBP Failure
27	XMC /XM16KP Failure
26	OCP Failure
25	HSSM Failure
24	WMAP Failure

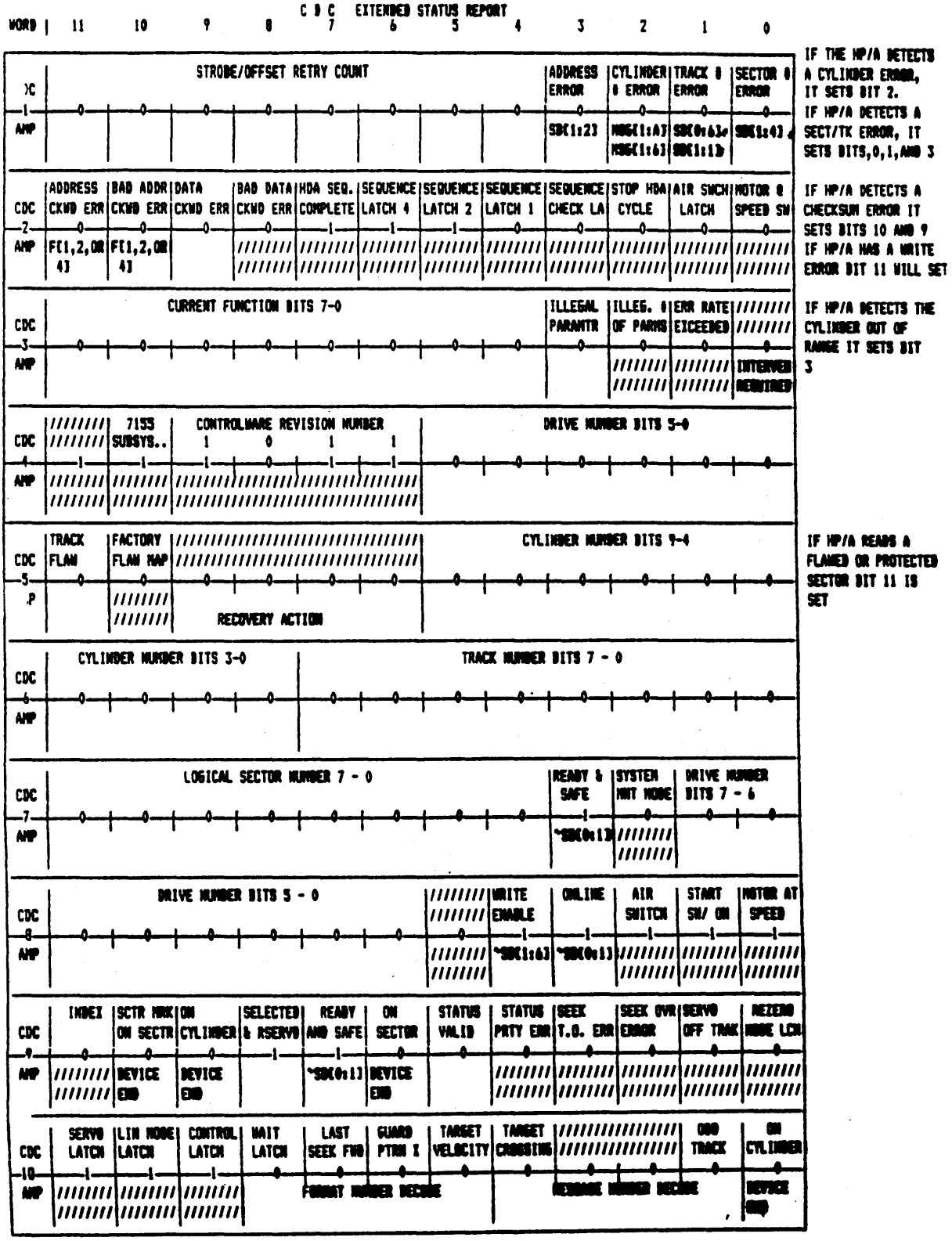
Thumbwheel Display Locations 800-BFF

These thumbwheel display locations are not applicable to the 7100-30.

8.5 CDC General Status

Bit	Definition
11	Abnormal termination. Preceding function terminated abnormally. General status bits 8 and 9 indicate whether recovery is possible. Detailed status shows cause of abnormal termination.
10	Multiple-access controller reserved. Controller is reserved to another PP channel. All other status bits are meaningless.
9	Nonrecoverable error. Controller detected error from which no recovery is possible. Detailed status identifies error.
8	Recovery in process. Controller is ready to attempt error recovery in response to 0014 (continue) function.
7	Checkword error. Controller detected checkword error in address field or data field of record. Detailed status word 2, bits 8 through 11, provides error analysis.
6	Correctable address error. Controller detected correctable read address checkword error. 0014 (continue) function enables data to be processed on subsequent disk revolution.
5	Unused.
4	Drive malfunction. Drive-related error occurred. Detailed status reflects drive status at time of malfunction.
3	Drive reserved. Requested drive is reserved by other controller.
2	Autoload error. Controlware loaded is not compatible with controller.
1	Busy. Controller and/or requested drive are busy.
0	Unused.

8.8 CDC Detailed Status



C D C EXTENDED STATUS REPORT

WORD	11	10	9	8	7	6	5	4	3	2	1	0
CDC 11	CAPABLE ENAB ERR	WRITE OVERRUN	MULTIPLE HEAD ERR	WRITE CRNT ERR	WRITE TRANSIT	CONTROL ERROR	INDEX CHECK	HEAD SHORT	I/O NO CONTROL	WRITE IN OFFSET	////	////
AMP 11	EQUIP CHECK	////	////	////	////	////	////	////	////	////	////	////
CDC 12	EARLY STROBE	LATE STROBE	FORWARD OFFSET	////	////	SECTOR CMPR ERR	DRIVE ERROR	////	READ/WRI ERROR	////	////	ACCESS CHECK
AMP 12	////	////	////	////	////	////	////	////	DATA CHECK	UNIT CHECK	////	////
CDC 13	BUFFR TO DISK ERR	ACC CONN B4 GEN'L	DRIVE B4 CONNECT	////	////	////	////	////	////	////	////	////
AMP 13				ERR HP/A DETECTED	SENSE BYTE 8							
CDC 14	////	////	////	////	////	////	////	////	////	////	////	////
AMP 14	SENSE BYTE 9								SENSE BYTE 10 UPPER NIBBLE			
CDC 15	////	////	////	////	////	////	////	////	////	////	////	////
AMP 15	SENSE BYTE 10 LOWER NIBBLE				SENSE BYTE 11							
CDC 16	LOST DRV CLOCK	UNUSED BUT RESERVED			ECC RES. NONZERO	CHAN DAT PRTY ERR	PROCESS. INST T-O	LOST CNTRL WD	UP/DOWN CNT <> 0	PAK UNSF NOT READY	BUFF OUT PRTY ERR	WRITE VRFY ERR
AMP 16	////	////	////	////	////	////	////	////	////	////	////	////
CDC 17	SYNC BYT SEARCH	SECTOR LEN BAD	LOST DATA	SYNC BYT MISCOMPR	CKWD ERR CRCN TRY	BUFF OUT REG FULL	BUFF IMP REG FULL	CHANNEL RESERVED	DEADMAN TIMEOUT	CHANNEL ACTIVE	DATA FLD ERR	ADDRESS FLD ERR
AMP 17	////	SDE1s13*	////	////	////	////	////	////	////	////	////	////
CDC 18	D	C	B	A	////	////	////	ECHO MODE	LARGE SECTOR	////	////	////
AMP 18					////	////	////	////	////	////	////	////
CDC 19	////	////	////	////	////	////	////	////	////	////	////	////
AMP 19	SENSE BYTE 12								UPPER NIBBLE OF SENSE BYTE 14 FOR FORMAT 4, SENSE BYTE 16			
CDC 20	////	CONTROLLER HARDWARE UNIQUE IDENTIFIER										
AMP 20	LOWER NIBBLE OF SENSE BYTE 14 FOR FORMAT 4, SENSE BYTE 16											

HP/A SETS BITS 9 AND 10.

HP/A WILL UPDATE BITS 8,9,10,AND11 FOR THE ACCESS CONNECTED

Note: For a tilde (~) please read "NOT"
SB[x:y] means Amperif Sense Byte Number x Bit y
MSG[j:k] means Amperif Sense Byte 7 Format j Message k
FSB[n:x:y] means Amperif Format n Sense Byte Number x Bit y
WD[m:n] means CDC Extended Status Byte m Bit n

Comments:

8.7 Converting from CDC to 9720-Sabre 5

To convert from CDC cylinder, track, and record to 9720-Sabre 5 physical cylinder, track, and record, use the following formula: (Be sure to convert CDC numbers of cylinders, tracks, and records to decimal numbers before using this formula.)

$$((\text{CDC cylinder} \times 1280) + (\text{CDC track} \times 32) + \text{CDC record}) \times 116 = \text{RWA}$$

where

$$\frac{\text{RWA}}{67 \times 116 \times 15} = \text{whole \#1} + \text{fraction \#1}$$

whole #1 = physical cylinder

fraction #1 X 15 = whole #2 + fraction #2

whole #2 = physical head

fraction #2 X 67 = record + 1 = record

For ILD purposes, only the cylinder and head are needed.

8.8 CDC Function Codes

Octal Code	Function	Words Output	Words Input	General Status Required
0000	Connect (1)	1		Yes
0001	Seek, 1:1 interlace (1)	4		Yes
0002	Seek, 2:1 interlace (1)	4		Yes
0004	Read		(6)	Yes
0005	Write	(6)		Yes 2
0006	Write verify	(6)		Yes 2
0007	Read checkword			Yes
0010	Operation complete			No
0011	Disable drive reserve			No
0012	General status		1	No
0013	Detailed status		12	No
0014	Continue	(6)(3)	(6)(4)	Yes
0015	Drop seeks			No
0016	Format pack (1)	7		Yes
0017	Return drive address		3	No
0020	Drive release			No
0021	Return cylinder address		1	No
0022	Set/clear flaw (1)	1		Yes
0023	Extended detailed status		20	No
0024	Read gap sector		(6)	Yes
0025	Write gap sector	(6)		Yes (2)
0026	Write verify gap sector	(6)		Yes (2)
0027	Read checkword gap sector			Yes
0030	Read factory data		322	Yes
0031	Read utility map		322	Yes
0032	Block transfer buffer read		322	No
0033	Block transfer buffer write (1)	322		Yes
0034	Read protected sector		322	Yes
0035	Write last sector	(6)		Yes
0036	Write verify last sector	(6)		Yes
0037	Write protected sector	322		Yes
0040	Read short		319 (5)	Yes
0041	Select strobe and offset (1)	1		Yes
0042	Clear connected access			No
0043	Buffer read		322	Yes
0044	Buffer write	322		Yes
0046	Write buffer to disk			Yes
0047	Scan cylinder addresses			Yes
0050	Output on processor channel (1)	3		Yes
0051	Execute control word sequence (1)	49		Yes

NOTES

(1) When PP channel deadman timer expires during this function, controller prepares 5000 general status and sets deadman timeout bit (word 17, bit 3) in detailed status.

(2) Except when executing this function at 2:1 interlace on 844 drive, controller returns general status before transferring data from buffer to disk. If error occurs during buffer-to-disk transfer, controller responds only to 0012 (general status) function. This ensures that buffer-to-disk errors do not go undetected.

(3) Following write-type function only.

(4) Following read-type function only.

(5) 844 only; use 318 for 885; 1360 for 885 large sector.

(6) 322 words for small sector, 1376 words for large sector 885.

SUBSYSTEM FUNCTIONS (Contd)

Octal Code	Function	Words Output	General Words Input	Status Required	Octal Code	Function	Words Output	General Words Input	Status Required
0052	Input processor channel status		32	No	0063	Input display data		64	No
0053	Echo output channels		32	No	0064	Time difference counter			No
0054	Issue processor flag pulse 1	1		Yes	0066	Force Error	1		Yes
0055	Enable input channel timing 1	1		Yes	0067	Interlock Autoload	16870		Yes
					01NN	Autoload from disk			No
0056	Input timing data		2	No	03NN	Disk deadstart			No
0057	Echo one word	1	1	No	0414	Autoload from PP	16870		Yes
0061	Autodump		12288	No	0720	Echo one word	1	1	No
0062	Manipulate processor	5		No					

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9. CONTROLLER FIELD REPLACEABLE UNIT (FRU) INDEX

This section provides procedures for isolating and identifying failed Field Replaceable Units (FRU) in the Amperif 7100-30 Mass Storage System.

NOTE: *The following FRU index is not complete.*

The 7100-30 controller detects and generates error information on specific error conditions within the controller, the HSSM, the disk interface, and the disk drives themselves.

These errors are stored in the scratchpad memory and an interrupt is sent to the host system. The host system issues a sense I/O command to retrieve the sense bytes. The sense bytes can then be printed at the host console or can be retrieved from the host system log file. These errors can also be read from the controller scratchpad memory, via the OCP (COCP) thumbwheel switch. See section 8 for the location and format of the error information.

The following chart tells you which section contains information about a specific error type:

Host Error Indication	Error Type	Go to
Sense Byte 07 = 1x	Unit Check	Section 9.1
Sense Byte 07 = 2x	Equipment Check	Section 9.2

9.1 Unit Checks

This section covers the unit check category of errors (sense Byte 07 = 1n). Unit checks are generated by the controller.

There are eight error types in this category. FRU lists and error descriptions for each of the eight error types are described in the following sections.

1. Sense byte 07 = 10 (section 9.1.1)
2. Sense byte 07 = 16 (section 9.1.2)
3. Sense byte 07 = 17 (section 9.1.3)
4. Sense byte 07 = 19 (section 9.1.4)
5. Sense byte 07 = 1A (section 9.1.5)
6. Sense byte 07 = 1C (section 9.1.6)
7. Sense byte 07 = 1E (section 9.1.7)
8. Sense byte 07 = 1F (section 9.1.8)

Table 9-1
FRU Error Selection Matrix Chart

NOTE: *This chart defines a subgroup of FRUs for a particular error condition. Use with sections 9.1.1 through 9.1.8.*

CONTROLLER OPERATION	BYPASS	
ERROR OCCURS THROUGH:	ONE	BOTH
ALL DRIVE DEVICES	1B	6B
ONE DRIVE CABINET	2B	7B
ONE DRIVE GROUP	3B	8B
ONE DRIVE DEVICE	4B	9B
ONE DRIVE HDA	5B	10B

9.1.1 Sense Byte 07 = 10 Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 08 = 02	Busy	Use table 9-1 to determine applicable FRU lists.	While attempting to select a disk drive, the controller received a busy status from the disk.

FRU Lists

1B	2B	3B	4B	5B	6B 7B 8B	9B	10B
*	*	*	*	DCB I/O PCB A cable B cable	*	*	DCB (drive board) I/O PCB (drive board) DRIVE

* This situation should only occur from a single defective drive HDA, to either one or both controllers.

9.1.2 Sense Byte 07 = 16 Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 07 = 16	Set CAR error	Use table 9-1 to determine applicable FRU lists.	After a drive presented a seek complete status to the controller, the controller read a record header of the disk and determined that the drive was at the wrong cylinder.

9.1.3 Sense Byte 07 = 17 Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 07 = 17	Set HAR error	Use table 9-1 to determine applicable FRU lists.	After a drive presented a seek complete status to a controller, the controller read a record header and determined that the drive was at the wrong head.

FRU Lists

1B	2B	3B	4B	5B	6B 7B 8B*	9B	10B
DIFE	AIO	AIO	BIOE	BIOE	see below	BIOE	DCB
MPCP	(2)cable	(3)cable		DCB		DCB	CON

* This situation should only occur from a single defective drive HDA, to either one or both controllers.

9.1.4 Sense Byte 07 = 19 Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 07 = 19	Drive status not as expected		

9.1.5 Sense Byte 07 = 1A Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 07 = 1A	Seek error		

9.1.6 Sense Byte 07 = 1C Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense byte 07 = 1C	HSSM SM-Interrupt timeout		

9.1.7 Sense Byte 07 = 1E Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 07 = 1E	Unable to determine drive type		

9.1.8 Sense Byte 07 = 1F Unit Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 07 = 1F	Initial select busy timeout		

9.2 Equipment Checks

This section covers the equipment check category of errors (sense byte 07 = 20). Equipment checks are generated by the controller. FRU lists and error descriptions for equipment checks are described in this section.

Sense Byte 07 = 20 Equipment Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 08 = 02	MDB U-DMA check	MDB MPCP XMC XMCIP DIFE	After a U-side data transfer completed, the U-DMA ending address was different from the microcode-computed ending address.
Sense Byte 08 = 04	HSM test failure	XMC Backplane	During the controller throughput checking, the HSM test failed.

Sense Byte 07 = 20 Equipment Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 09 = 0x	HSM/HSSM test failure codes	N/A	HSM/HSSM error codes. Sense byte 08 equals a 04 HSM failure code. Sense byte 09 equals a 40 HSSM failure code.
Sense Byte 09 = 08	MDB SM DMA check	MDB MPCP XMC DIFE XMCIP	After an SM-side data transfer completed, the ending address of the SM-DMA was different from the microcode-computed ending address.
Sense Byte 09 = 10	DIF FIFO check	DIFE MDB XMCIP MPCP	After a data transfer completed, the FIFO on the DIFE had not gone empty.
Sense Byte 09 = 40	HSSM test failure	MPCP MDB DIFE XMCIP	During the controller throughput checking, the microcode detected one of eight failures having to do with a disk operation.
Sense Byte 09 = 80	ALU address conversion failure	XMC XM16KPD XM16KP	While doing a relative word address conversion, the XMC detected an error between two subsequent calculations for the same data.
Sense Byte 10 = 01	DIF parity error	MDB DIFE MPCP XMCIP Backplane	While trying to read either the CMC-bus or the MDB-bus, the DIFE detected bad parity.

Sense Byte 07 = 20 Equipment Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 10 = 02	HSM/HSSM Instruction Bus parity error	XMC XMCIP INST cable Backplane	While reading the INSTRUCTION-bus, the XMCIP detected bad parity.
Sense Byte 10 = 04	SMB parity error	XMC	While reading data from the scratchpad memory, the XMC detected bad parity.
Sense Byte 10 = 08	HSSM U-bus parity error	XMCIP XMC UBI U-bus cable Backplane	While receiving data from the U-bus, the XMCIP detected bad parity.
Sense Byte 10 = 20	XMC CT-bus parity error	XMC XMCIP COCP CT cable Backplane	During a read operation of the CT-bus, the XMC detected bad parity.
Sense Byte 10 = 40	XMC U-bus parity error, upper bits	XMC UBI U-bus cable XMCIP Backplane	While reading the upper 18 bits of the U-bus, the XMC detected bad parity.
Sense Byte 10 = 80	XMC U-bus parity error, lower bits	XMC UBI U-bus cable XMCIP Backplane	While reading the lower 18 bits of the U-bus, the XMC detected bad parity.
Sense byte 11 = 01	HSSM/MDB detected buffer memory error	MDB XMCIP MPCP DIFE Backplane	While reading the MDB buffer via the UMD-bus, the XMCIP detected bad parity.
Sense Byte 11 = 02	HSSM parity error or internal check error	MDB XMCIP MPCP DIFE Backplane	While reading the CMC-bus, the MPCP detected bad parity. or the MDB had an internal check error

Sense Byte 07 = 20 Equipment Check

Error Indication	Mnemonic	FRU List	Error Description
Sense Byte 11 = 04	HSSM CT-bus parity error	XMCIP XMC COCP CT cable Backplane	While reading the CT-bus, the XMCIP detected bad parity.
Sense Byte 11 = 08	HSSM busy timeout	XMCIP MPCP MDB DIFE XMC	While trying to select the HSSM for a disk operation, the XMC timeouts due to the busy flag being continuously set.
Sense Byte 12 = 20	OCP not available	OCP XMC INST-bus CT-bus Backplane	The OCP could not be selected.
Sense Byte 12 = 40	OCP parity error	OCP	During a read operation of the drive status memory, or INST-bus parity, or CT-bus parity, the OCP detected a parity error.

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10. SUBASSEMBLY REMOVAL/REPLACEMENT PROCEDURES

This section describes the procedures required to remove and replace defective devices within the 7100-30.

10.1 Pluggable Logic Board/Card

Removal and replacement procedures are described below.

10.1.1 Removal

1. Remove power from the power supply that powers the board/card to be removed.
2. All pluggable logic boards/cards in the controller are equipped with two camming lock-down levers. Rotating these levers simultaneously (out and up for the top, and out and down for the bottom), will disengage the logic board/card from its backplane connector.
3. Grasp board/card gently but firmly and pull out.

10.1.2 Replacement

1. Place board/card in top and bottom alignment guides.
2. Seat board/card to backplane connectors by gently but firmly engaging the camming lock-down levers on the top and the bottom of the cage until levers rest against the edge of the board/card. DO NOT FORCE.
3. If board/card will not seat, remove and inspect for bent pins on backplane or other obstructions.

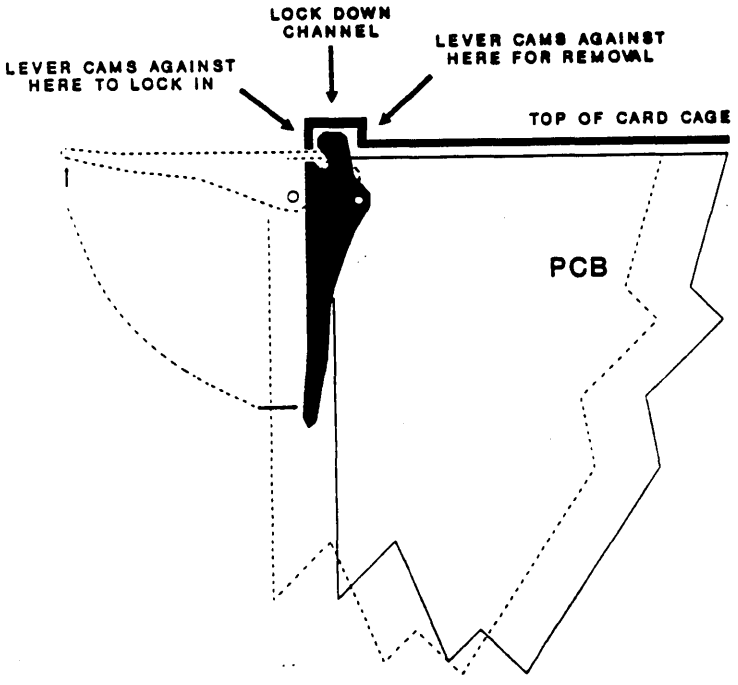


Figure 10-1
Pluggable Logic Board/Card Removal

10.2 Disk Drive Power Supply

1. At the system console, down the applicable drive via controller A path and controller B path.
2. At the OCP, place the applicable drive in bypass mode.
3. At the disk drive control panel, perform the following operations for the applicable drive:
   - o Deactivate the CHA and CHB switches to place the drive offline.
   - o Activate the drive write protect switch.
   - o Deactivate the PWR switch.
4. Open the rear door of the 7100-30 cabinet. All remaining steps can be performed at the rear of the cabinet.
5. Turn off the applicable drive power switch located at the front of the power supply.
6. Carefully slide the drive tray out of the cabinet. Pull the tray out far enough to access the cable connections.
7. Using a magnetic-tip Phillips screwdriver, remove the four screw/washer assemblies (two in front and two in back) which secure the power supply to the drawer, and lift the power supply out.
8. Disconnect the DC power harness from the power supply by pulling it gently but firmly. You may want to use pliers at either side to help.
9. Remove the AC plug from the back of the power supply.
10. Mounting brackets must be removed from the power supply if the supply is to be replaced. (There are four screws holding the power supply to the bracket.)
11. Install in reverse order.

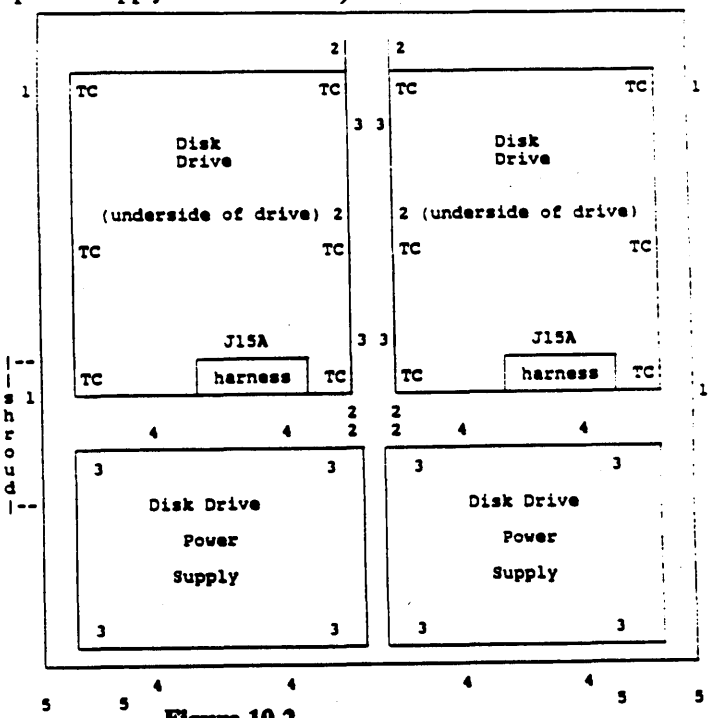


Figure 10-2
Disk Drive Power Supply Removal

NOTES: *The shroud covers the space between the bottom of the drives and the top of the power supplies.*
1 - These screws attach the drive directly to the tray.
2 - These screws attach the bracket to the tray.
3 - These screws attach the power supply (or the drive) to the power supply (or drive) bracket.
4 - These screws attach the power supply bracket to the tray.
5 - These screws attach the locking hold-down brackets mounted across the front of the drive tray.

10.3 CDCI Board

1. Power off the appropriate controller.
2. Remove the in and out I/O cables on the affected rack; label them, if necessary.
3. Remove the two signal cables from the top CDCI board.
4. Remove the two signal cables from the bottom CDCI board.
5. Remove the VCC and GND wires from the top and bottom CDCI boards.
6. Remove the five screws holding the rack to the frame.
7. Remove the two I/O signal cables from the CDCI board.
8. Support the board with one hand while removing the four screws holding the CDCI board to the rack.
9. Reinstall in reverse order.

NOTE: *Be sure to reinstall all four mounting screws to prevent VCC from shorting to the frame.*

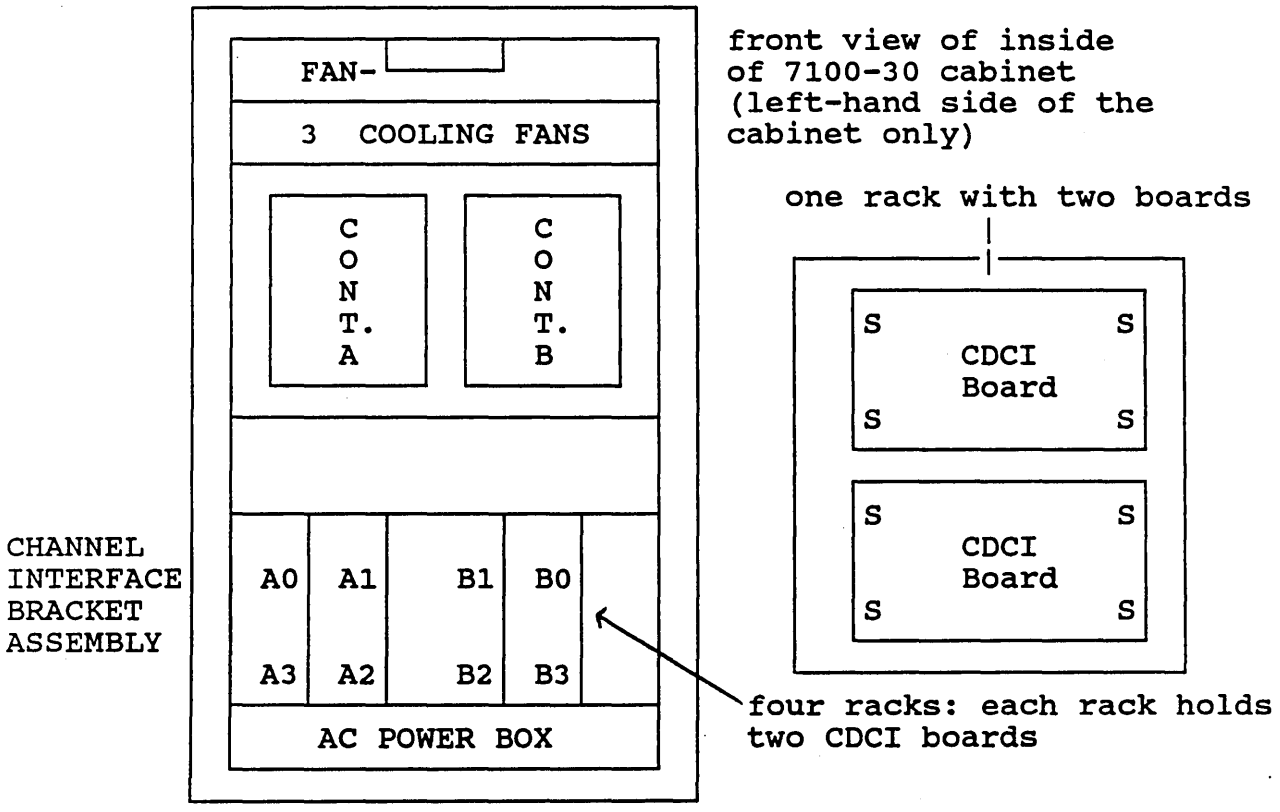


Figure 10-3
CDCI Board Removal

10.4 Driver/Receiver Board

The removal and replacement procedures for the driver and receiver boards are identical; the only information which differs is where they are plugged into the backplane. This information follows:

- The driver boards are plugged into JJ1A for the A controller and MJ1A for the B controller.
- The receiver boards are plugged into JJ2A for the A controller and MJ2A for the B controller.

1. Make sure that the channel is down at the host. (This means that the channel is inactive and there is no I/O activity occurring.)
2. Take the matching channel of the sister 7100-30 system offline.
3. Unplug the 40-pin connector from the board.
4. Using a Phillips screwdriver, loosen the two screws closest to you on the bracket which attaches to the backplane.
5. Grasp the cable side (right side) of the board and gently but firmly pull it out.

In the figure below, S represents a Phillips screw.

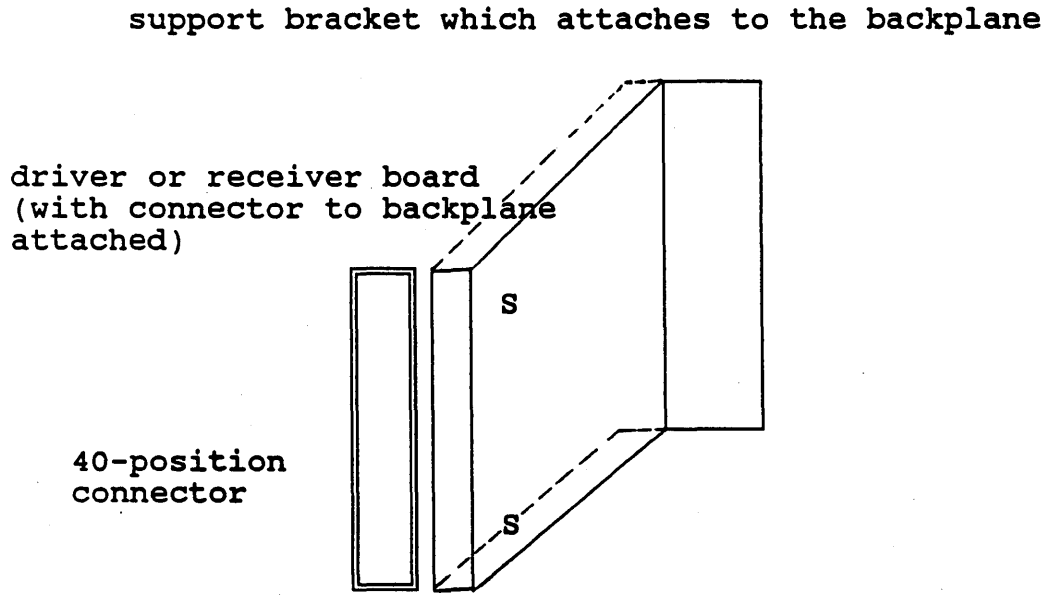


Figure 10-4
Driver/Receiver Board Removal

10.5 Controller Cardcage

1. Power off dual controller.
2. Label and remove all boards from the controller cardcage.
3. Label and remove all signal cables from backplane board.
4. Label and remove the three heavy black 5V cables (and any other wires) from the 5V lugs on the backplane.
5. Label and remove the ground cables from the left end of the ground bus (mounted on the rear of the backplane).
6. Locate twisted pair (one white, one black) wires on left side of AC fan supply (outside of the cage). Label and disconnect the slip-on connectors.
7. Remove eight mounting screws at front of cage.
8. Reinstall in reverse order.

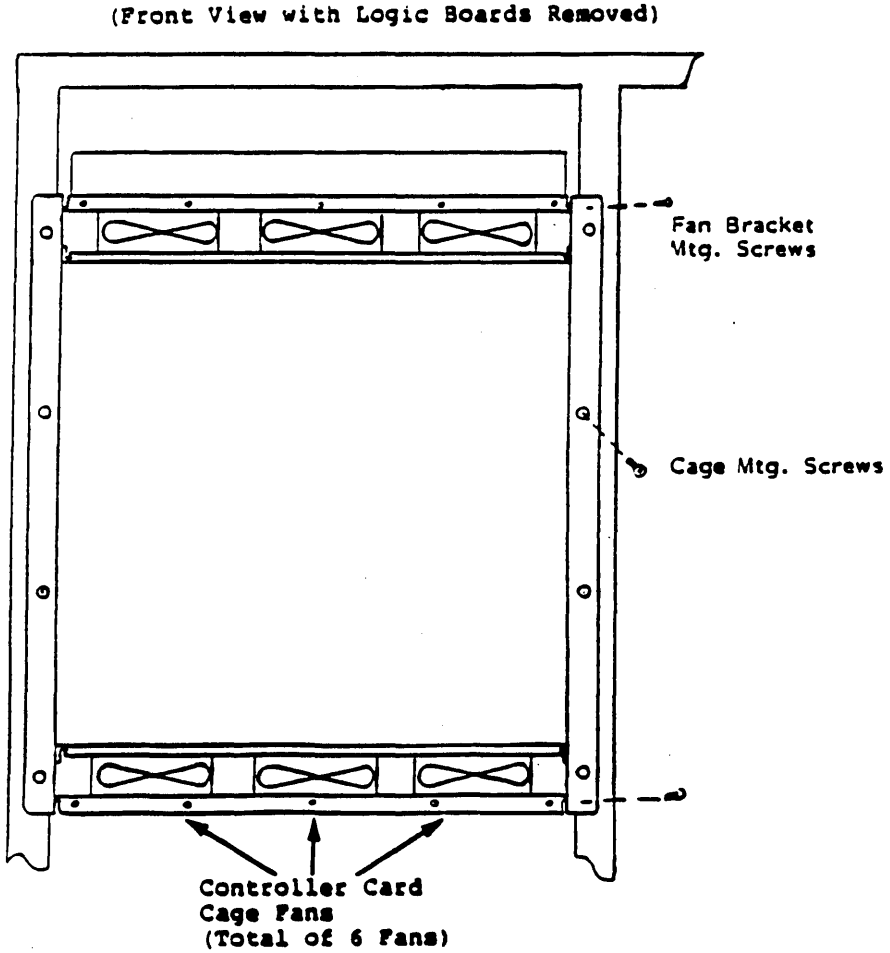


Figure 10-5
Controller Cardcage Removal

10.6 Controller Cardcage Backplane

1. Remove controller cardcage as described in section 10.5. See figure 10-5.
2. Place cardcage on flat surface with backplane up.
3. Remove ten screws holding backplane to frame.
4. Reinstall in reverse order.

10.7 Controller Cardcage Fan

1. Remove controller cardcage as described in section 10.5. See figure 10-5.
2. Place cardcage on flat surface with backplane board up. (Be careful not to bend connector pins on backplane.)
3. Remove three screws from each side of controller cardcage for the three-fan assembly to be removed (upper or lower).
4. Tilt fan assembly out, taking care not to damage the two AC input wires to the assembly.
5. Remove the slip-on connectors of the fan being replaced.
6. Remove the four mounting screws holding the fan to the assembly.
7. Reinstall in reverse order.

10.8 Top Cover

1. Power off the dual controller before proceeding.
2. Remove fan ground and unplug power to fans.
3. Remove eight top cover nuts and screws (A).
4. Carefully slide top fan assembly in whatever direction is convenient for removal.

CAUTION: **Because the unit weighs 40 lbs., we recommend that two people work together to remove or replace it.**

5. Reinstall in reverse order.

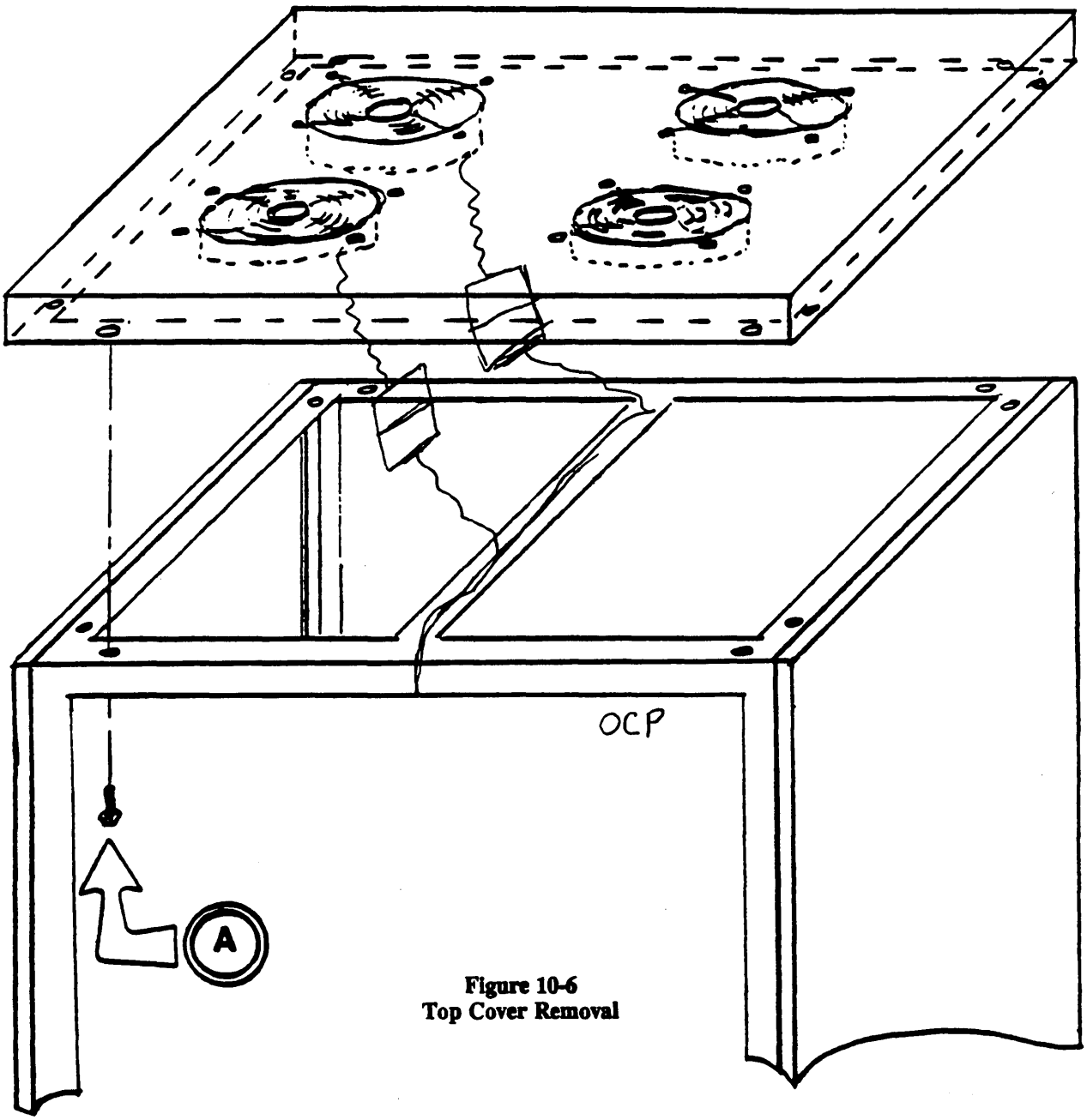


Figure 10-6
Top Cover Removal

10.9 Top Cover Fan

1. Remove top cover as described in section 10-8. See figure 10-6.
2. Remove the slip-on connectors of the fan being replaced.
3. Remove four screws holding fan to top cover assembly.
4. Reinstall in reverse order.

10.10 Disk Drive I/O Cardcage

1. Power off the 7100-30 (along with the A side of the sister system, if there is one). Be sure that all drives (in both systems) have been write protected.
2. Label and remove all cards from I/O cardcage.
3. Label and remove all signal cables from I/O cardcage backplane.
4. Cut cable ties on voltage and ground cables along top rear and left side of cage.
5. Label (if necessary) and remove voltage and ground wire from lugs on backplane.
6. While supporting cage with one hand, remove four mounting screws and remove assembly.

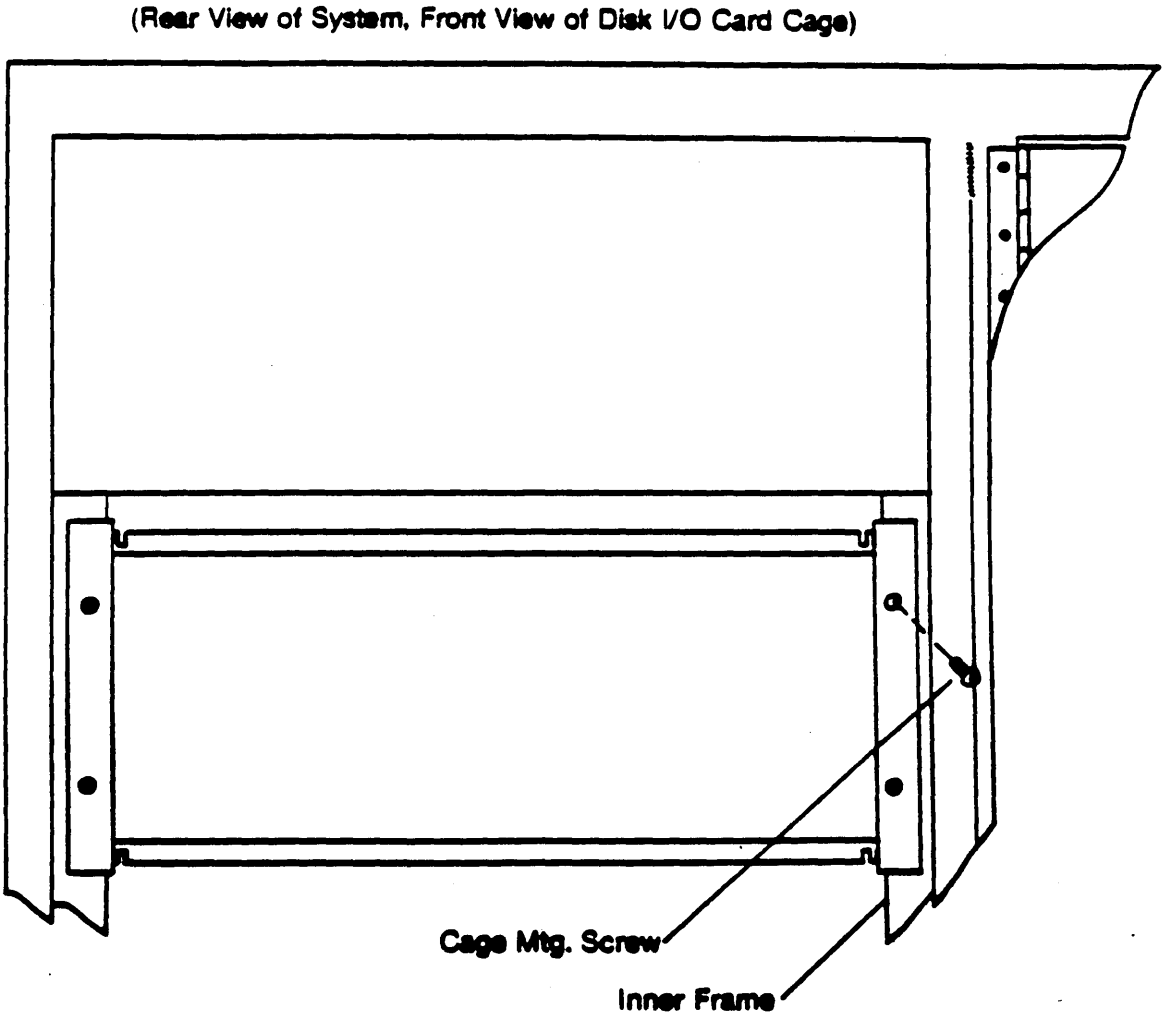


Figure 10-7
Disk Drive I/O Cardcage Removal

10.11 Disk Drive I/O Cardcage Backplane

1. Remove disk drive I/O cardcage as described in section 10.10. See figure 10-7.
2. Place cardcage on flat surface with backplane up.
3. Remove ten screws holding backplane to cage frame.
4. Reinstall in reverse order.

10.12 Expansion Cardcage

1. Power off the 7100-30 (along with the A side of the sister system, if there is one). Be sure that all drives (in both systems) have been write protected.
2. Label and remove the three cards from the expansion cardcage. See figure 10-8.
3. Label and remove all signal cables from the expansion cardcage backplane.
4. Cut cable ties on voltage and ground cables along top rear and left side of the cage.
5. Label (if necessary) and remove voltage and ground wire from lugs on backplane.
6. While supporting cage with one hand, remove four mounting screws and remove assembly.

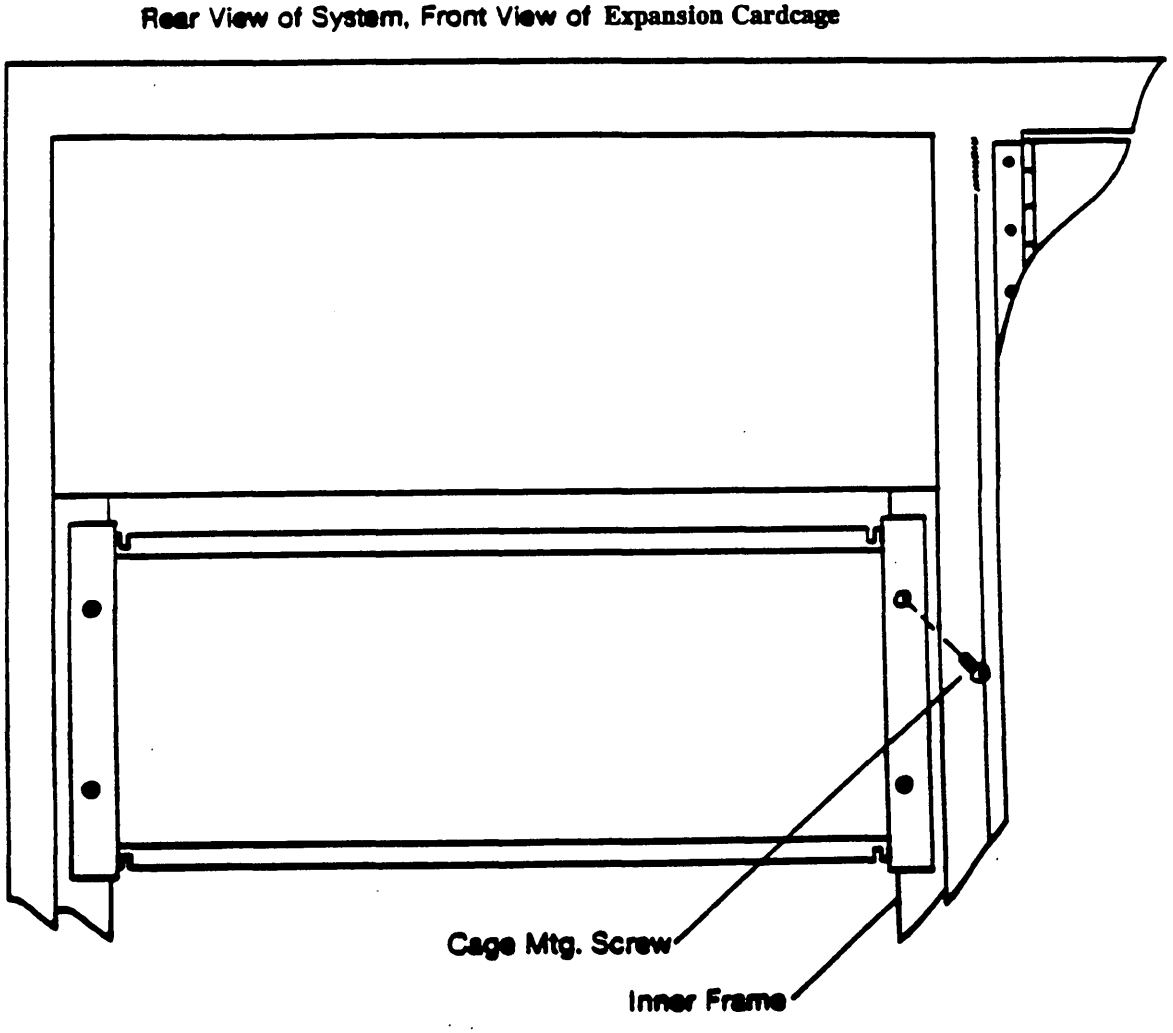


Figure 10-8
Expansion Cardcage Removal

10.13 Expansion Cardcage Backplane

1. Remove expansion cardcage as described in section 10.12. See figure 10-8.
2. Place cardcage on flat surface with backplane up.
3. Remove ten screws holding backplane to cage frame.
4. Reinstall in reverse order.

10.14 Disk Drives

The following sections describe removal and replacement procedures for the 9720 drives in the 7100-30.

10.14.1 Removal

1. At the system console, down the applicable drive via control unit A path and control unit B path.
2. At the 7100-30 OCP, place the applicable drive in bypass mode.
3. At the disk drive control panel, perform the following operations for the applicable drive:
   - o Deactivate the CHA and CHB switches to place the drive offline.
   - o Activate the WRITE PROTECT switch for the drive.
   - o Deactivate the PWR switch to power down the drive.
4. Open the rear door of the cabinet; all remaining steps can be performed at the rear of the cabinet.
5. Turn off the applicable drive via the on/off switch located on the power supply for that drive.
6. Remove the locking hold-down brackets mounted across the drives. This bracket is held in place with four screws: two on the left side and two on the right side front of the drive tray.
7. Carefully slide the drive tray out of the cabinet. Pull the tray out far enough to access the cable connections.
8. Disconnect all interface cables from the rear of the applicable drive.
9. Remove the shroud covering the space between the power supply and the drive by removing the two screws at the top front of the drives and then lifting the shroud up. Then remove the drive top cover; it is held in place with six screws, three on each side of the drive.
10. Disconnect the DC power harness. See figure 10-9, J15A.
11. Remove the four screws that attach the drive bracket to the drive tray. Two of these are located at the front between the drives (one upper and one lower), the third is located in the back of the tray, and the fourth is located beneath the drive. See figure 10-9.
12. Remove the two screws on the side of the tray; these go through the drive tray and into the drive itself. See figure 10-9.
13. Slide the drive forward and lift it out of the drawer.
14. Remove the drive from the bracket by removing the two mounting screws which attach it to the bracket. See figure 10-9.

10.14.2 Replacement

Replace a drive using the same procedures described in "Removing a Disk Drive," but perform them in reverse order. Keep in mind that if a replacement drive (or HDA) is to be installed, the following additional steps are required:

1. Uncrate the replacement drive or HDA. Check the shock watch on the unit to ensure that it has not been damaged in shipment. If damage has occurred, the unit must be returned unused. Verify that a manufacturer's media flaw map is present and that the indicated serial number matches the replacement unit.

2. Set switches to match the settings on the drive being removed. See figures 10-10 and 10-11.

3. If the drive you are installing is the last one on the string, leave the terminators in place; if not, remove the terminators. Make sure that the power supply is switched on. Install the replacement drive and turn on the AC power. Wait for the drive to spin up and for all "normal" lights to appear. Be sure that a READY indication appears on the drive control panel and the drive itself.

4. At the system console (host), down either control unit A or control unit B. The downed control unit will be used to run inline diagnostics (ILDs) to the replacement drive.

5. Load the OCP data switches with the worst case data pattern for the drive (6AF6DB06F).

6. For first-time formatting of a 9720 drive, follow the steps below:

   a. Load Toggle 7.
   b. Perform ILD 1. (CYL 0 to CYL 1633; HD 0 to HD 14.)
   c. Turn off the clock on the MPC board (top switch down) and answer **YES** when **DRIVE X OK?** is displayed at the OCP.
   d. Turn on the clock on the MPC board (top switch up) and answer **YES** when **DO YOU WANT TO FORMAT DRIVE X?** is displayed at the OCP,

7. Allow the ILD 1 format operation to complete normally.

8. Create a new alternate track log for the drive by following these procedures:

   a. Record the drive number and the drive serial number on a blank alternate track log sheet.
   b. Refer to the media flaw map for the drive. In sequential order, write down the cylinder and head number for all error bursts.

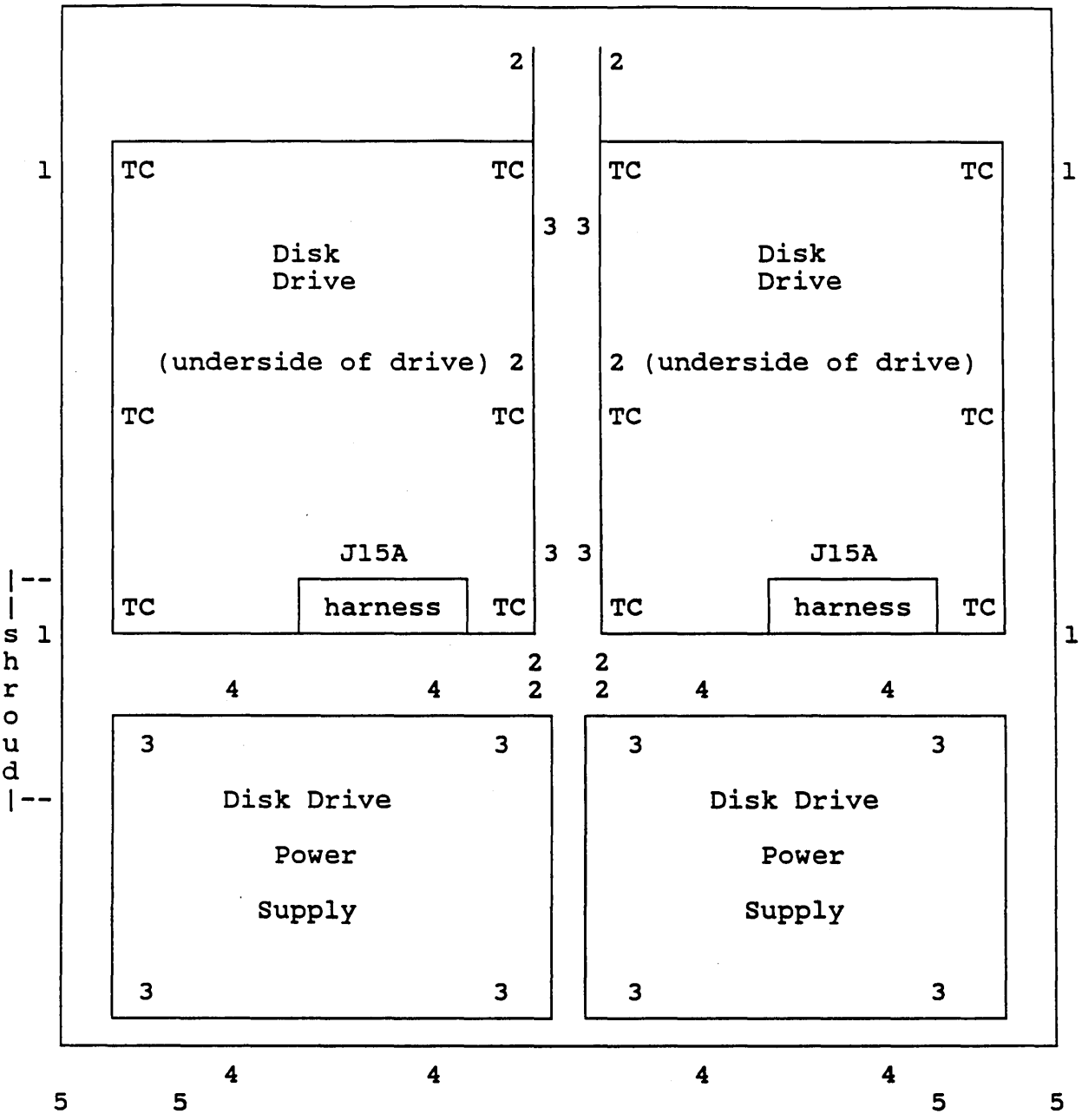
9. Use ILD 4 to flag (as defective) all alternate tracks on the drive which are indicated on the flaw map. The alternate tracks are in the range of cylinders numbered 1624 through 1633.

10. Optionally, run ILD 3 to verify the formatting of the defective tracks.

11. Run ILD 2 (Verify).

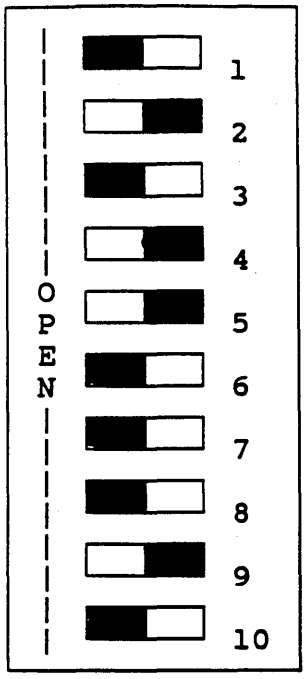
12. After formatting (ILD 1) and assigning alternates (ILD 4), run ILD B option 50X where X equals the drive number (see section 5.4, Offline Diagnostics). Monitor the thumbwheel switch 4D8 to watch that the diagnostic sequentially writes and reads every cylinder on the drive. When the random mode has started, terminate the ILD (if desired).

13. See section 5.4 to Write Manufacturing Data (4EX). When this step has been completed, the drive is ready for use.



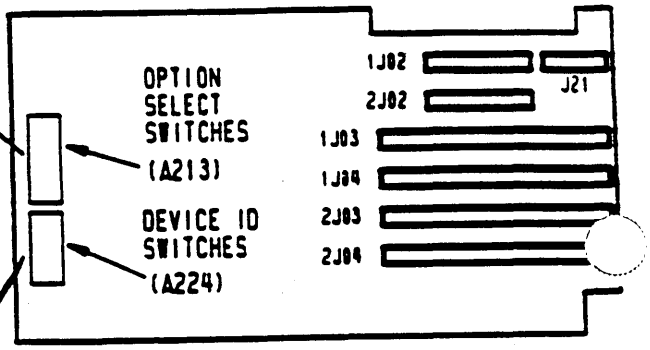
NOTES: *The shroud covers the space between the bottom of the drives and the top of the power supplies.*
1 - These screws attach the drive directly to the tray.
2 - These screws attach the bracket to the tray.
3 - These screws attach the power supply (or the drive) to the power supply (or drive) bracket.
4 - These screws attach the power supply bracket to the tray.
5 - These screws attach the locking hold-down brackets mounted across the front of the drive tray.

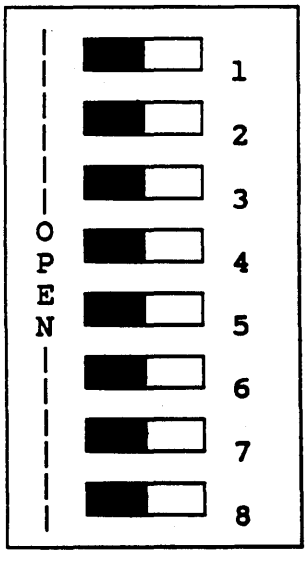
Figure 10-9
Drive Tray containing Two Disk Drives and Two Power Supplies (Top View)



A213

Switches 2,4,5, and 9 are ON (closed).

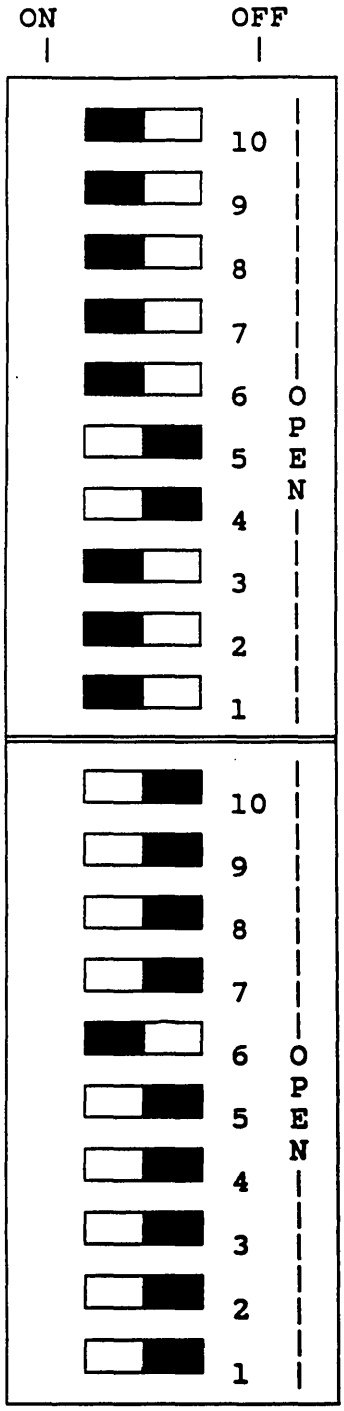




A224

All switches are OFF (open).

Figure 10-10
Disk Drive I/O Board Switches



For a type 3 control board:

Switches 10,9,8,7,6,3,2, and 1 are ON (closed).

Switches 5 and 4 are OFF (open).

Switch 6 is ON (closed).

Switches 10,9,8,7,5,4,3,2, and 1 are OFF (open).

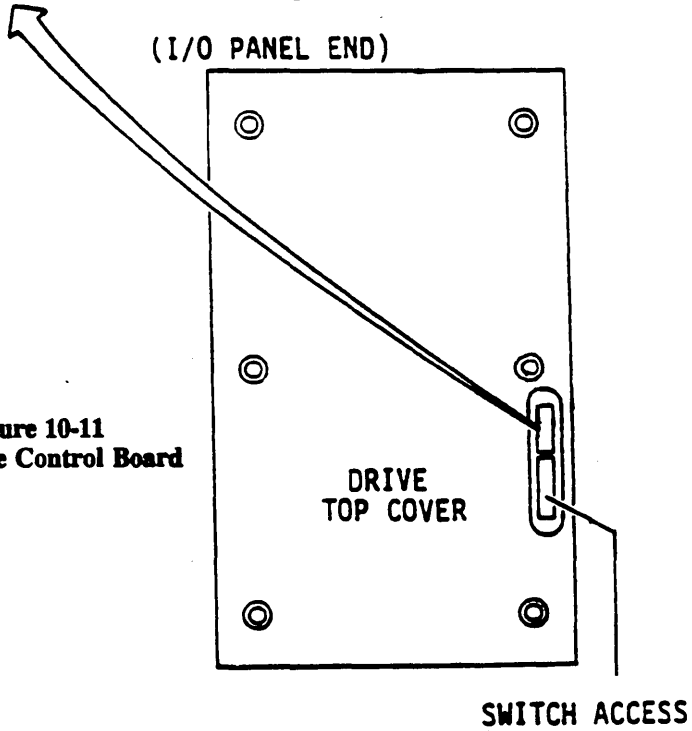


Figure 10-11
Disk Drive Control Board

Table 10-1
Switch Settings for Logical Drive Address

Drive	2^3	2^2	2^1	2^0
0	ON	ON	ON	ON
1	ON	ON	ON	OFF
2	ON	ON	OFF	ON
3	ON	ON	OFF	OFF
4	ON	OFF	ON	ON
5	ON	OFF	ON	OFF
6	ON	OFF	OFF	ON
7	ON	OFF	OFF	OFF
8	OFF	ON	ON	ON
9	OFF	ON	ON	OFF
10	OFF	ON	OFF	ON
11	OFF	ON	OFF	OFF
12	OFF	OFF	ON	ON
13	OFF	OFF	ON	OFF
14	OFF	OFF	OFF	ON
15	OFF	OFF	OFF	OFF

10.15 OCP Control Panel Assembly

The OCP control panel assembly is made up of six smaller assemblies:

- o Display panel
- o LED PCBA
- o Keypad
- o Drive control PCBA
- o OCP PCBA (on the rear cover of the OCP control panel assembly)
- o 8085 PCBA (plugged into the OCP PCBA)

The following procedures explain how to remove the entire OCP control panel assembly, as well as how to remove each of the six assemblies individually. (You would only replace the entire assembly if the front panel had been damaged.)

Entire Panel

1. Disconnect the cable assemblies for each component as described in the "Individual components" section below.
2. Remove the four screws which secure the panel assembly to the mainframe.
3. Remove the panel assembly from the mainframe.
4. Reinstall in reverse order.

Individual components

8085 PCB Assembly

1. Power off the dual controller.
2. Carefully unplug and remove the 8085 from the OCP PCB assembly. (There are no cable connectors.)
3. To reinstall, plug the 8085 back into the OCP PCB assembly.

OCP PCB Assembly

1. Power off the dual controller.
2. Label and remove signal cables from the top and bottom rows of connectors.
3. Label and remove the four slip-on wires (+5 V and ground).
4. Cut any cable ties, if present and interfering.
5. Remove the four bottom screws which hold the board to the frame. (All screws should be removed from component side of the board.)
6. Support the board with one hand and remove the four top mounting screws.
7. Remove the board.
8. Reinstall in reverse order.

CAUTION: When opening OCP gate B, be careful not to pull cables from the LED board (located on gate A) connectors (J1, J2, J3, and J4).

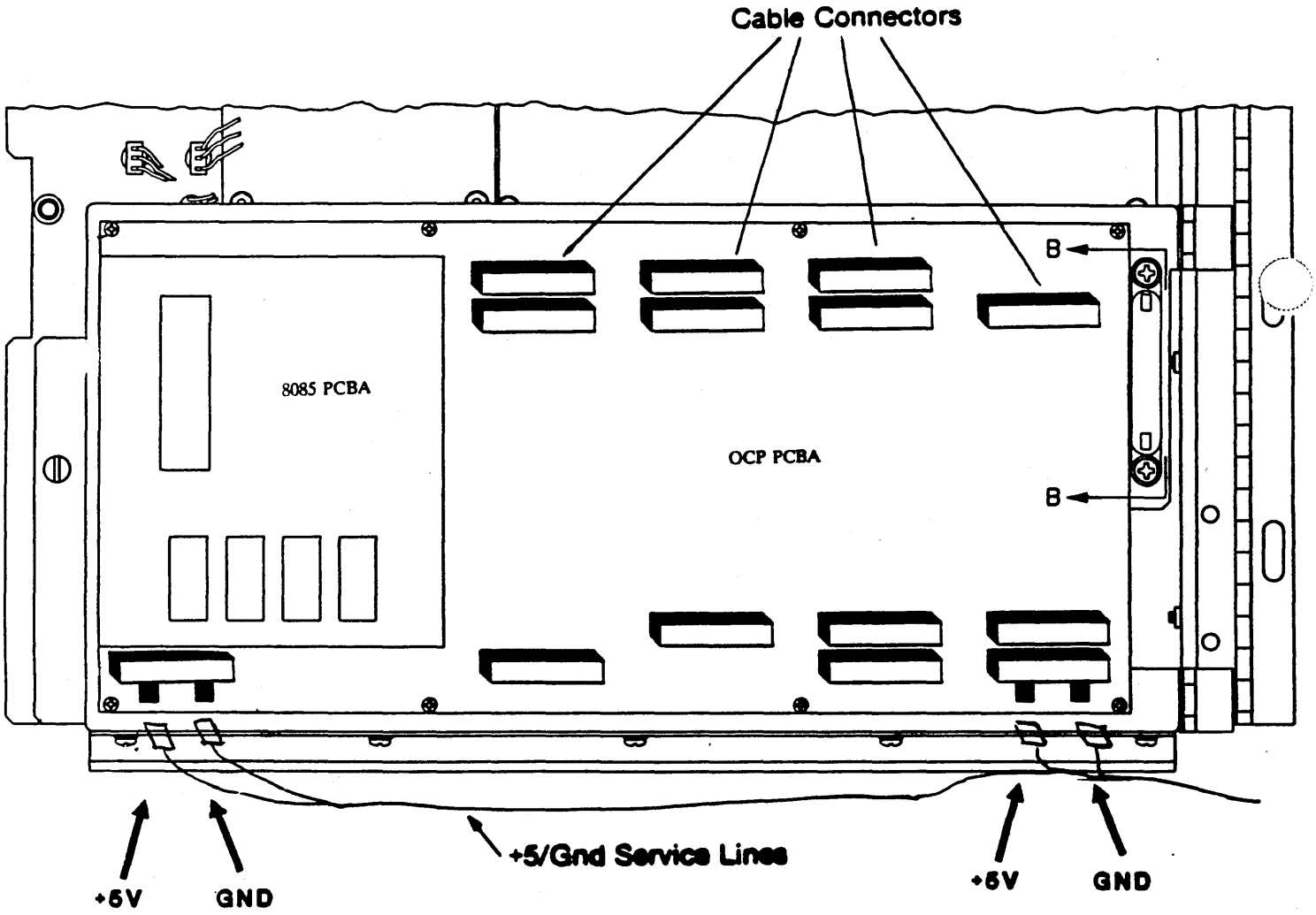


Figure 10-12
OCP Panel Assembly with Rear Cover

LED PCB Assembly

1. Power off the dual controller.
2. Loosen the captive screw at the left-hand side of the rear cover and then swing the cover out to your right.
3. Locate the LED assembly.
4. Label and unplug the four signal cable connectors from the LED assembly.
5. Label and remove the LED assembly 5V and ground slip-on connectors.
6. Remove the mounting nuts.
7. Remove the board.
8. Reinstall in reverse order.

Display Panel Assembly

1. Power off the dual controller.
2. Loosen the captive screw at the left-hand side of the rear cover and then swing the cover out to your right.
3. Locate the display panel assembly.
4. Label and unplug the display panel assembly signal connector.
5. Label and remove the display panel assembly 5V and ground slip-on connectors.
6. Remove the mounting nuts.
7. Remove the board.
8. Reinstall in reverse order.

Keypad Assembly

1. Power off the dual controller.
2. Loosen the captive screw at the left-hand side of the rear cover and then swing the cover out to your right.
3. Locate the keypad assembly.
4. Remove the cable connections.
5. Unplug the keypad assembly signal cable.
6. Remove the mounting nuts.
7. Remove the board.
8. Reinstall in reverse order.

Drive Control PCB Assembly

1. Power off the dual controller.
2. Loosen the captive screw at the left-hand side of the rear cover and then swing the cover out to your right.
3. Locate the drive control PCB assembly and remove the cable connections.
4. Remove the screws.
5. Remove the board.
6. Reinstall in reverse order.

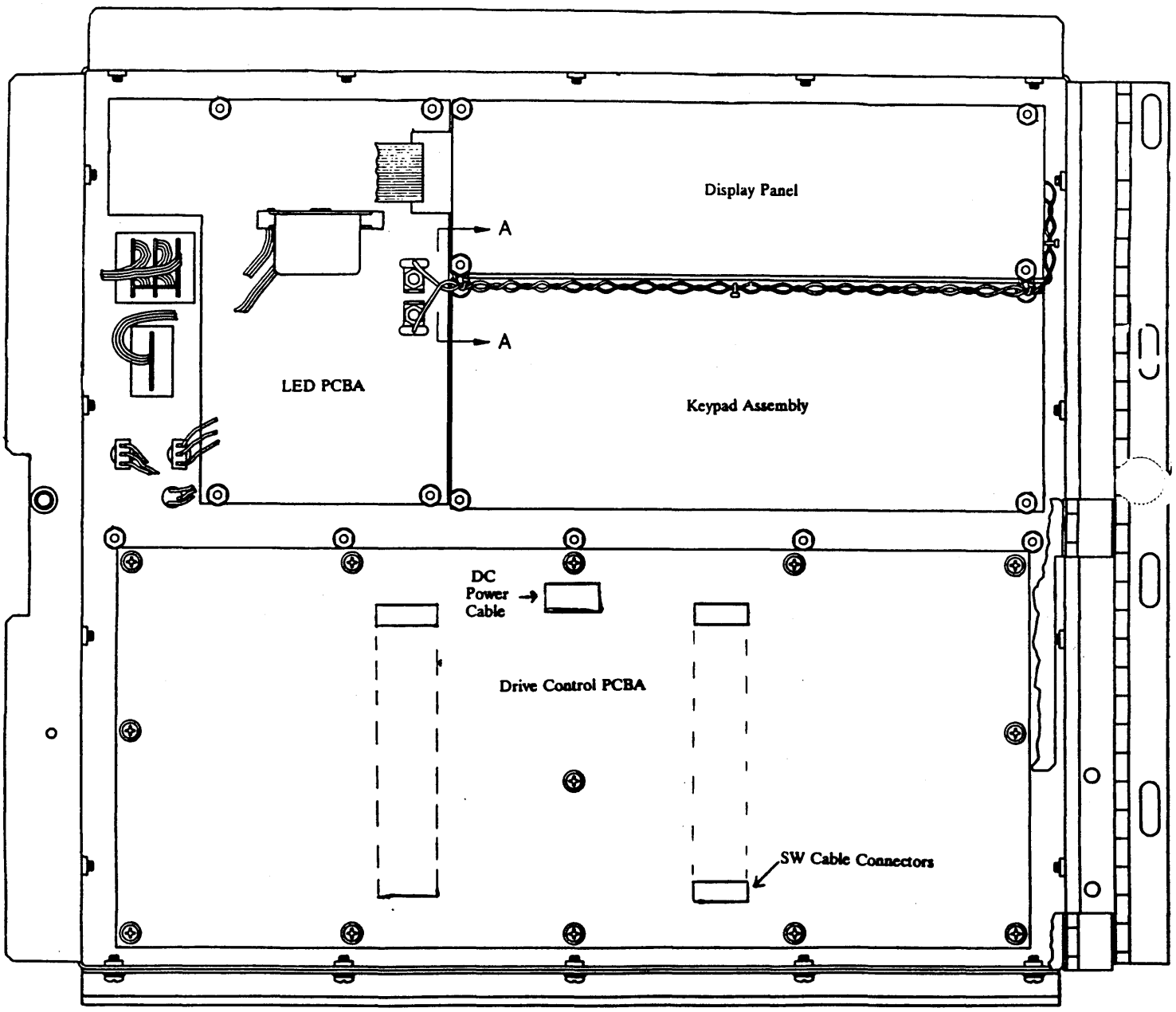


Figure 10-13
OCP Panel Assembly without Rear Cover

10.16 OCP Power Supply (+5 V)

The following procedures apply to the OCP power supply which is located on the power supply panel. The power supply panel is inside the right side of the cabinet, as you face the back of the 7100-30.

Figure 10-14 shows the power supplies which are located on the power supply panel. (See sections 10.17 and 10.18 for removal and replacement procedures for the controller power supplies on the power supply panel.)

1. Open the front door of the 7100-30 cabinet.

2. Turn off the AC power to the OCP power supply by switching off the appropriate breaker in the AC power box. (The AC power box is located at the lower left of the cabinet as you face the front of the 7100-30.)

3. Open the rear door of the cabinet; all remaining steps are performed at the rear of the cabinet.

4. Open the power supply panel by removing the five bolts securing the cover of the panel. Swing the panel open to the left.

5. Remove the power supply panel safety cover by removing the four screws which attach the cover to the power supplies.

6. Disconnect all wires leading to the OCP power supply.

7. The OCP power supply is attached to a bracket which is then attached to the power supply panel itself. To remove the power supply, you must first remove the bracket from the panel. To remove the bracket from the panel, remove the four screws which attach the bracket to the panel. (These screws are on the opposite side of the panel.) Remove the bracket with the OCP power supply still attached to it.

8. Remove the four screws which attach the power supply to the bracket and then remove the power supply.

9. Reinstall in reverse order.

10.17 +5 V Controller Power Supplies

The following procedures apply to the two +5 V controller power supplies (one for controller A and one for controller B) which are located on the power supply panel. The power supply panel is inside the right side of the cabinet, as you face the back of the 7100-30.

Figure 10-14 shows the power supplies which are located on the power supply panel. (See sections 10.16 and 10.18 for removal and replacement procedures for the other power supplies on the power supply panel.)

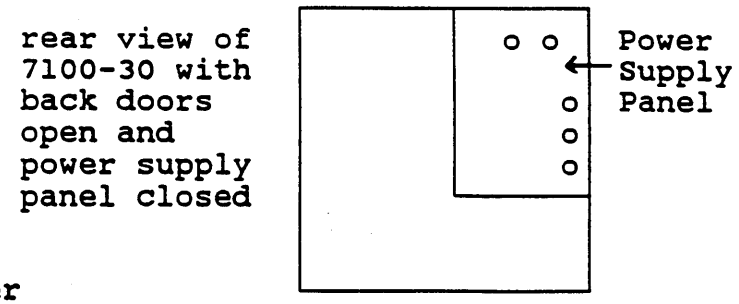
1. Open the front door of the 7100-30 cabinet.
2. Turn off the AC power to the power supply you are replacing by switching off the appropriate breaker in the AC power box. (The AC power box is located at the lower left of the cabinet as you face the front of the 7100-30.)
3. Open the rear door of the cabinet; all remaining steps are performed at the rear of the cabinet.
4. Open the power supply panel by removing the five bolts securing the cover of the panel. Swing the panel open to the left.
5. Remove the power supply panel safety cover by removing the four screws which hold the cover to the power supplies.
6. Remove the DC wires. (These are near the top of the power supply.)
7. From the opposite side of the power supply panel, remove the four screws which hold the power supply to the panel. Lift the power supply carefully because it is still attached to AC wires.
8. Remove the 10 screws which attach the cover to the power supply (five of these screws are on one side of the power supply and the remaining five are on the opposite side).
9. Disconnect the AC wires (these are at the bottom of the power supply) and remove the power supply entirely.
10. Reinstall in reverse order.

10.18 -5 V Controller Power Supplies

The following procedures apply to the two -5 V controller power supplies (one for controller A and one for controller B) which are located on the power supply panel. The power supply panel is inside the right side of the cabinet, as you face the back of the 7100-30.

Figure 10-14 shows the power supplies which are located on the power supply panel. (See sections 10.16 and 10.17 for removal and replacement procedures for the other power supplies on the power supply panel.)

1. Open the front door of the 7100-30 cabinet.
2. Turn off the AC power to the power supply you are replacing by switching off the appropriate breaker in the AC power box. (The AC power box is located at the lower left of the cabinet as you face the front of the 7100-30.)
3. Open the rear door of the cabinet; all remaining steps are performed at the rear of the cabinet.
4. Open the power supply panel by removing the five bolts securing the cover of the panel. Swing the panel open to the left.
5. Remove the power supply panel safety cover by removing the four screws which attach the cover to the power supplies.
6. Disconnect all wires leading to the power supply.
7. From the opposite side of the power supply panel, remove the four screws which hold the power supply to the panel and gently remove the power supply.
8. Reinstall in reverse order.



B = screw which holds the bracket to the panel
S = screw which holds the power supply to the panel or the bracket
--- = position of power supply panel safety cover

Figure 10-14
Power Supply Panel (Swung Open)

11. POWER SUPPLY ADJUSTMENT PROCEDURES

The following section provides procedures for adjusting the power supplies in the 7100-30. There are three types of power supplies in the 7100-30: two of these are mounted on the back of the power supply panel; the third is the separate power supply for each disk drive.

Figure 11-1 shows the power supplies which are located on the power supply panel. Adjustment procedures for these power supplies are described in sections 11.1 through 11.5. If you need detailed information regarding how to open the power supply panel to access these power supplies, see the appropriate power supply directions in section 10, "Removal and Replacement Procedures."

Section 11.6 describes the adjustment procedures for the separate power supply for each disk drive.

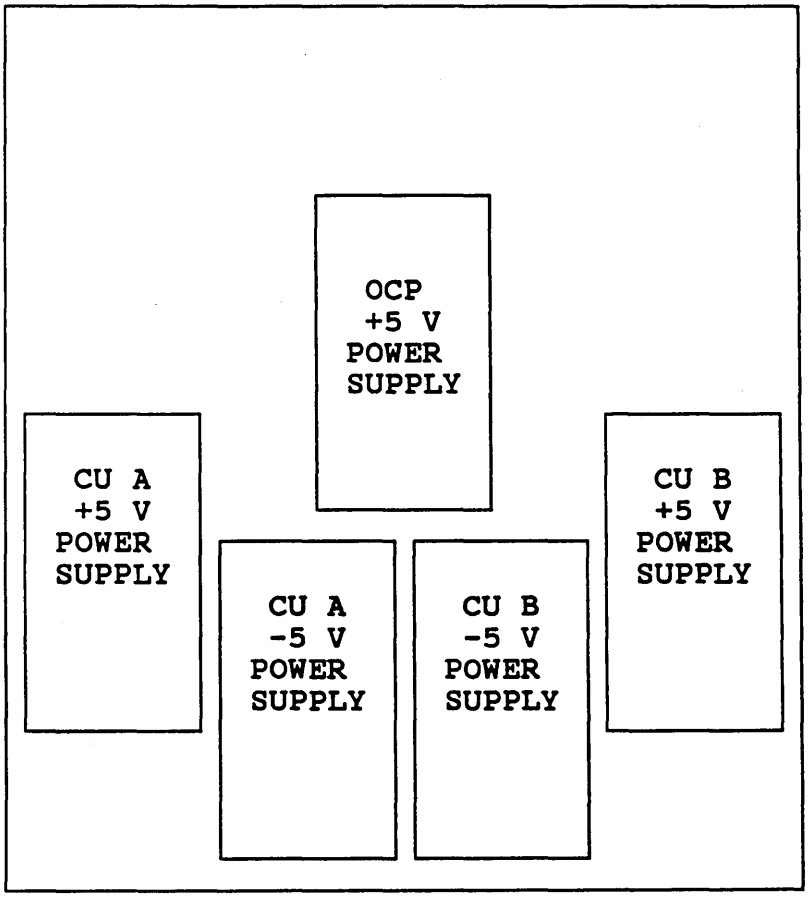


Figure 11-1
Location of Power Supplies on Power Supply Panel (Panel is Open)

11.1 Controller A (+5 V) Power Supply Adjustment Procedure

1. Measure the voltage at the backplane of the controller cardcage by connecting the positive lead of a digital voltmeter to terminal TP6 (on the controller cardcage backplane) and the meter common lead to TP3 (also on the controller cardcage backplane). See figure 11-2 for the location of these terminals.

2. Remove the power supply panel cover. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot (R35) inside the power supply until the voltage measured in step 1 is +5.05 V DC ± 1%. See figure 11-3 for the location of the adjust pot.

3. Differential check. Move the ground lead to the DC ground bus on the DC distribution panel. Use the positive lead to check for voltage differential at the following points:

   a. TP6 on the controller backplane (see figure 11-2)

   b. I/O cardcage +5 V lug on right side, when viewing the cable side of the backplane (see figure 11-8)

   c. VCC on CDCI boards for controller A (see figure 11-6)

   None of these measurements should differ from +5.05 V by more than 0.2 V. If any of these measurements differ from +5.05 V by more than 0.2 V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.2 Controller A (-5 V) Power Supply Adjustment Procedure

1. Connect the positive lead of a digital voltmeter to one of the controller A (-5 V) lugs on the DC distribution block (see figure 11-4); connect the meter common lead to either of the ground bus bars on the DC distribution block.

2. Remove the power supply panel cover. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot (R29) inside the power supply until the voltage measured in step 1 is -5.10 V DC ± 1%. See figure 11-5 for the location of the adjust pot on -5 V power supplies.

3. Differential check. Leaving the ground lead in place, use the positive lead to check for voltage differential at the following points:

   a. -5 V DC terminal on controller A DC terminal block (see figure 11-4)

   b. I/O cardcage -5 V lug on right side, when viewing cable side of the backplane (see figure 11-8)

   c. expansion cardcage -5 V lug (see figure 11-7)

   None of these measurements should differ from -5.10 V by more than 0.3 V. If any of these measurements differ from -5.10 V by more than 0.3 V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.3 Controller B (+5 V) Power Supply Adjustment Procedure

1. Measure the voltage at the backplane of the controller cardcage by connecting the positive lead of a digital voltmeter to terminal TP4 (on the controller cardcage backplane) and the meter common lead to TP1 (also on the controller cardcage backplane). See figure 11-2 for the location of these terminals.

2. Remove the power supply panel cover. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot (R35) inside the power supply until the voltage measured in step 1 is +5.05 V DC ±1%. See figure 11-3 for the location of the adjust pot on the +5 V power supplies.

3. Differential check. Move the ground lead to the DC ground bus on the DC distribution panel. Use the positive lead to check for voltage differential at the following points:

   a. TP4 on the controller backplane (see figure 11-2)

   b. I/O cardcage +5 V lug on left side, when viewing the cable side of the backplane (see figure 11-8)

   c. VCC on CDCI boards for controller B (see figure 11-6)

   None of these measurements should differ from +5.05 V by more than 0.2 V. If any of these measurements differ from +5.05 V by more than 0.2 V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.4 Controller B (-5 V) Power Supply Adjustment Procedure

1. Connect the positive lead of a digital voltmeter to one of the controller B (-5 V) lugs on the DC distribution block (see figure 11-4); connect the meter common lead to any point on either of the ground bus bars on the DC distribution block.

2. Remove the power supply panel cover. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot inside the power supply until the voltage measured in step 1 is -5.10 V DC ± 1%. See figure 11-5 for location of adjust pot on -5 V power supplies.

3. Differential check. Leaving the ground lead in place, use the positive lead to check for voltage differential at the following points:

   a. -5 V DC terminal on controller B DC distribution block (see figure 11-4)

   b. I/O cardcage -5 V lug on left side, when viewing the cable side of the backplane (see figure 11-8)

   c. expansion cardcage -5 V lug (see figure 11-7)

   None of these measurements should differ from -5.10 V by more than 0.3 V. If any of these measurements differ from -5.10 V by more than 0.3V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.5 OCP (+5 V) Power Supply Adjustment Procedure

1. Measure the voltage at the OCP backplane test points. See figure 11-9.

2. Remove the power supply panel cover. Insert a plastic screwdriver into the adjust hole of the +5 V OCP power supply (see figure 11-5) and turn the adjust pot (R29) inside the OCP power supply until the voltage measured in step two is adjusted to +5.00 V (± 50 millivolts).

3. Differential check. Move the ground lead to the common ground distribution bar. Use the positive lead to check for voltage differential at the +5 V lugs on the OCP PCB and TP5 of the controller cardcage backplane. The measured voltage should not differ from the setup voltage of the +5 V adjustment made above by more than 0.2 V. If any discrepancies appear, check wiring for loose crimps or terminals, bad junctions or splices, and wrong wire size or wire connector size.

11.6 Disk Drive Power Supply Adjustment Procedure

Under normal conditions, there is no need to adjust the disk drive power supply because it is preadjusted and should arrive adjusted correctly. However, if you need to verify the adjustment, use the procedure below.

NOTE: *Disk drive power supplies are factory preset and cannot be adjusted in the field. If you find that any voltage you measure is outside the acceptable limits listed below, order a replacement part.*

J15 is the 13-pin connector located at the right front end of each disk drive. Using a digital voltmeter and pin 3 as the ground, verify that the following voltages are correct. (You need only check those which have entries under the "Acceptable Limits" heading.)

Pin	Voltage	Aceeptable Limits
1	+5 V high	+4.75 V to +5.25 V
2	+5 V sense	
3	ground (±5 V, -12 V)	
4	±5 V sense return	
5	-5 V high	-5.25 V to -4.75 V
6	-5 V sense	
7	-12 V high	-12.5 V to -11.5 V
8	+5 V power OK	+4 V to +6 V
9	key (There is no pin in this position of the connector.)	
10	ground (+24 V)	
11	ground (+24 V)	
12	+24 V high	+23 V to +25 V
13	+24 V high	+23 V to +25 V

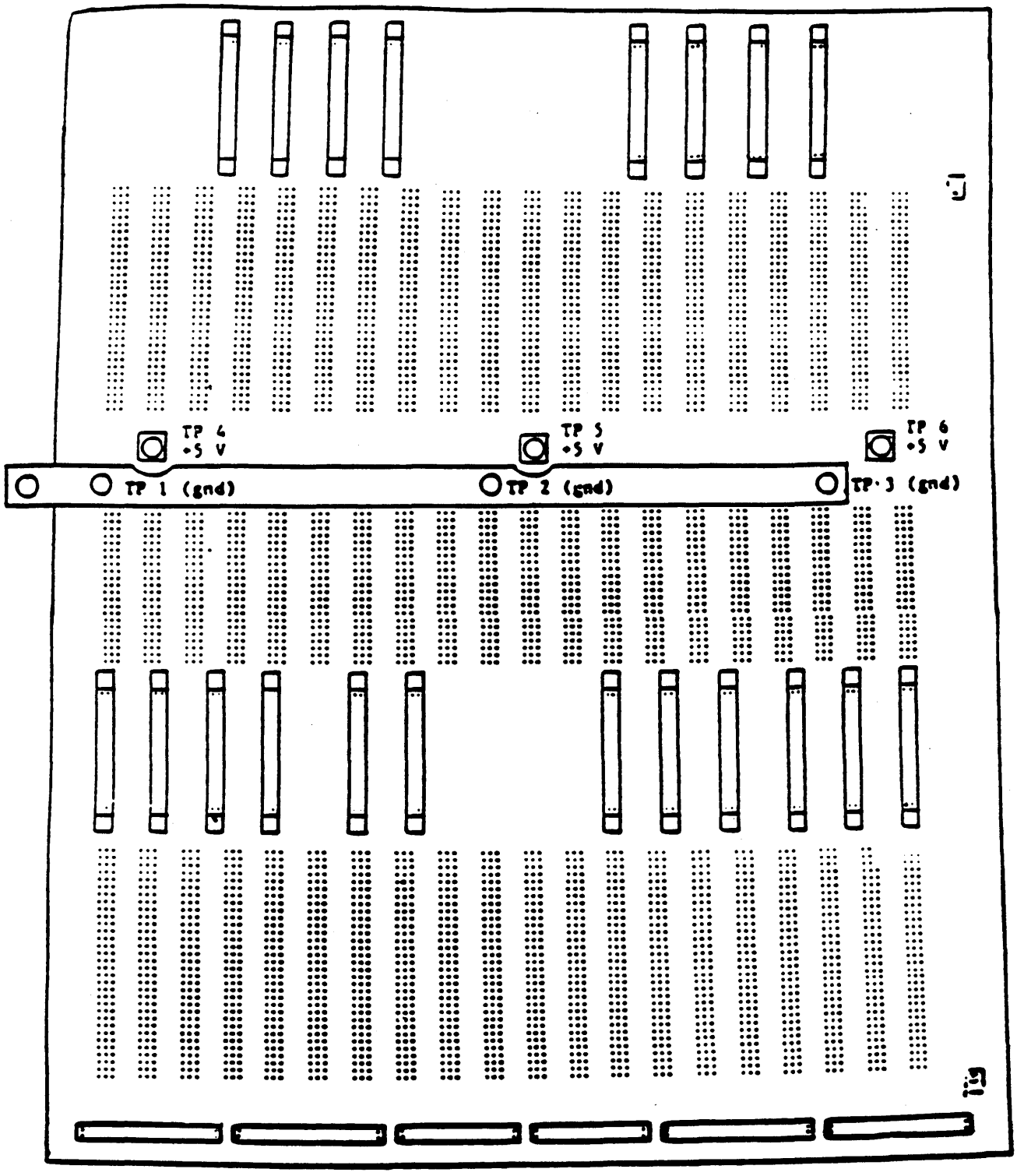


Figure 11-2
Controller Backplane

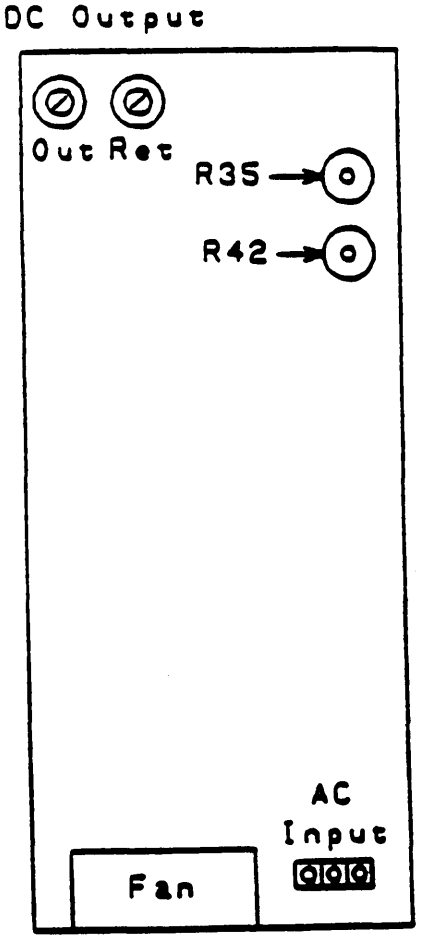


Figure 11-3
Location of Adjust Pot
on Controller A and B +5V Power Supplies

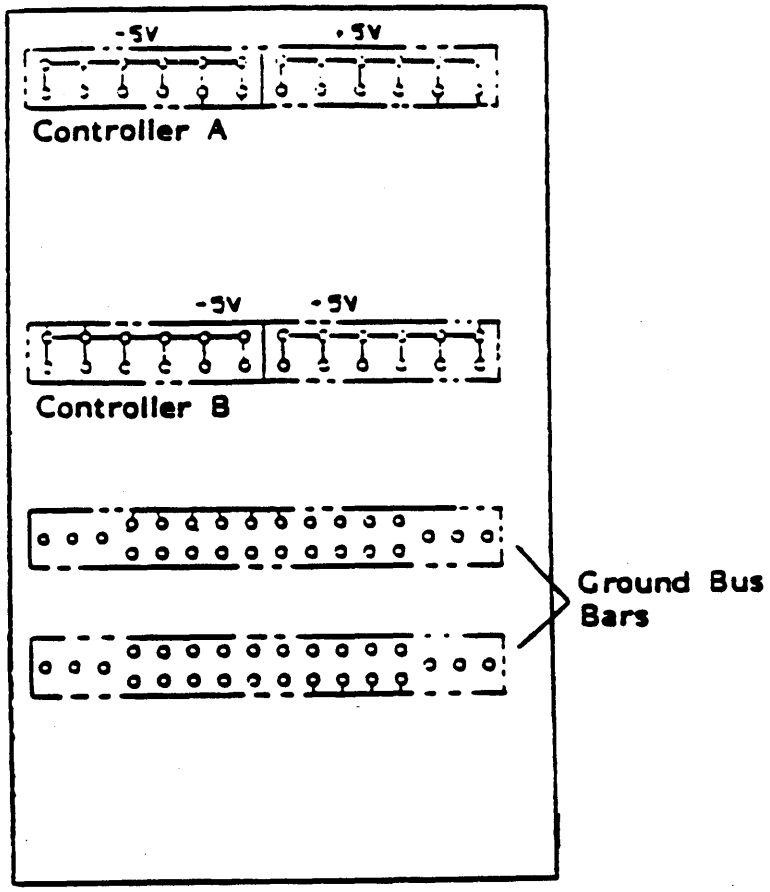


Figure 11-4
DC Distribution Block

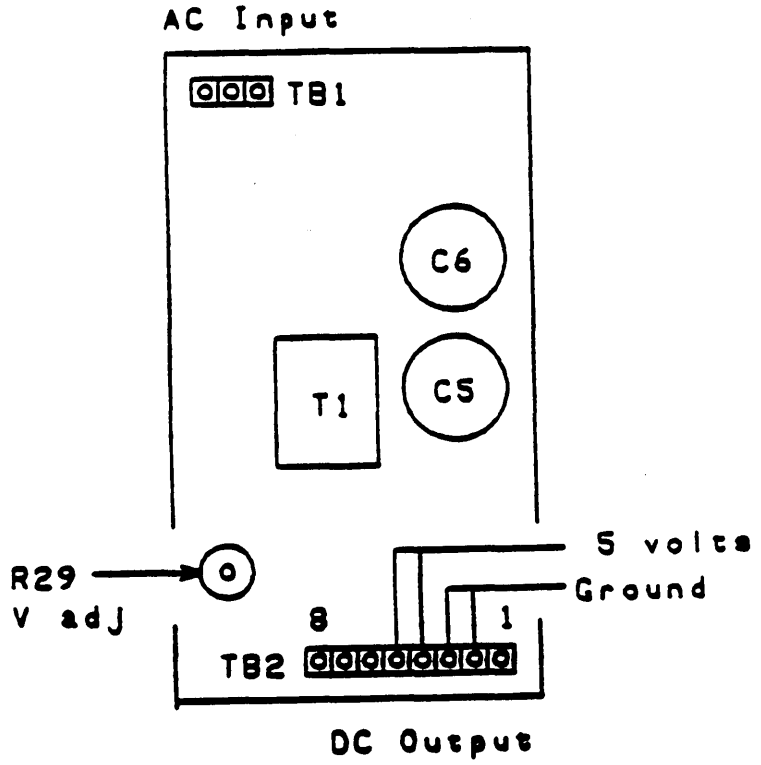


Figure 11-5
Location of Adjust Pot
on Controller A and B -5V Power Supplies and OCP +5V Power Supply

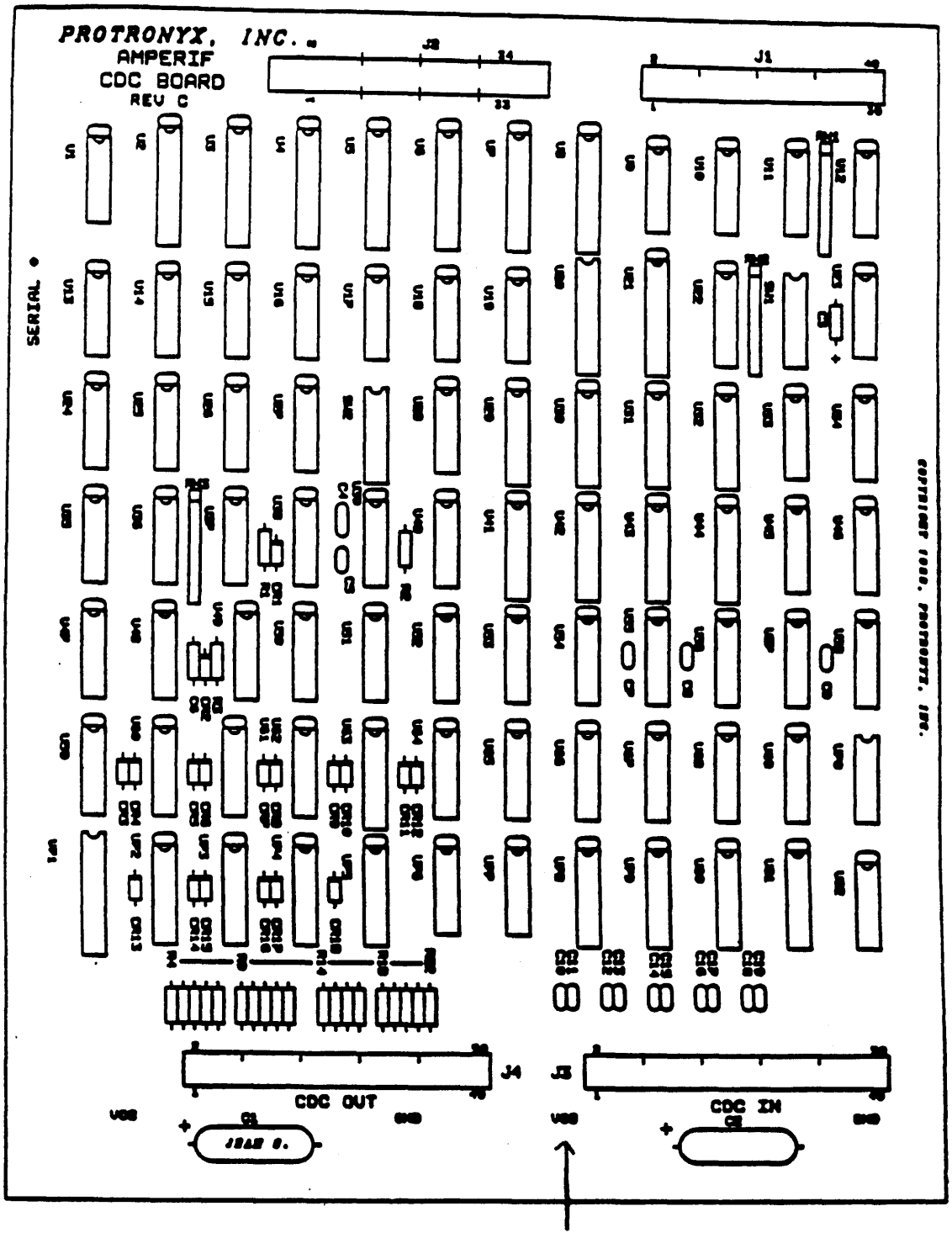


Figure 11-6
CDCI Board

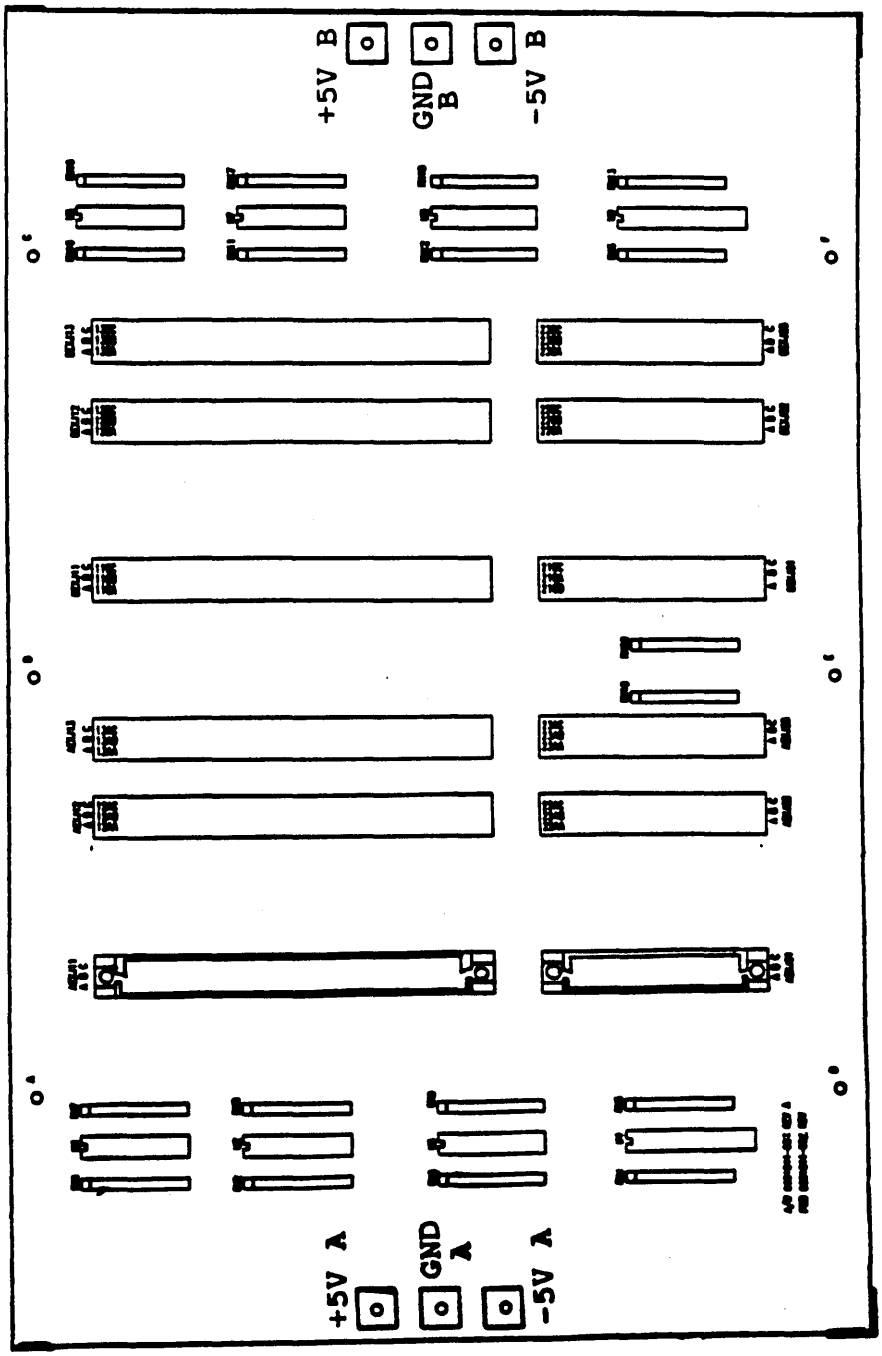


Figure 11-7
Expansion Cardcage Backplane

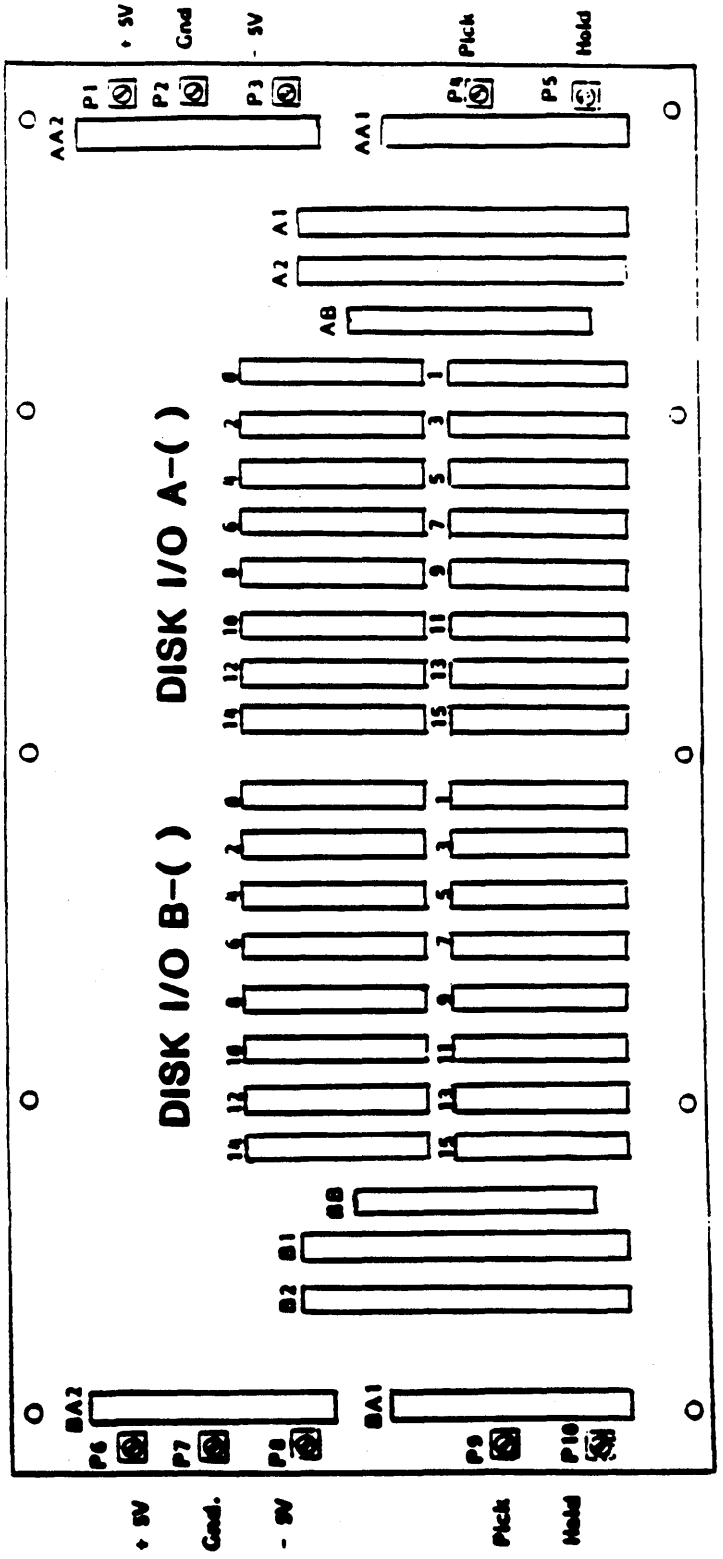


Figure 11-8
Disk Drive I/O Cardcage Backplane (cable side)

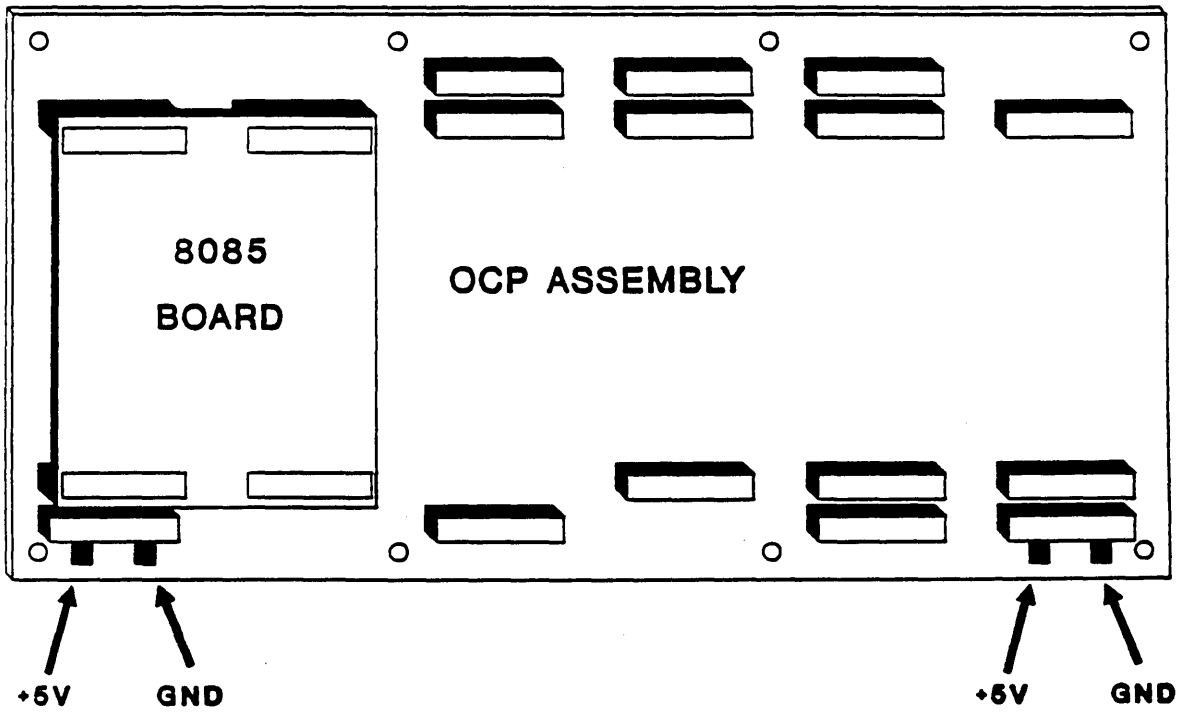


Figure 11-9
OCP Backplane Test Points

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12. EQUIPMENT INSTALLATION PROCEDURES

Use the following procedures to prepare your site for an installation and to do the installation.

12.1 Preinstallation

This section provides information required to prepare a site for the installation of Amperif equipment. Equipment clearance, air conditioning, and power and grounding requirements are discussed.

12.1.1 Equipment Placement

Computer Room Installation. A false floor is required due to a large I/O cable bend radius. The area must be large enough to accommodate the equipment and to allow working room around it: about three feet in front and three feet in back of the system. Consideration must also be given to equipment cable-length restrictions and obstructions such as walls, pillars, aisles, and doors that restrict the position of equipment.

Air Conditioning. Amperif's equipment must be placed in an air-conditioned environment suitable for proper operation of computer equipment. The air conditioning should provide proper cooling during maximum seasonal conditions. A backup system may be appropriate in areas where air conditioning is not stable. To determine the approximate number of tons of air conditioning required, take the total Btu/hour value of the equipment and divide that number by 12,000. For example, assume your system uses 7 KVAs of power and generates 24,000 Btus of heat. Therefore, 24,000 Btus divided by 12,000 equals 2,000 lbs, indicating 1 ton of air conditioning is required.

Equipment Environment. Although the exact temperature and humidity requirements will vary for individual components, all of Amperif's equipment can operate satisfactorily in an environment with a temperature range of 50°F to 90°F and a humidity range of 20% to 80% noncondensing. These operating limits are the conditions for the air supply where it enters the cabinet.

Input Power Requirements. The dual controller and disk drives require the following power:

208-240 Volts, 60 Hz, three phase, four wire: 3 power and a ground
220/380 Wye, 50 Hz, three phase, five wire: neutral and a ground
240/415 Wye, 50 Hz, three phase, five wire: neutral and a ground

Variations in voltage for all of these systems should not exceed the following:

Long-term nominal: +6%, -10%
Frequency variation must not exceed 0.5%
Harmonic content must not exceed 5%

Power Distribution. Equipment should be supplied from a dedicated branch circuit. If the equipment is located in a noisy electromagnetic interference area, isolation transformers should be considered. (An isolation transformer has shielded primary and secondary windings in order to minimize line noise.) The customer must provide one or more circuit breaker panels for the distribution of AC power and ground to the Amperif equipment.

- Power wiring should run through a metallic conduit that serves as a shield against electrical interference. Each run should be as short as possible.

- Each power run must terminate in a suitable receptacle which is located within 15 feet (the length of the power cord) of the equipment or cabinet it serves. For 60 Hz systems, a NEMA L15-20 receptacle is required. For 50 Hz systems, the plug of the AC power cord is customer-supplied and must be an approved-type locking connector.

- Power wiring must be routed as far as possible from the signal cables.

A dimensional illustration of the 7100-30 cabinet is provided in figure 12-1. For system specifications and power and voltage requirements, see section 4 of this manual.

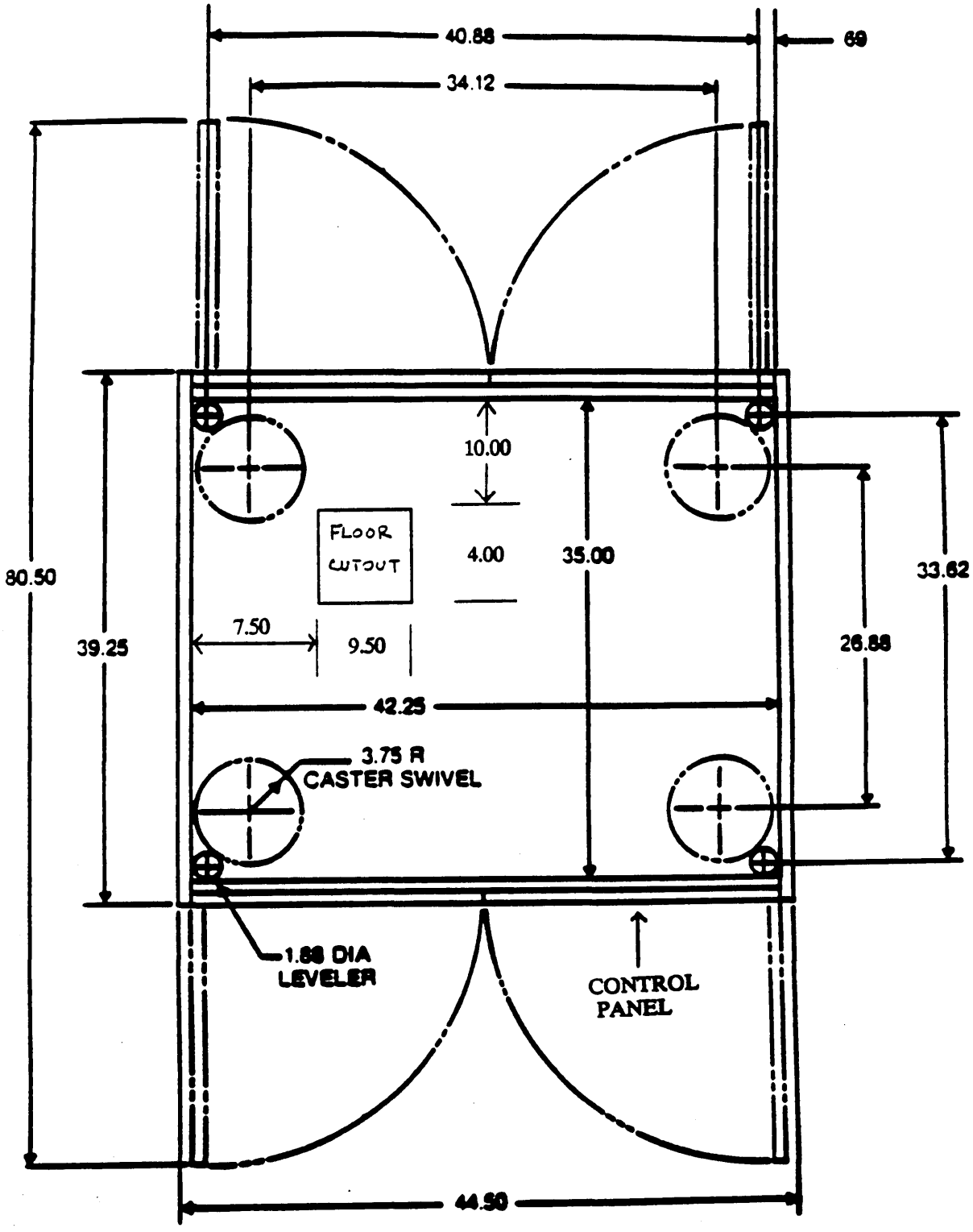


Figure 12-1
Dimensional Illustration of 7100-30 Mass Storage System

12.1.2 Equipment Unpacking Procedures

Unpacking

1. Remove all shipping materials.

   a. Undo all metal band strapping that secures the equipment and the attached ramp in place. Lower the ramp to floor level. Remove the plastic and then attach the ramp to the pallet with the included hinge bolts.

   b. Remove all plastic or cardboard protectors that protected the equipment during shipment.

   c. Remove the stretch wrap cellophane that held the eight cardboard corner protectors in place; retain the protectors.

2. Remove and retain shipping documentation.

   a. Locate and retain the Quality Assurance documentation package that was shipped with the equipment. Verify that the serial number of the documentation package matches the serial number of the unit.

   b. Verify that the following additional documents have also been shipped:

      - o AC wiring diagrams
      - o DC wiring diagrams
      - o interconnecting diagrams
      - o maintenance handbook (The handbook includes the *7100-30 Maintenance Manual* and the *User's Manual for Disk Drives*.)

3. Follow these procedures to remove the unit from the pallet:

   a. Remove the eight 9/16-inch bolts that hold the four retaining brackets in place. These brackets surround the four leveling pads which are part of the equipment: the brackets and pads secure the equipment to the pallet.

   b. Turn the leveling footpads until they are completely recessed into the equipment.

   c. Remove the four 9/16-inch bolts that secure the two wooden wheel block assemblies. Slide the block assemblies out from under the equipment.

   d. Use the attached ramp to roll the unit onto the floor and off the pallet.

   NOTE: *If the equipment is to be shipped, retain the shipping pallet along with all the hardware.*

4. Open all covers and doors.

   a. Remove all packing material and boxes.

   b. Remove the two 7/16-inch shipping bolts on the power supply door.

   c. Cut tie-wraps on cables that have been coiled and restrained within the unit for shipping purposes.

General Inspection

1. Check all shock watches which are affixed to the disk drives. If any drive sustained a severe shock in transit, the tube in the shock watch will be red. If the tube is red, the unit may have to be replaced.

   NOTE: *If shipping brackets are to be removed from the disk drives, retain them for future use.*

2. Check all ribbon cable connections for secure seating and all DC wiring screw lugs for tightness. Also check major mechanical hardware for misalignment which may have occurred during transit. Remove cardcage cover plates and check seating of all printed circuit boards.

3. Check the equipment to be sure all FCO tags, serial number plates, and UL approval stickers are attached.

4. Inspect equipment for cosmetic shipping damage and broken or missing hardware.

Equipment Inventory

1. Ensure equipment configuration matches the Quality Assurance checksheet in the documentation package shipped with the system.

2. Verify that all I/O cables, grounding cables, lugs, etc., have been received. (See documentation package for cable lengths, number of cables, etc., required.)

3. Remove the covers of the controller boards in the left front of the system and ensure the serial numbers on the boards match those on the quality assurance checksheet. Similarly, check the disk drive I/O boards at the top left rear corner of the system.

4. Reseat all controller boards and disk drive I/O boards.

5. Verify that configuration options and jumpers are configured according to specifications. See section 6 of this manual for this information.

12.1.3 Equipment Packing Procedures

1. Collect the following documentation, secure it in a packet, and attach the packet within the equipment.

   - o Quality Assurance documentation.
     Be sure to collect all the documents that were shipped with the equipment. Verify that the documentation serial number matches that of the equipment.

   - o All log information that was maintained on the unit.
     This includes FCO cards, feature updates, and equipment enhancements, for example.

   - o Technical documentation to be sent with the equipment.

2. Secure all cable assemblies that are to ship with the equipment; coil and tie-wrap the AC power cord within the unit.

3. Secure access doors.

   a. Secure the power supply door with the two 7/16-inch shipping bolts.

   b. Make sure that cardcage cover plates are in place.

   c. Verify that the frame to logic ground shorting strap is installed for shipping.

   d. Make sure that disk drive shipping brackets are installed.

   e. Close and lock the front and rear doors.

4. Secure equipment to the shipping pallet.

   a. Make sure that when equipment is rolled onto the pallet, the front of the unit will face the center of gravity mark on the pallet.

   b. Rotate the leveling pads until they are recessed into the equipment.

   c. Roll the equipment onto the pallet via the attached ramp.

   CAUTION: This is a heavy unit; at least four people should be available to do this.

   d. Use the shipping hardware that was retained upon initial installation (or ordered from Amperif) to slide the wooden wheel block assemblies under the equipment until they are against the wheels and lined up with the bolt holes. Use the four 9/16-inch bolts to secure the assemblies.

5. Add protective wrapping.

   a. Attach center of gravity stickers/indicators, "cut along arrow" sticker, and "front" label at the correct locations. See figure 12-2.

   b. Attach the eight cardboard corner protectors.

   c. Place the top plastic sheet cover over the unit so there is at least six inches of overhang.

   d. Wrap the stretch plastic wrap around the unit until the entire unit has at least two full wraps. Be sure that the stretch wrap extends at least four inches over the top. See figure 12-3.

e. Remove the hinges that attach the loading ramp to the pallet and store the ramp up against the equipment. Use bubble wrap or cardboard protectors between the ramp and the equipment. Use the stretch wrap plastic to secure the ramp.

f. Attach the shipping documentation envelope, the shipping information label, and both the large and small caution labels at the correct locations. See figure 12-2.

6. Band wrap the equipment to the pallet.

a. Run two lengths of metal shipping band under the pallet, through the cutouts provided, and then over the equipment. The bands should cross from the front to the back of the equipment.

b. Tighten the metal bands using the band ratchet tool. While holding the bands with this tool, use the crimping tool to crimp on the remaining brackets. The unit is now ready for pickup.

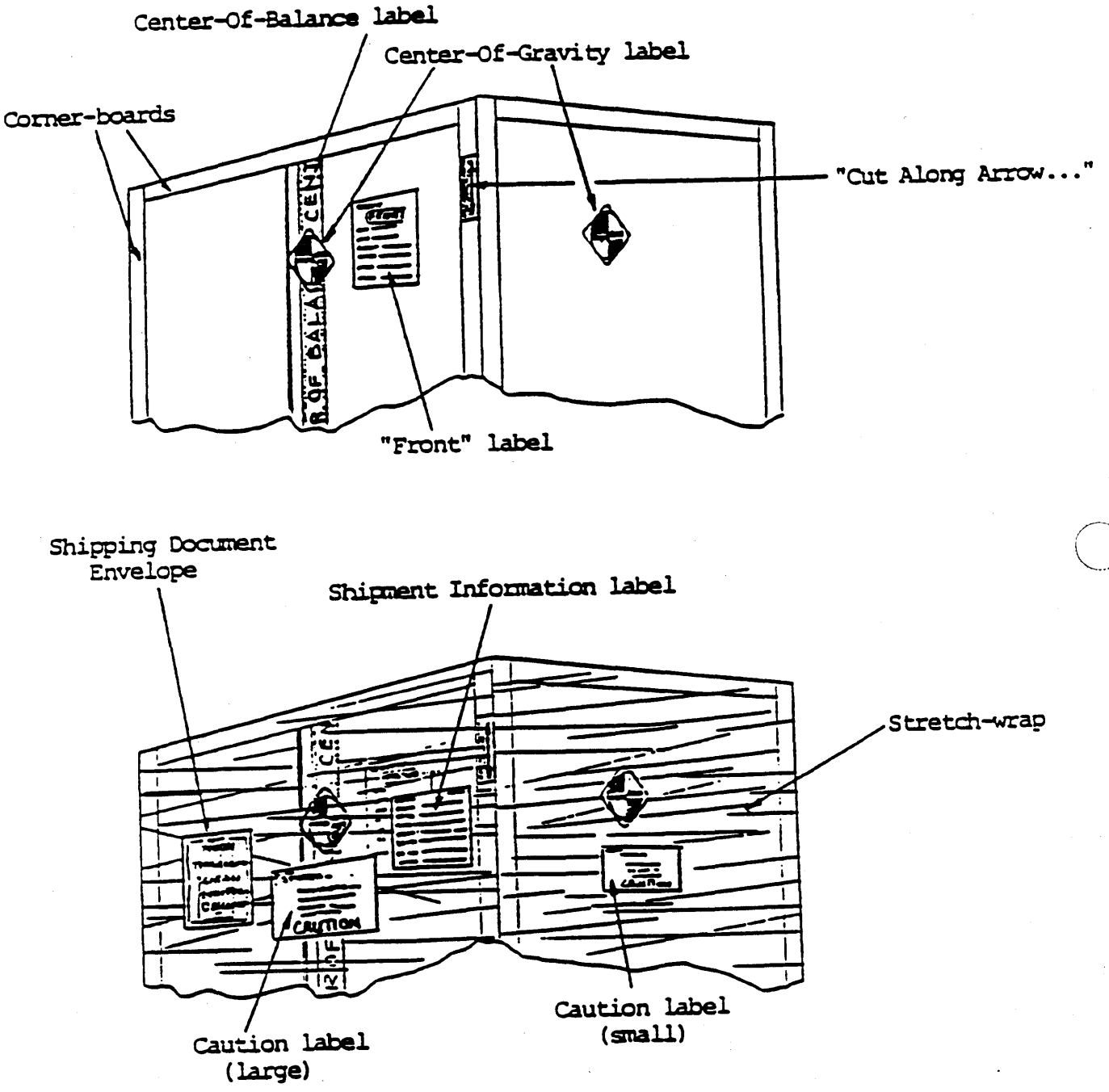
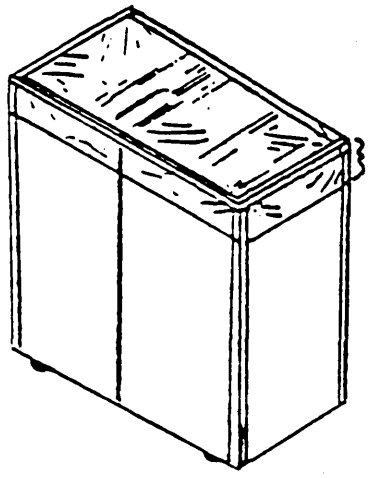
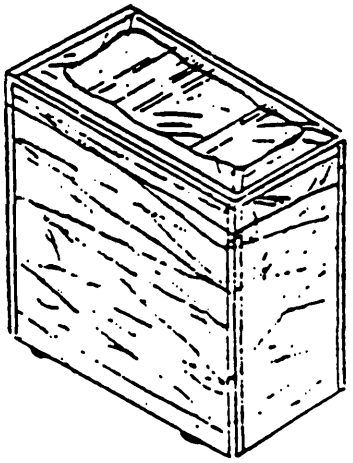
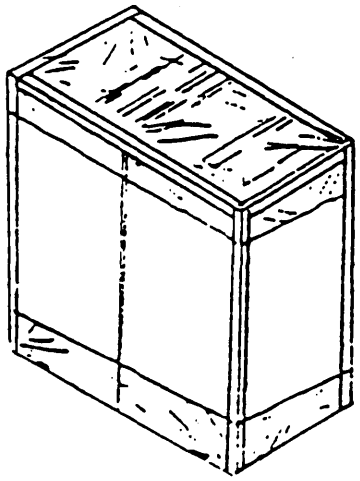


Figure 12-2
Label Location

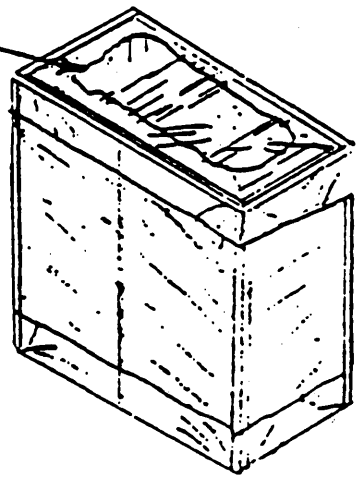


Top sheet cover.
minimum of 6" of
film overhang

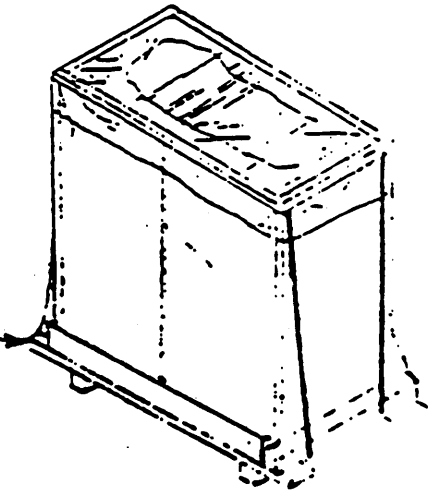




Minumum of 4" of film
over the top.



Bottom sheet application
if shipping spec requires
full enclosure.
Note: Desiccant must be
included.



stretch wrap shall
cover part of skid

Figure 12-3
Stretch Wrap Application

12.2 Installation of the 7100-30 Cabinet

This section describes the procedures for installing the 7100-30. These procedures include verifying that logic ground to frame ground is open, connecting logic ground to system ground, and making I/O connections between the 7100-30 and the host.

12.2.1 Logic Ground to Frame Ground Check

Remove the logic to frame ground shorting wire at the rear of the system. Using a VOM, verify that logic ground to frame ground is open. Logic ground may be referenced at the logic ground lug located on the DC voltage distribution panel in the rear middle portion of the 7100-30 cabinet (see figure 12-4). Frame ground may be referenced at any unpainted metallic point on the 7100-30 cabinet frame. A good choice would be the I/O connector mounting bracket.

12.2.2 Logic Ground Connections

Connect logic ground from controller logic ground lug to system ground.

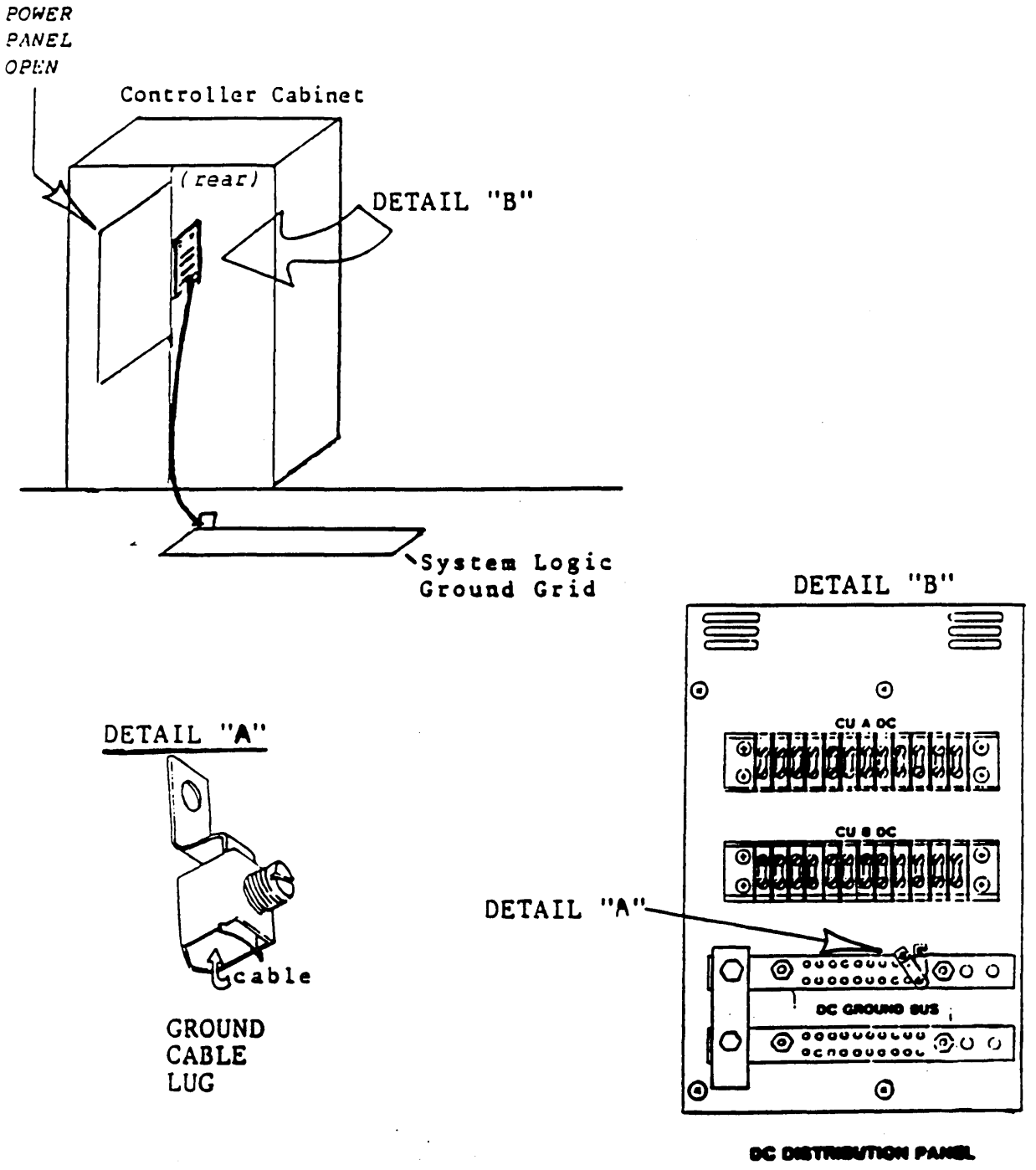


Figure 12-4
System Grounding Detail

12.2.3 I/O Connections

Verify system I/O path configuration with the customer. Label the I/O cables and then run them from the 7100-30 cabinet to the CDC I/O cabinets. Labeling them first ensures proper connection and provides a future reference should they be disconected for maintenance purposes. Cables should be labeled as to whether they connect through controller A or B and whether they connect through CDCI 0,1,2, or 3. Connect I/O cables to proper CDCI ports within the 7100-30 cabinet as illustrated in figure 12-5.

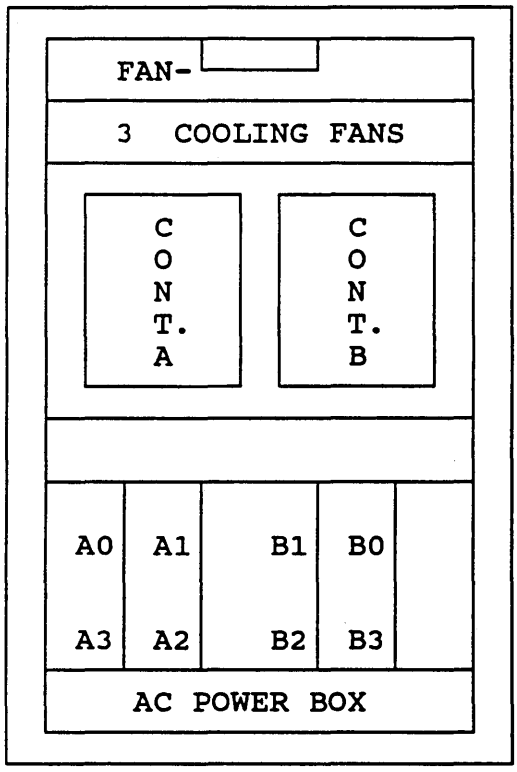

FAN-
3 COOLING FANS
C O N T. A
C O N T. B
CHANNEL INTERFACE BRACKET ASSEMBLY
A0 A1 B1 B0
A3 A2 B2 B3
AC POWER BOX
front view of inside of 7100-30 cabinet (left-hand side of the cabinet only)
four racks: each rack holds two CDCI boards
one rack holds two CDCI boards
CDCI Board
CDCI Board

Figure 12-5
Channel Interface Bracket Assembly with CDCI Boards

12.2.4 AC Power Connections

1. Verify that all circuit breakers are in the OFF position.
2. Measure the voltage at the receptacle and ensure that it is as specified under "Input Power Requirements" at the beginning of this section.
3. Remove the tie wraps securing the AC power cord and route the cord through the cutout in the system floor and out to the receptacle.
4. Plug AC power cord into proper receptacle.

NOTE: *For 50 Hz systems, the plug of the AC power cord is customer-supplied. It must be an approved-type locking connector.*

12.2.5 Equipment Leveling

After all logic ground, I/O and AC power connections are completed, level the controller cabinet by lowering the leveling pads, with the understanding that most of the weight of the system must remain on the wheels. Recheck equipment leveling after a few days and adjust, if necessary, for any settling that may have occurred.

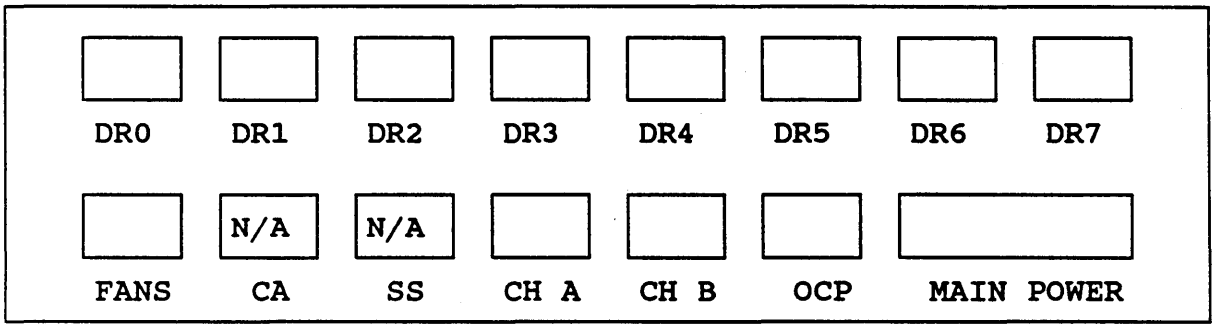
12.2.6 Power On Checks

1. Turn on the MAIN and FANS circuit breakers located in the AC power box. See figure 12-6.
2. Check that all fans inside and above the controller are operational.
3. Turn on the OCP, CHANNEL A, and CHANNEL B circuit breakers located in the AC power box in the order listed.
4. Using a voltmeter, check the following voltage measurements and adjust if necessary. See section 11 for adjustment procedures.

   a. +5V $\pm$ 5% on the OCP power supply measured between the center terminal on the DC ground bus bar and the controller backplane terminal TP5. See section 11.2.5 for adjustment procedure.

   b. +5V $\pm$ 5% on the CHA and CHB power supplies, measured between the left (CHB) terminal on the DC ground bus bar and the TP4 terminal on the controller backplane, and between the right (CHA) terminal on the DC ground bus bar and the TP6 terminal on the controller backplane. -5V $\pm$ 5% measured at the CDCI board of the disk drive I/O cardcage.

   d. +5V $\pm$ 5% ripple test on OCP power supply and on CHA and CHB power supplies measured at locations in steps b and c above.



NOTES:

DR0 controls drives 0 and 1.
DR1 controls drives 2 and 3.
DR2 controls drives 4 and 5.
DR3 controls drives 6 and 7.
DR4 controls drives 8 and 9.
DR5 controls drives 10 and 11.
DR6 controls drives 12 and 13.
DR7 controls drives 14 and 15.
CA and SS are nonfunctional in the 7100-30.

Figure 12-6
AC Power Box

12.3 System Initialization

The following two sections provide procedures for initializing the controllers and disk drives. The third section provides procedures for verifying that alternate tracks have been assigned to drives.

12.3.1 Initialize Controllers

1. Turn on all circuit breakers on power distribution panel behind the cabinet.
2. At the OCP keypad press **PROGM 4** and initialize both controllers (see section 5.2.18). Make sure **CHANNEL READY** appears at the OCP display.
3. Initialize the OCP. See section 5.2.20 for instructions.

12.3.2 Initialize Disk Drives

NOTE: *Verify that the release timer in the drive switches has been set.*

1. Turn on all circuit breakers for drives in the 7100-30 cabinet.
2. Power up drives at front panel by pressing START switches. Make sure each drive is ready (READY light appears on drive control panel) before proceeding to the next one. Drives should already be formatted from the factory.
3. Run a Read Data (ILD B code 2EX) to all drives from both controllers, as described in section 5.2.28. Run this ILD to all cylinders and all heads.
4. To verify headers, load MODE 1 before performing any seeks.
5. Run an Oscillating Seek (ILD 5) to all drives from both controllers, as described in section 5.2.30.
6. Run a Random Seek (ILD 6) to all drives from both controllers, as described in section 5.2.31.
7. Run a Sequential Seek (ILD 7) to all drives from both controllers, as described in section 5.2.32.

12.3.3 Verify that Alternate Tracks Have Been Assigned to Drives

Verify alternate tracks by performing the ILD 3 procedure outlined in section 5.2.29.

12.4 OCP Offline Checkout/Testing

This section describes how to verify that the operator control panel (OCP) is working properly. It is not necessary to go through the entire procedure when performing the functions in this section. Just perform the first two or three instructions to make sure the OCP and keypad are functioning correctly.

This section provides only a quick reference of the DISP, LOAD, PROGM and ILD functions.

12.4.1 Display/Load Functions

The DISP or LOAD key specifies a particular register, data, status or message which may be displayed at the OCP or loaded into the system. To check the following load and display functions, press the DISP or LOAD key and then press the appropriate function key number.

Function Key	Description
0/TOD	Time of day
1/BUT	Backup time
2/INT	Interval time
3/DSW	Data switch register
4/TOG	Toggle switch register
5/PB	Push button register
6/PRS	Present unit status *
7/REQ	Requested unit status *
8/PASS	Password/clearance status
9/EVC	Event counter
A/BRK	Break point address
B/MODE	Mode register
C/PGM	Program display *
D/MSG	System message

* No LOAD function.

12.4.2 Program Functions

The PROGM key specifies a certain program to be performed. To check the following Program functions, press the PROGM key and then press the appropriate function key number.

Function Key	Description
0	Introduction routine
4	Initialize channel
8	Initialize OCP
9	Initialize RAM
A	8085 editor mode
C	Repeat XMC clear
E	Slow run mode
F	Single step mode

12.4.3 Inline Diagnostic (ILD) Functions

The ILD key specifies an inline diagnostic or operating function to be performed. To check the following inline diagnostic functions, press the ILD key and then press the appropriate function key number.

Function Key	Description
0	ILD halt
1	Format and verify drive
2	Verify drive
3	Verify one track
4	Alternate defective track
5	Oscillating seek
6	Random seek
7	Sequential seek
8	Clear disk drive ECC display

12.5 Offline Installation Testing

Once you have completed the ILD tests in section 12.4.2, perform the following procedures. (Additional information about these utilities is provided in section 5.4.)

1. Perform a Write and Read using hex function 50X where X is the device address.
2. Perform a Read Data using hex function 2EX where X is the device address.
3. Perform a Write Manufacture Data using hex function 4EX where X is the device address.

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13. PREVENTIVE MAINTENANCE

This section provides the recommended preventive maintenance procedures for a 7100-30 System. Since the 7100-30 is relatively maintenance-free, it requires minimal upkeep time.

13.1 Daily Checks

The following procedures tell you what checks you need to perform on a daily basis. There are separate checks for the controller and the disk drives.

13.1.1 Controller Checks

1. At the OCP keypad, press **DISP 6** to check the present drive states. Make sure all the drives are in their proper state.

2. At the OCP keypad, press **DISP 0** to check the time-of-day clock. Make sure the 7100-30 clock and the CDC host clock are in sync.

13.1.2 Disk Drive Checks

Check the disk ECC error logs (at display locations 431-436) and the daily system error reports. These reports indicate that a bad spot has been found on a drive. If the same error cylinder and head appear several times during the course of a week, schedule time to assign an alternate track for that area.

13.2 Quarterly Checks

The following procedures tell you what checks you need to perform on a quarterly basis. There are separate checks for the controller, the disk drives, and the OCP power supplies.

13.2.1 Controller Checks

1. Perform a visual check of the inside of the dual controller cabinet. Look for loose cables and cable harnesses.
2. Make sure fans are turning properly and that nothing is obstructing the fans.
3. Remove the fan cage (see section 10) and wipe the blades clean. Replace the fan cage after cleaning the fan blades.
4. Check all power supply voltages and adjust if necessary. See section 11 for these procedures.

13.2.2 Disk Drive Checks

1. Check for loose cables at the I/O section of the controller and the disk drives.
2. Check all drive fans for proper operation.
3. Check all power supply voltages and adjust if necessary. See section 11 for these procedures.

13.2.3 OCP Power Supply Checks

Check all power supply voltages and adjust if necessary. See section 11 for these procedures.

APPENDIX A: CDC CYBER CONSOLE COMMANDS

Descriptions of the following commands are included in this section:

- o System display commands
- o Dayfile commands
- o Job processing control commands
- o Equipment control commands
- o Subsystem control commands
- o System control commands
- o Memory entry commands
- o Channel control commands

DSD is an interpretive display driver; When a console operator is typing a command, DSD completes the command as soon as it recognizes enough characters to establish the uniqueness of the command. DSD does not accept or display invalid characters.

The system displays are selected by the command. An example follows:

xy. CR

where x and y represent the letter designations of the displays; x appears on the left and y appears on the right.

Letter	Description
A	Dayfile display. This is a chronological history of system operations. It includes the system display (A,. or A.), the account display (A,ACCOUNT FILE.), the error log display (A,ERROR LOG.), the operator message display (A,OPERATOR), and the job dayfile display (DAYFILE,jsn.).
B	System status display. This is the current status of all jobs assigned to control points. It includes the system status displays (B.O. and B,A.).
C,D	Central memory display. These are portions of the contents of central memory in five groups of four octal digits and their display code equivalents.
E	Equipment status display. This is the status of peripheral devices. It includes the equipment status table display (E,. or E.A.), the drive configuration display (E,C.), the family status display (E,F.), the drive status display (E,M.), the resource requests display (E,P.), and the tape status display (E,T.).
F,G	Central memory display. These are the portions of the contents of central memory in four groups of five octal digits and display code equivalents.
J	Individual job status display. Status of the specified job sequence name.
K	CPU programmable display. This is the dynamic operator/CPU program communication.
P	PP registers display. Current contents of PP registers or PPs active for a particular job.
Q	Queue status display. Status of active input and output queues in the queued file table. This includes all queues (Q.), input queue (Q,IN.), plot queue (Q,PL.), print queue (Q,PR.), punch queue (Q,PU.), or wait queue (Q,WT.).
R	Rollout queue status display. Current status of all executing jobs including those that the system has rolled out.

Letter	Description
T	Interactive status display (IAF). Status of interactive users.
W	System information display. Status of the system. Includes channel status (W,C.), request queues (W,Q.), resource information (W.R.), and miscellaneous parameters (W,M.).
Y	Monitor function display. List of all monitor function mnemonics and codes.
Z	Directory display. List of the latter designations and description of all DSD displays.

There are a few special first character entries which are explained below.

Character	Description
*	Alternates display control between DSD and another console program each time * key is pressed.
+	Advances left screen display. For E,Q,R,S,T, or W display, advances to the next page of display. For memory display (C,D,F, or G), advances display address by 40 octal locations.
-	Reverses left screen display. For E,Q,R,S,T, or W display, reverses to previous or first page of display. For memory display (E,D,F, or G), decrements display address by 40 octal locations.
(	Advances right screen as described for + key.
)	Reverses right screen as described for - key.
CR	Carriage return key. Sets repeat entry flag. Subsequent entry is processed, but not erased after completion. Flag is cleared by pressing left blank key.
left blank	Clears current keyboard entry and any resultant error messages.
BKSP	Deletes last character entered and clears error message if one exists.
CR	Initiates processing of command entered.

System Display Commands

Command	Description
m,jsn	Sets display m (C,D,F,G,J, or K) to display only information for job with job sequence number jsn.
xz,addr.	x = letter designation of a storage display (C,D,F, or G). z = type of display modification. 4 changes the entire display to display the memory contents beginning at location addr. 5 increments the display by addr locations. 6 decrements the display by addr locations.

Dayfile Commands

Command	Description
A.	Resets the A display to the beginning of the dayfile buffer.
A,.	Resets the A display to the system dayfile when the error log account dayfile, or a job dayfile is currently being displayed.
A,ACCOUNT FILE.	Displays the account dayfile buffer on the left screen.
A,ERROR LOG.	Displays the error log buffer on the left screen.
A,OPERATOR.	Displays system messages to the operator.
DAYFILE,jsn.	Displays the dayfile buffer for the job with job sequence name jsn.
LOG,ord.	Clears message ord from A,OPERATOR display.

Job Processing Control Commands

Command	Description
DROP,jsn.	Drops job with job sequence name jsn.
KILL, jsn.	Kills job with job sequence name jsn.
OVERRIDE,jsn.	Drops job with job sequence name jsn.
ROLLIN,jsn,L.	Allows job with job sequence name jsn to be scheduled to a control point. L is optional; if omitted, the job can be selected by the scheduler for rollout.
ROLLOUT,jsn.	Causes job with job sequence name jsn to be rolled out and remain rolled out until the operator rolls the job in via the ROLLIN command or terminates it via the DROP, KILL, or OVERRIDE command.
ROLLOUT,jsn,n.	Causes job with job sequence name jsn to be rolled out and remain rolled out for n scheduler cycles. When n scheduler cycles have elapsed, the job becomes eligible for scheduling.
GO,jsn.	Clears the pause and status flags for job with job sequence name jsn.

Equipment Control Commands

Command	Description
ASSIGN,jsn,est.	Assigns device with EST ordinal est to job with job sequence name js.
DOWN,CHcc	Discontinues use of channel cc for all I/O operations. If channel cc is the only channel available to a mass storage device, its use is not discontinued for that device.
DOWN,EQest.	Discontinues use of device with EST ordinal est for all channels.
OFF,est.	Logically turns off device with EST ordinal est.
ON,est.	Logically turns on device with EST ordinal est.
UNLOAD,est.	Physically unloads the magnetic tape on EST ordinal est or logically removes the removable mass storage device on EST ordinal est from the operating environment while the operator dismounts a tape or disk drive pack.
UP,CHcc	Reverses the effect of DOWN command for channel cc and resumes normal use of the channel for all tape and mass storage I/O operations.
UP,EQest.	Reverses the effect of DOWN command for device with EST ordinal est. Device remains in OFF state.
VSN,est.	Clears current VSN for tape unit with EST ordinal est and checks if a VSN is specified on the tape. Valid only if the unit is not currently assigned.
VSN,est,vsn.	Assigns one- to six-character VSN vsn to magnetic tape unit with EST ordinal est.

Subsystem Control Commands

Command	Description
IAF.	Initiates the interactive facility subsystem.
IDLE,sub.	Terminates the subsystem sub.
MAG.	Initiates the magnetic tape subsystem.
NAM.	Initiates the network access method subsystem.
STOP,sub.	Drops (terminates) subsystem sub.

System Control Commands

Command	Description
AUTO.	Initiates all currently enabled subsystems to control points and initiates automatic job processing.
CHECK POINT SYSTEM.	Rolls out all jobs and transfers contents of central memory tables to mass storage.
DIS,jsn.	Initiates job display package (DIS) to job with job sequence name jsn. (Console keyboard must be unlocked.)
LOCK.	Locks the console keyboard.
MAINTENANCE.	Performs the same functions as the AUTO command, but also initiates several maintenance service class jobs to perform online hardware checkout.
STEP.	Sets monitoring step mode. Stops all central memory I/O operations and prevents the system from processing PP requests when the next monitor function is encountered.
UNLOCK.	Unlocks the console keyboard.
UNSTEP.	Clears step mode. (Console keyboard must be unlocked.)

Memory Entry Commands (These commands can only be entered when the location to be changed is currently displayed on the left screen.)

Command	Description
loc,val.	Changes contents of central memory location loc to val (20 digits).
loc,b,val.	Changes contents of byte b at central memory location loc to val.

Channel Control Commands

Command	Description
ACN,cc.	Activates channel cc.
DCN,cc.	Deactivates channel cc.
FCN,cc,func.	Outputs functions code func to channel cc. If func is not specified, this command outputs a zero function code (no activity) to channel cc.
IAN,cc.	Inputs to pseudo A register from channel cc.
LDC,nnnn.	Loads pseudo A register with nnnn. (nnnn is normally a peripheral equipment function code.)
OAN,cc.	Outputs contents of pseudo A register to channel cc.

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APPENDIX B: LIST OF FIELD REPLACEABLE PARTS

Amperif Part Number	Description
1602208-101	Disk I/O backplane
1106010-204	LED-Challenger II PCBA
1106011	Keyboard assembly PCB
1106012-401	8085
1602003-303	OCP
1601962-402	XMC
1106095	AIO
1601527-101	BIOE
1120010-402	XMCIP
1120014-302	MDBP
1120016-803	MPCP
1602209-401	3 MB controller backplane
1601909-101	EXXP
1601138-103	AIX
1601715-101	BIXE
1603016-101	OCP control panel
1601916-602	Disk drive control PCBA
1602276-203	Expansion backplane PCBA
1601316	Cable, thumbwheel switch to OCP
1601317	Cable assembly display to OCP
1601459-002	Cable assembly, LED-J3 to SW
1601494-202	XM16KP
1601495-131	XM16KPD
1601716-822	DIFE
20055612	40-character display 5 X 7 dot, VF
20105213	Fan, 4.5", 230 VAC
20105413	Fan, 10", 230 VAC
20187611-003	Circuit breaker, 7.5 A
20187611-002	Circuit breaker, DPST, 5 A, 230 VAC
20109311	Circuit breaker, 4SPT, 20 A, 230 VAC
20187611-001	Circuit breaker, DPST, 3 A, 230 VAC
20114801	Power supply, 400 W +5 V
20114901-001	Power supply, 150 W, -5 V
1602910-101	UBI PCA
1602911-101	29116 SB PCA
1602912-301	CDCI PCA
1602913-101	CDC backplane PCBA
30160450-001	CDC Sabre drive power supply, 430 W
30160550-001	CDC Sabre disk drive, 8"
1602748-101	Driver PCBA
1602749-101	Receiver PCBA

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GLOSSARY

Access time. The time required to locate data on any disk. For disks, the time required for the heads to be moved to the appropriate cylinder (seek time) and for the appropriate point on the track to rotate to the read/write head (latency).

CCT. Controller confidence test. Diagnostic procedures that verify the proper operation of the controller hardware.

Channel. A path along which signals, commands, and data can be sent.

Controller. A functional unit in a data processing system that controls one or more units of peripheral equipment, such as a disk controller.

Cylinder. The set of all tracks accessible at a single position of the read/write heads.

Disk drive. A mechanism for moving a disk pack or magnetic disk and controlling its movement.

Disk, magnetic. A flat circular platter with magnetic surface(s) on which data can be stored by selective magnetization of portions of the surface.

Disk, Winchester. A sealed unit which contains disk platters (fixed on a spindle) and recording heads.

ECC. Error correction code. Additional bits appended to data that allow media errors to be detected and corrected.

Emulate. To imitate one system with another, primarily by hardware, so that the imitating system accepts the same data, executes the same programs, and achieves the same results as the imitated system.

FIPS. Federal Information Processing Standard.

Format. The arrangement or layout of data in or on a data medium.

Header. System-defined control information that precedes user data.

Host system. The computer system to which the 7100-30 is attached.

ILD. Inline diagnostics. A set of diagnostic routines and programs which can run while the system is online.

Latency. The time it takes for a point on a track to rotate to the read/write head so data transfer can begin. Average latency is one-half a revolution.

LED. Light-emitting diode.

Movable head. A read/write head which can be moved over several tracks.

Prep factor. Disk space is formatted by software into discrete physical record areas with short intervening spaces (interrecord gaps). Prep factor is the length of these physical record areas. Thus, if the length of the data field in each physical record is 116 words, this is said to have a prep factor of 116.

Read before write. A time-consuming operation that occurs when the starting or ending address of data to be written does not match the physical record boundaries on the disk pack.

Read/write head. A magnetic head which can record information on or read information from a magnetic disk surface.

Record. A set of related data or words treated as a unit.

Seek. An operation that positions the read/write heads to the addressed cylinder.

Seek time. The time required to physically move the read/write heads on the disk drive to the requested cylinder of the disk pack.

Track, physical. Defined by one disk revolution under one head, typically much larger than a sector formatted track.

Transfer rate. The rate at which data can be transferred between two devices.

Instantaneous transfer rate. The maximum possible transfer rate between the disk and disk controller, assuming there are no interrecord gaps. This rate can be achieved only if the requested data is contained completely within one physical record.

Sustained transfer rate. The rate achieved in practice, allowing for the requested data to span several physical records.

Channel transfer rate. The rate at which data is passed from the dual controller along a channel to the host CPU input/output processor. Channel transfer rate is a function of CPU type and cable length.

Verify. To determine whether a transcription of data or other operation has been accomplished accurately.

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7001 MASS STORAGE SYSTEM*

MAINTENANCE MANUAL

* Although this manual refers to the "7001 System," the correct name of this product is the "7100-10 System."

Part No. 1602947
August 1989

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X. LAB TROUBLESHOOTING

1. INTRODUCTION

This section tells you what subjects are included in this manual and gives you an overview of the features and benefits of the 7001 Mass Storage System.

1.1 Scope of Manual

This manual describes the 7001 Mass Storage System. Included are a description of the boards in the system, system block diagrams, equipment installation procedures, subassembly replacement procedures, the troubleshooting menu, and preventive maintenance procedures.

1.2 Features and Benefits

CDC 170/180 Series Compatibility. The 7001 provides high-performance, online data storage for Control Data Cyber 170 and 180 data channel systems. The 7001 is compatible with all 170 and 180 Series channels and operates with any currently supported software level of the NOS, NOS/BE, or NOS/VE operating systems.

Disk Array Design. The 7001 stores data in an array of small, high capacity disk drives. An array of six dual-ported disk drives is housed in the 7001 cabinet for a total of 3.33 billion bytes of disk storage.

Small Footprint. A 7001 containing the dual controller and six disk drives has a footprint of only 12.13 square feet.

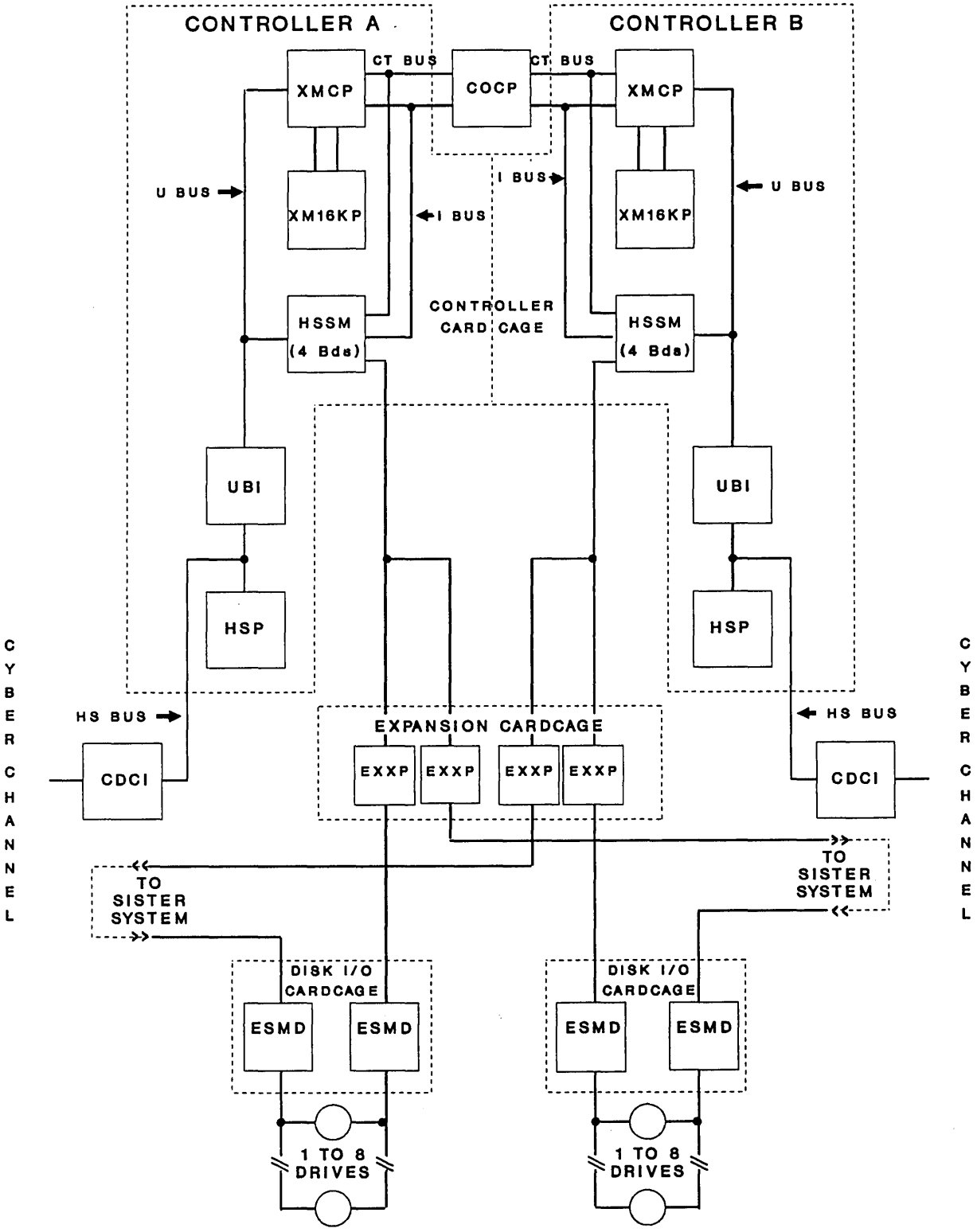
FIPS Compliancy. The 7001 uses an Enhanced Storage Module Device (ESMD) interface and therefore comply with FIPS 111.

Performance. Disk drives provide average seek times of 16 milliseconds. Rotational position sensing ensures greater data throughput, since the controller is freed from waiting until a drive revolves to a certain point.

Reduced Energy Consumption. Lower power consumption and less heat dissipation reduce utility bills.

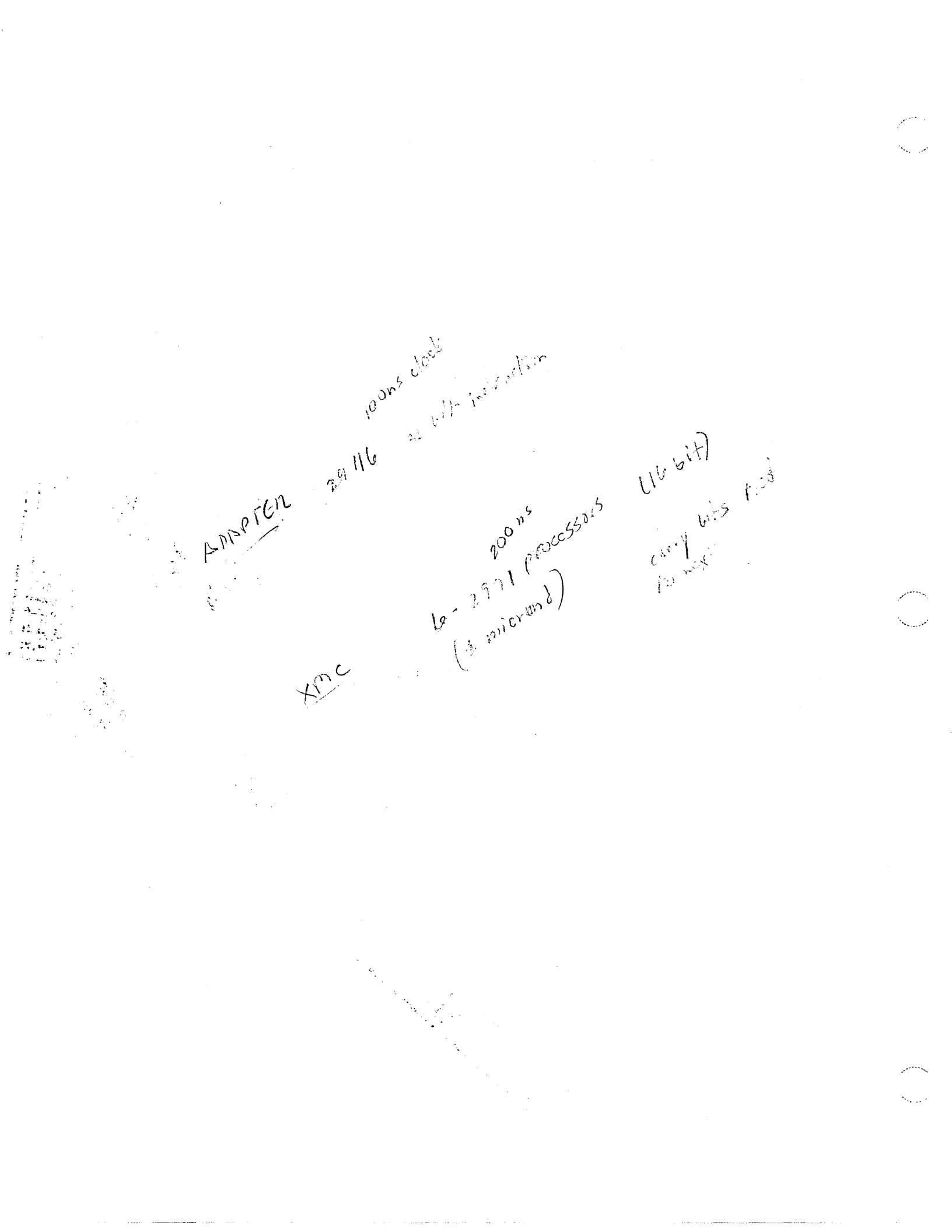
Installation. The 7001 is easily installed. No operating system changes or additions are required except configuring the operating system to support a standard CDC 7155/885 disk system.

A block diagram of the 7001 (figure 1-1) is provided on the following page.



7100-30 MASS STORAGE SYSTEM BLOCK DIAGRAM

THE "WALL"


100ns clock
ADAPTEN
29116
16 bit interface
200ns
16-bit processors
(4 microsecond)
(16 bit)
XMC

II.B 1. HS BUS - 29D BUS (13, simple) 16 bit plus par

The HS bus (high speed bus) is the communication and data bus which interconnects the adapter boards (CDCI, HSP, UBI). This bus provides the path for the adapter microcode to control the individual board functions. This is also the data path through which all channel communication takes place.

2. U BUS 36 + 2P

(36 bit)

Data is transferred through the U bus as a 36-bit word + 2 parity bits. Bits 0-17 comprise the lower half of the 36-bit word and bits 18-35 comprise the upper half of the 36-bit word. Each half of the word uses a parity bit to ensure data is transmitted correctly.

The U bus is used to transmit 5 types of information:

1. Command Function Words - adapter & XMC
2. Address Function Words
3. Status Words
4. Output Data
5. Input Data

The command and address function words are transferred between the CDCI and the XMC. The XMC breaks down the command and address function word data to determine the type of operation to be performed. The XMC also transmits Status Words through the U bus to the CDCI.

3. CT BUS 12 bit + ?

The CT bus is the overall communications bus. Data transmitted on the CT bus is 12 bits + parity. The type of information transmitted or received through a bus is determined by the hardware configuration and the microprogram. - ?, caching control, ...

4. INSTRUCTION BUS

The XMC sends instructions to all boards, except the adapter, via the instruction bus. The instruction bus is one directional; its only purpose is to supply the boards with information.

The instructions which are contained in bits 20 - 35 of the external microinstruction word are driven out as bits 0 - 15 on the instruction bus. Bits 12 - 14 define which board the instruction is going to. When an instruction is placed on the instruction bus, all of the boards are able to 'see' the instruction at the same time. However, only the board which is identified in bits 12 -14 of the instruction bus is able to read the information. The information is then decoded by theboard to determine the type of operation which is to be performed.

2. SYSTEM DESCRIPTION

This section provides the user with a functional description of each of the features that comprise a 7001 Mass Storage System.

A 7001 contains a dual controller containing two independent controllers; up to four channel interfaces per controller to the host; and a data storage base made up of six disk drives. Figures 2-1 through 2-3 show a front view of the outside of the 7001 cabinet and a front and rear view of the components which may be contained in the 7001 cabinet.

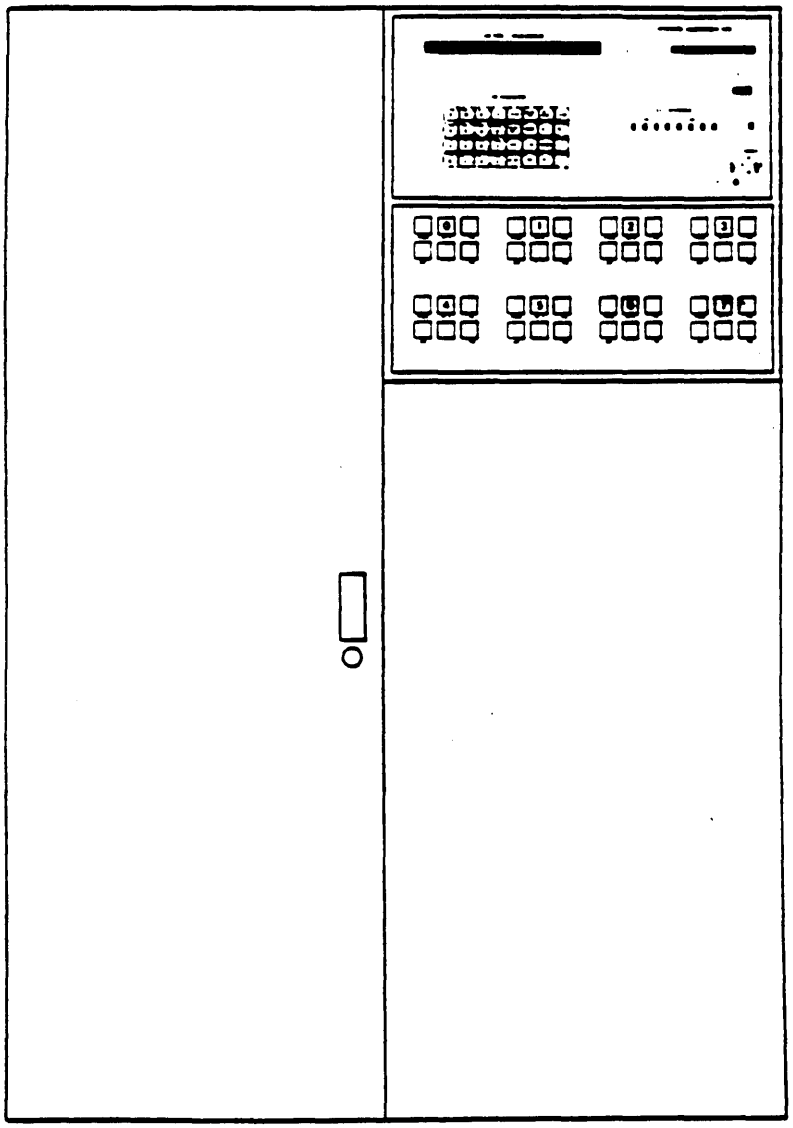


Figure 2-1
Front View of Outside of 7001 Cabinet

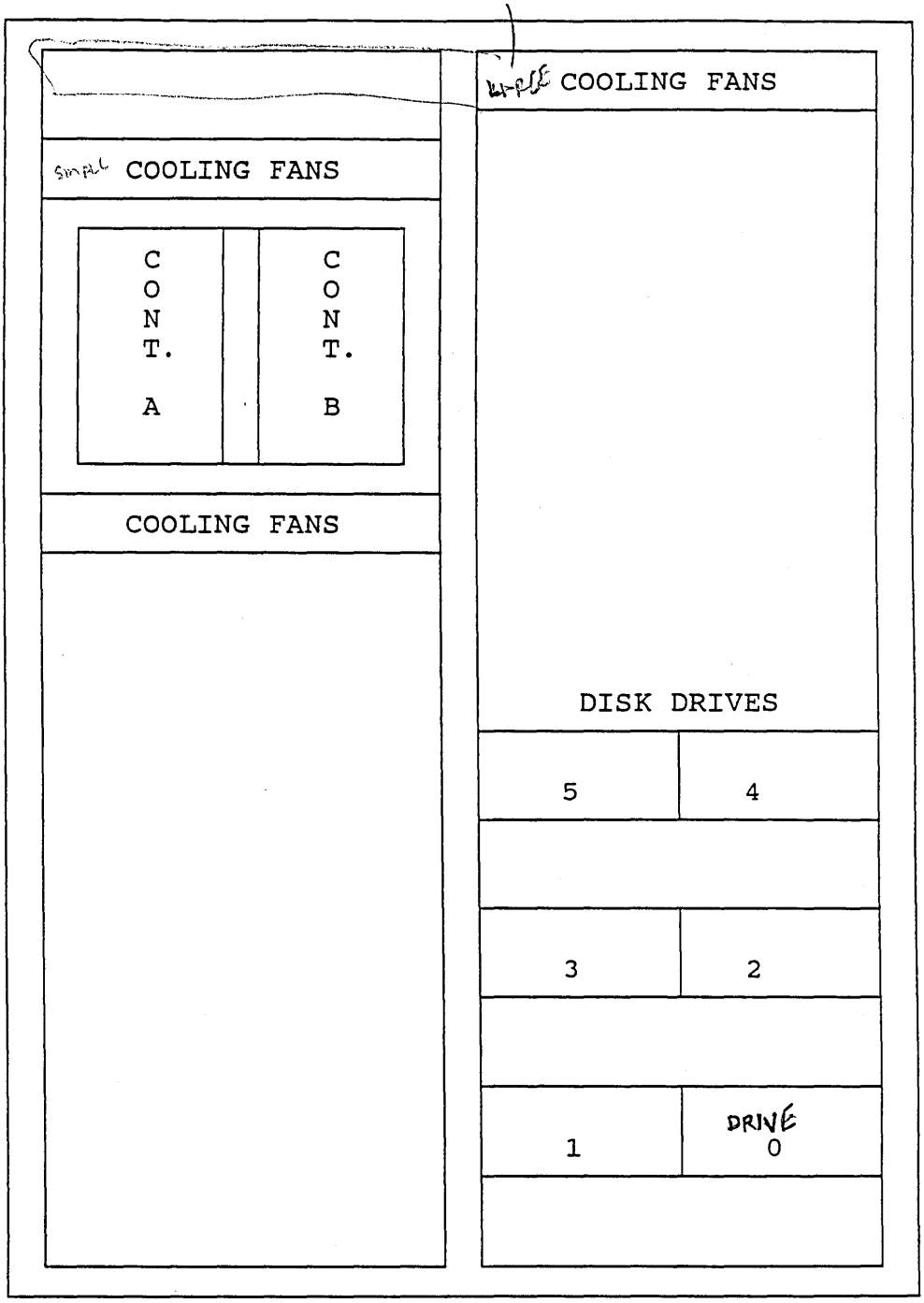
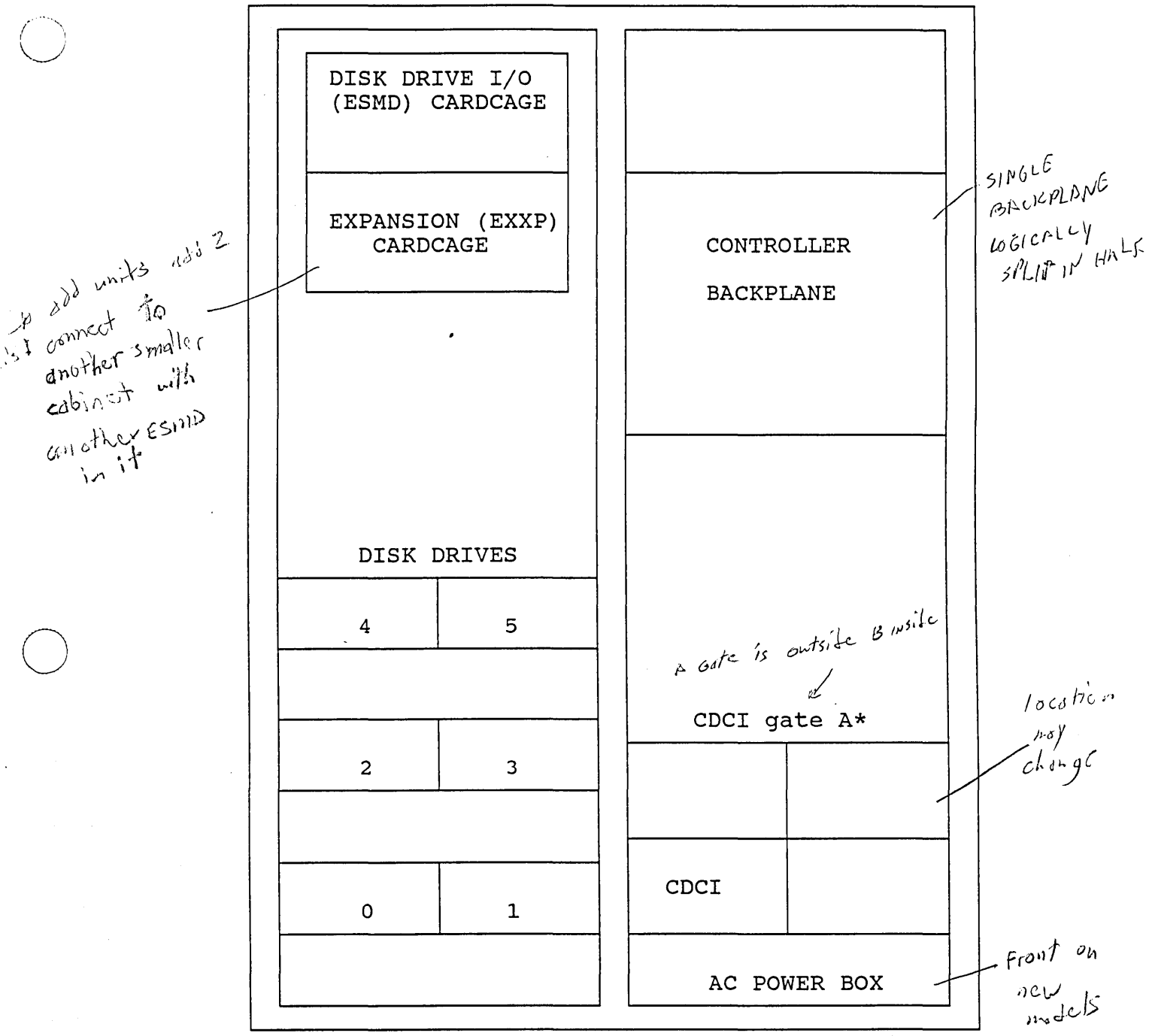


Figure 2-2
Front View of Inside of 7001 Cabinet



* CDCI gate B is behind gate A.

Figure 2-3
Rear View of Inside of 7001 Cabinet

2.1 Dual Controller

The dual controller is intelligent, microprogrammed, and controls all the functions for direct access storage operations. It contains two independent controllers that emulate Control Data 7155 channels. Each controller is capable of operating its storage devices should the other controller be offline.

Operation is via the standard Control Data Cyber device handler without modifications. The following operations are executed by the dual controller:

- Receives and interprets control information from the I/O channels
- Directs the activity of the selected storage device
- Accepts data read from the selected disk drive and transfers the data over the Cyber channel to the 830 or 960 central system processor.
- Routes the data received from the I/O channel to the selected drive and controls the writing of this data on drives.
- Executes command retry and error recovery without host intervention
- Automatically handles read-before-write

The above operations are handled by the dual controller via the boards in the system. These boards are located in the dual controller cardcage (figure 2-4) and are comprised of the following:

XMCP	contains the microprocessor that controls all disk drive functions. It communicates and commands the devices that comprise the mass storage system. The XMCP is located in slot E of controller A and slot Q of controller B.
XM16KP	provides the storage area for the microprogram code which is used for the operation of the processor in the XMCP. The XM16KP is located in slot F of controller A and slot P of controller B.
UBI	provides an external interface between the XMCP and the host channel adapter; converts the CDC 12-bit data bus to the Amperif 36-bit U bus. The UBI is located in slot H of controller A and slot N of controller B.
HSP	generates checksums on data during writes and validates these during reads. Maintains sources and destinations of data and generates address-related information to ensure proper addressing. The HSP is located in slot J of controller A and slot M of controller B.

The following boards are part of the HSSM which comprises the section that interfaces between the controller and the disk drives.

XMCIP	interfaces with the controller. The XMCIP is located in slot D of controller A and slot R of controller B.
MDBP	buffers the data. The MDBP is located in slot C of controller A and slot S of controller B.
MPCP	controls the operation of all the HSSM boards. The MPCP is located in slot B of controller A and slot T of controller B.
DIFE	interfaces with the disk drive. The DIFE is located in slot A of controller A and slot U of controller B.

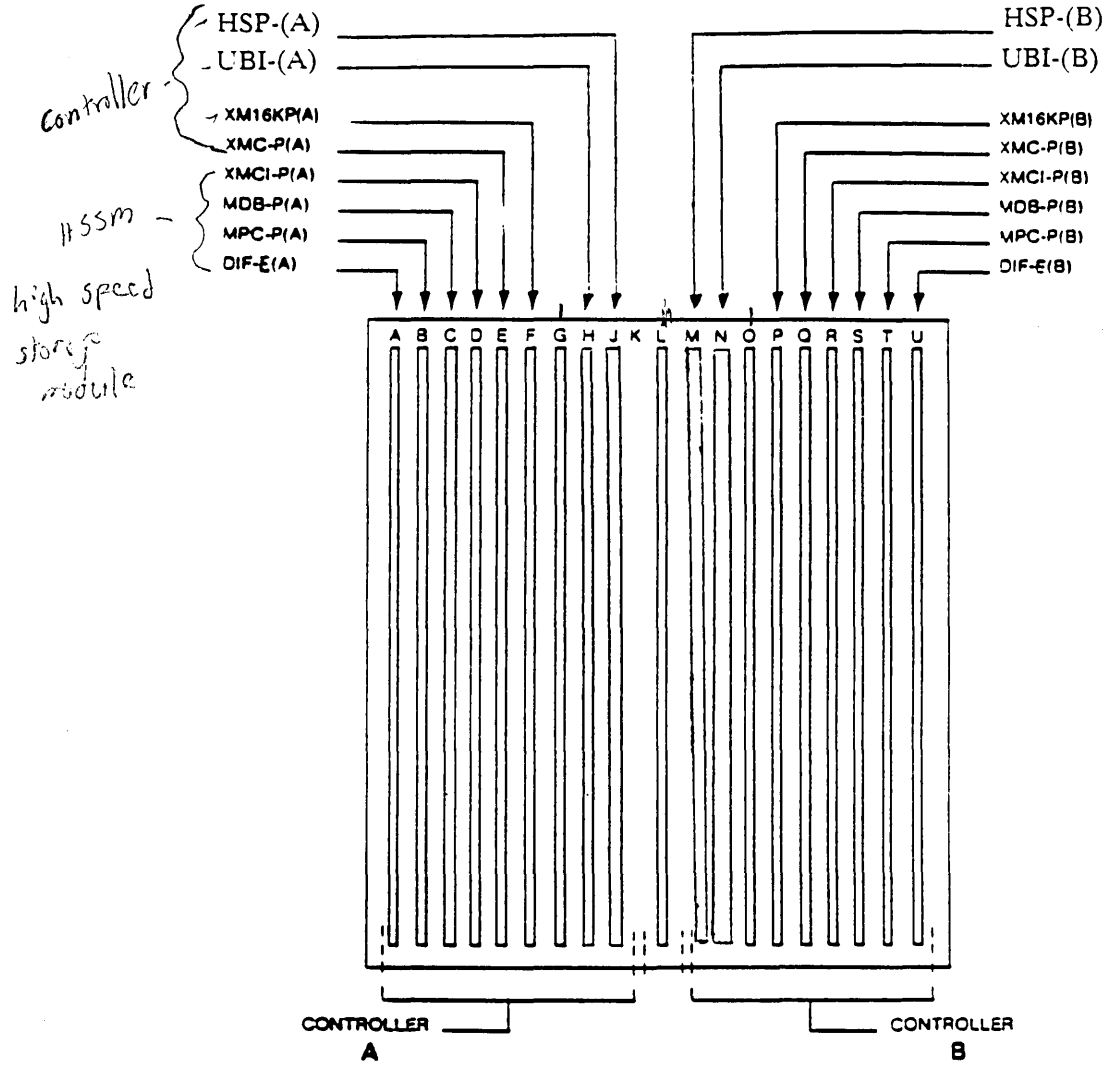


Figure 2-4
Dual Controller Cardcage

2.1.1 Channel Interface

The dual controller employs Cyber channel I/O protocol to communicate with the CDC computer system. Communication between a CDC channel and the dual controller takes place by transferring 12-bit data words, function words, and status words.

Each of the two independent controllers in the dual controller is attached to one channel of the CDC system. Optional channel interface expansion units allow each controller to be attached to a maximum of four host channels; thus, the dual controller may communicate with two to eight channels.

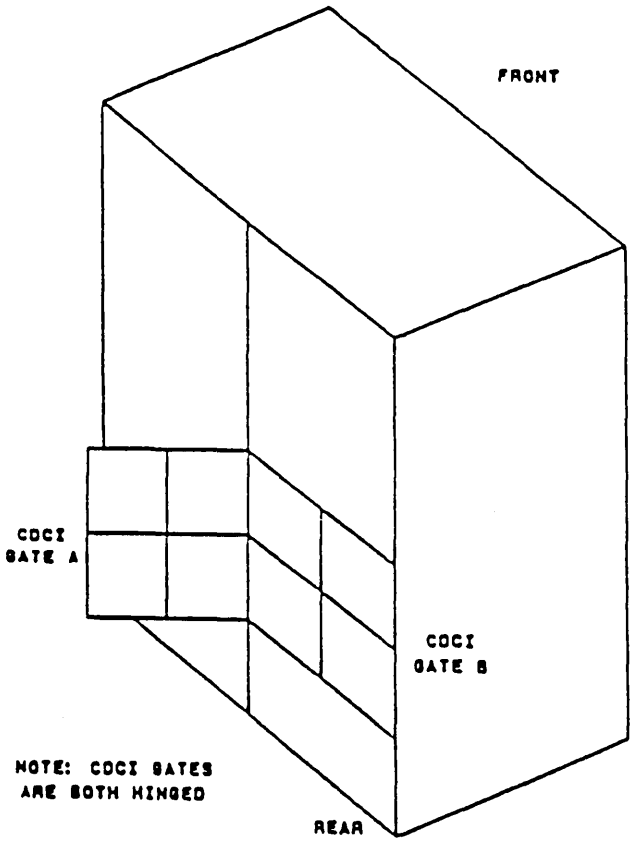
One mass storage system may be attached to up to eight hosts. Each half of the dual controller may be shared by up to four hosts, any of which can access each shared device.

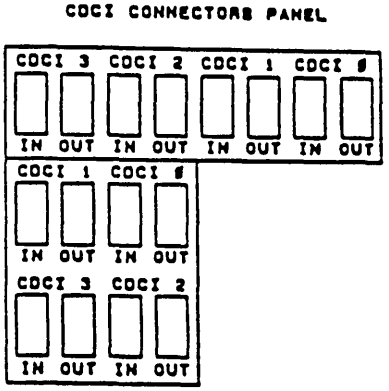
The CDCI and UBI provide the channel interface between the CDC channel and the internal U bus of the dual controller. See figure 2-5 for a view of the CDCI gates and figure 2-6 for the cable locations on the dual controller cardcage.

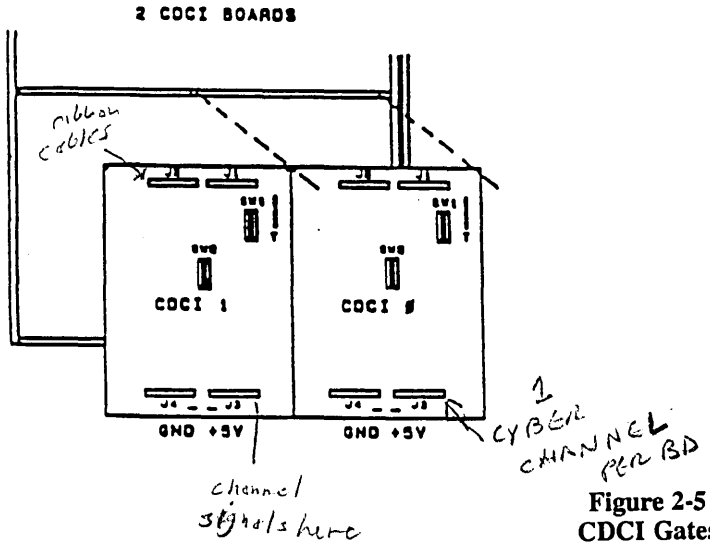
2.1.2 Data Integrity

Protection from data transfer errors is provided by parity checking, which takes place throughout the data path in the dual controller and through the channel. The microprogram contained in the dual controller performs automatic error recovery in a manner transparent to the system. Error and usage counters are maintained in the dual controller for each disk drive, whether or not the error is recoverable. In the case of recoverable errors, the error is recovered and the host CPU is not notified. In the case of nonrecoverable errors, the host CPU is notified that an error has occurred.

CDCI Gates A and B in Rear of Dual Controller Cabinet







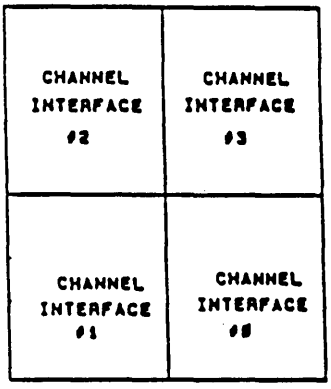


Figure 2-5
CDCI Gates

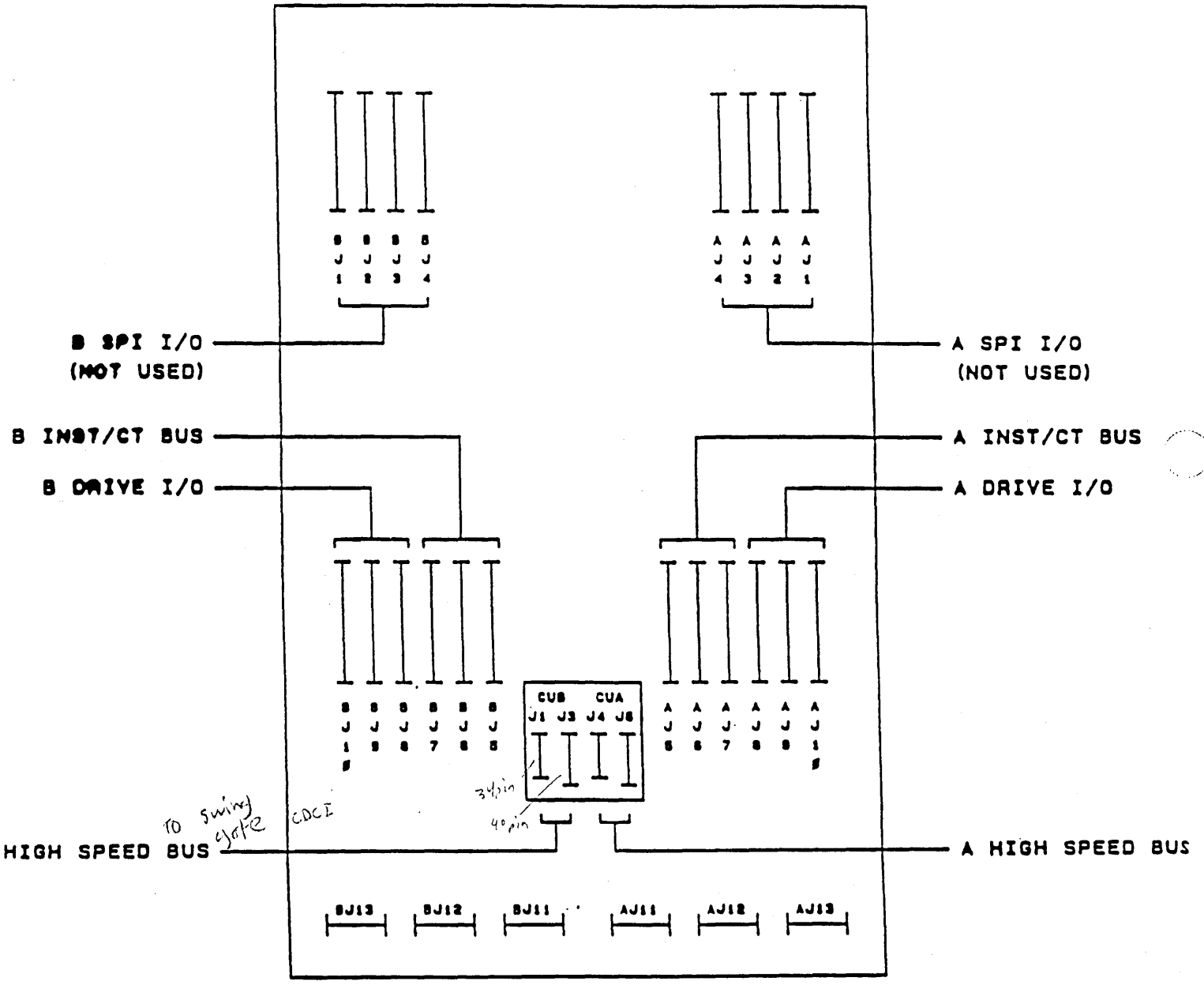


Figure 2-6
Cable Socket Locations on the Dual Controller Cardcage

2.2 Expansion Cardcage (EXXP)

The expansion cardcage contains two EXXP boards; one for each controller. The EXXP boards act as buffers for DIFE ecle logic going to the disk drive I/O cardcage. The EXXP board for controller A is located in slot A and the EXXP board for controller B is located in slot J. See figure 2-7 below.

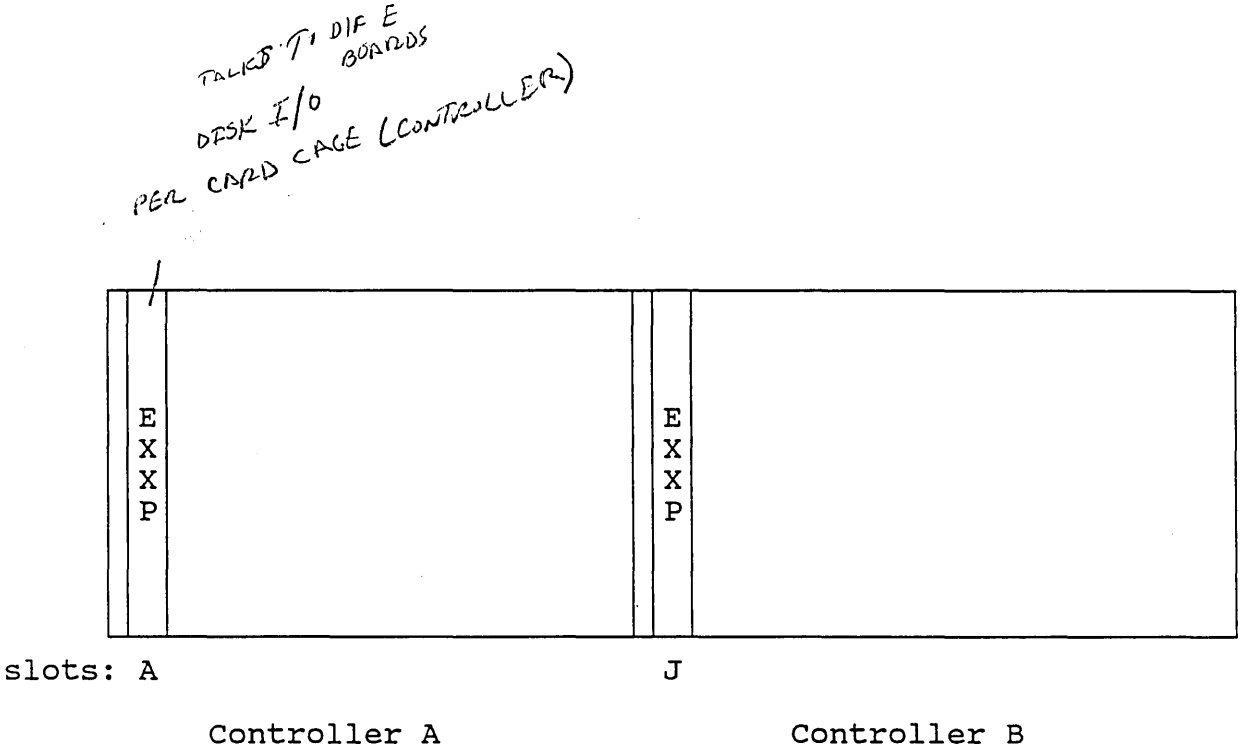


Figure 2-7
Expansion (EXXP) Cardcage

2.3 Disk Drive I/O Cardcage (ESMD)

The disk drive I/O cardcage contains four types of boards for the A side of the controller and the same four types of boards for the B side of the controller. Descriptions of the boards in these cardcages follow and they are shown in figure 2-8.

AIX provides receivers, drivers, and level translation logic required to interface the A cable signals with the EXXP cardcage. The AIX boards are located in slot A for the A side of the controller and in slot Y for the B side of the controller.

AIO provides receivers, drivers, and level translation logic required to interface the A cable signals with the ESMD interface. The AIO boards are located in slot B for the A side of the controller and in slot W for the B side of the controller.

BIX provides receivers, drivers, and level translation logic required to interface the B cable signals with the EXXP cardcage. The BIX boards are located in slot D for the A side of the controller and in slot V for the B side of the controller.

BIOE (There are three BIOE boards for the A side of the controller and three BIOE boards for the B side of the controller.)

provides the receivers, drivers, and level translation logic required to interface with a specific disk drive. Each BIOE board interfaces with two disk drives. The BIOE boards are located in slots F (for drives 0 and 1), H (for drives 2 and 3), and K (for drives 4 and 5) for the A side of the controller and slots O (for drives 0 and 1), Q (for drives 2 and 3), and S (for drives 4 and 5) for the B side of the controller.

DRIVES / TWO CABLES

TWO BOARDS LOGICALLY ON 1 BOARD

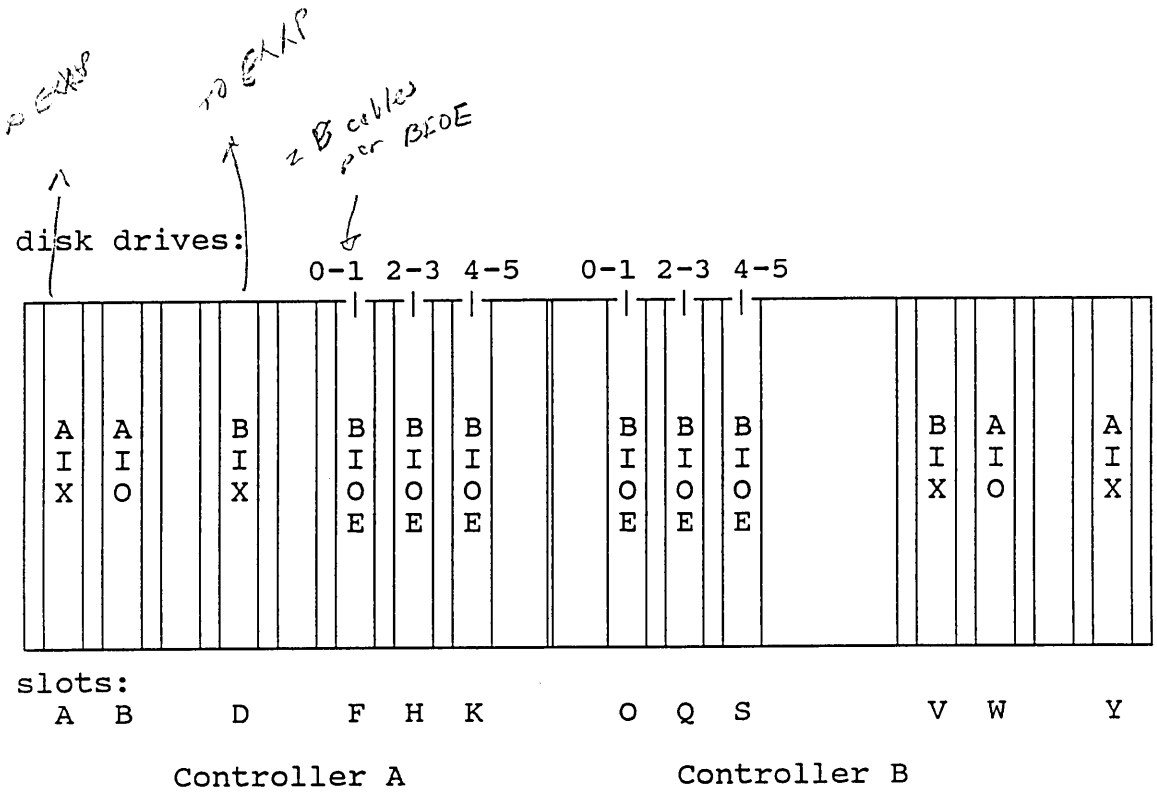


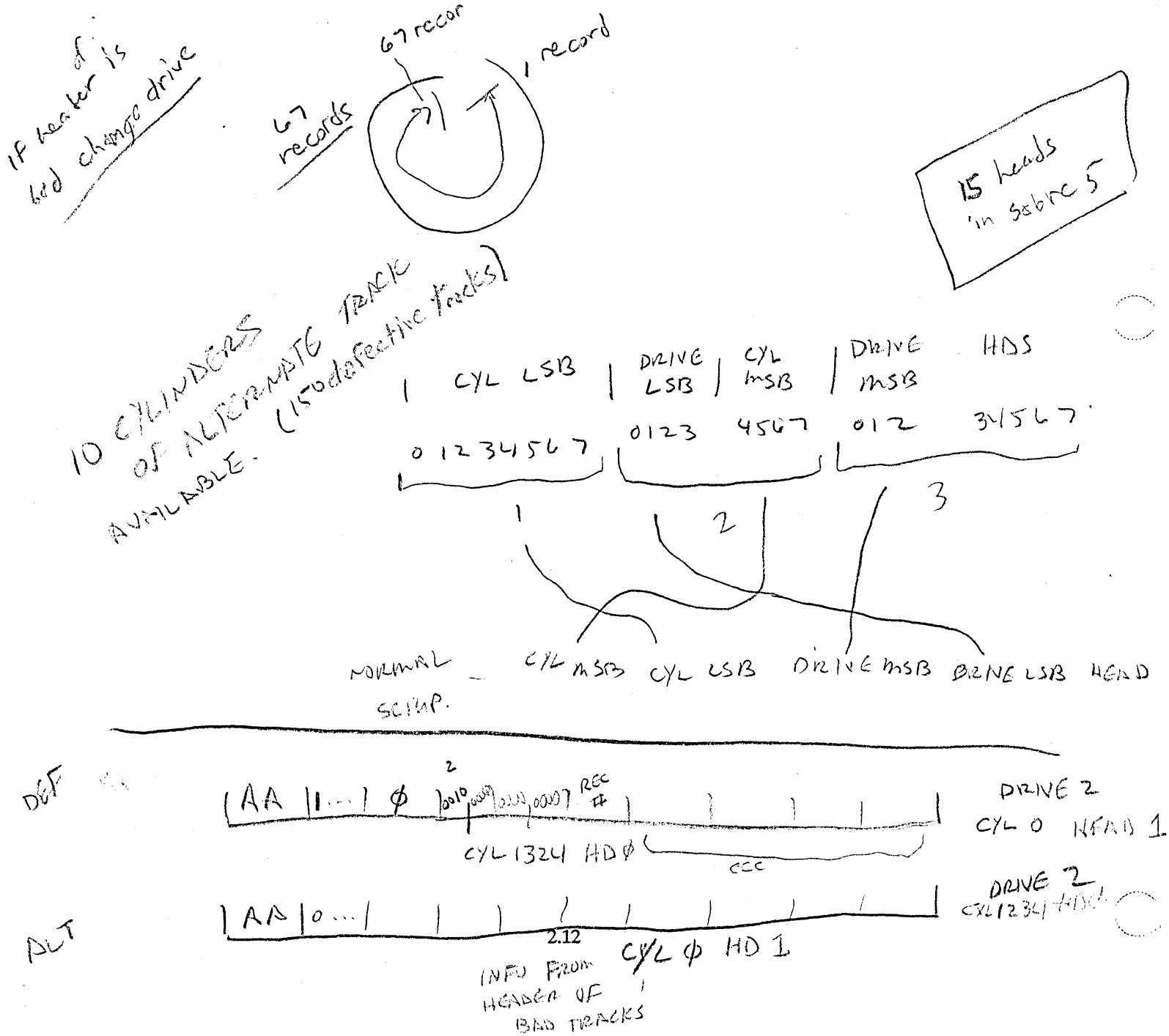
Figure 2-8
Disk Drive I/O Cardcage

2.4 9720 Disk Drives

The 9720-1230 disk drive emulates the CDC 885 disk unit. Managed by the dual controller, the drives store information on selected drive surfaces or read information from them. The 7001 contains the electronics required to perform the following functions:

- o Rotate the drive at the proper speed
- o Position the read/write heads at a particular cylinder (perform a seek operation)
- o Transfer data to/from the accessed area on the drive
- o Perform rotational position sensing to achieve greater throughput

The disk drives are random access mass storage devices using movable heads and rotating disks. A 7001 contains six disk drives.

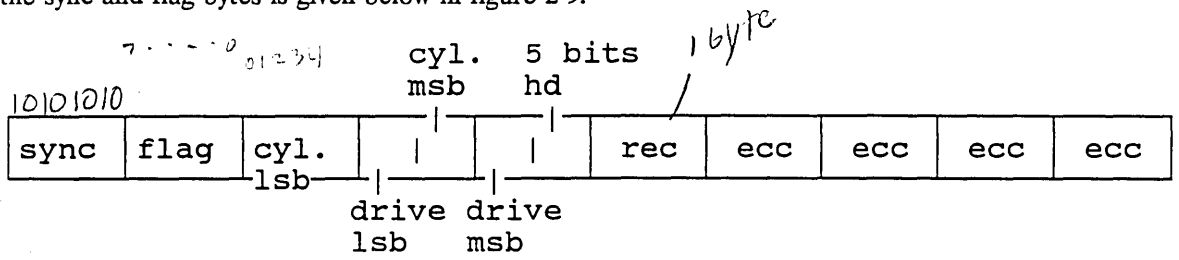


2.4.1 Track Organization

Physical Track. A track is one complete disk revolution. The physical track begins at an index point and continues until the index point is reached again. One index point serves the entire drive in indicating the physical beginning of all tracks.

Each track has the same basic organization and consists of equal-length data records. Data records are 522 bytes. A record consists of a header area and a data area. See figure 2-10 for illustration.

Header Area. The header area contains information about where the record is stored and how to access the information it contains. It contains the address and length of the data record, and an error detection code. The header area is composed of ten sections, each of which is one byte in length. Additional information on the sync and flag bytes is given below in figure 2-9.



Sync = AA
flag byte

0	Defective track			
1	Drive type	0 = Undefined	1 = Sabre 5 (9720)	2 = CDS 513
2	"	3 = M2333K	4 = Swallow 5	5 = Swallow 4
3	~~Record Length~~	6 = MPI 9720	7 = MPI 9720 with defect info.	
4	Record Length	0 = Undefined	1 = 116 WD	2 = 448 WD
5	"	3 = Undefined		
6	Emulation	0 = 8470	1 = 8434	2 = 8450
7	"	3 = Data copy		

Figure 2-9
Header Area

Data Area. The data area contains information defined by the user. An error correction code (ECC) is appended to the data area. The ECC contains a 35-bit detection and 12-bit correction capability (per physical record), thus enabling the system to correct data that has been erroneously recorded due to drive flaws.

Defective/Alternate Tracks. Should a drive track become defective, it is possible to substitute an alternate track for the defective track. An inline diagnostic (ILD) may be started from the operator control panel (OCP) or host console to mark a given track as no longer usable and assign a track from a special reserved area to replace the defective track. Once an alternate track is assigned, its use is transparent to the user. This process guarantees that the drive space as specified is always available for use.

2.4.2 Data Integrity

All drive storage operations are protected from flaws in the storage medium by an error correction code (ECC), which can detect any 35-bit burst that is in error and is able to self-correct any 12-bit burst in error for each physical record. Should any drive error occur, the information is recorded in an error log in the control unit.

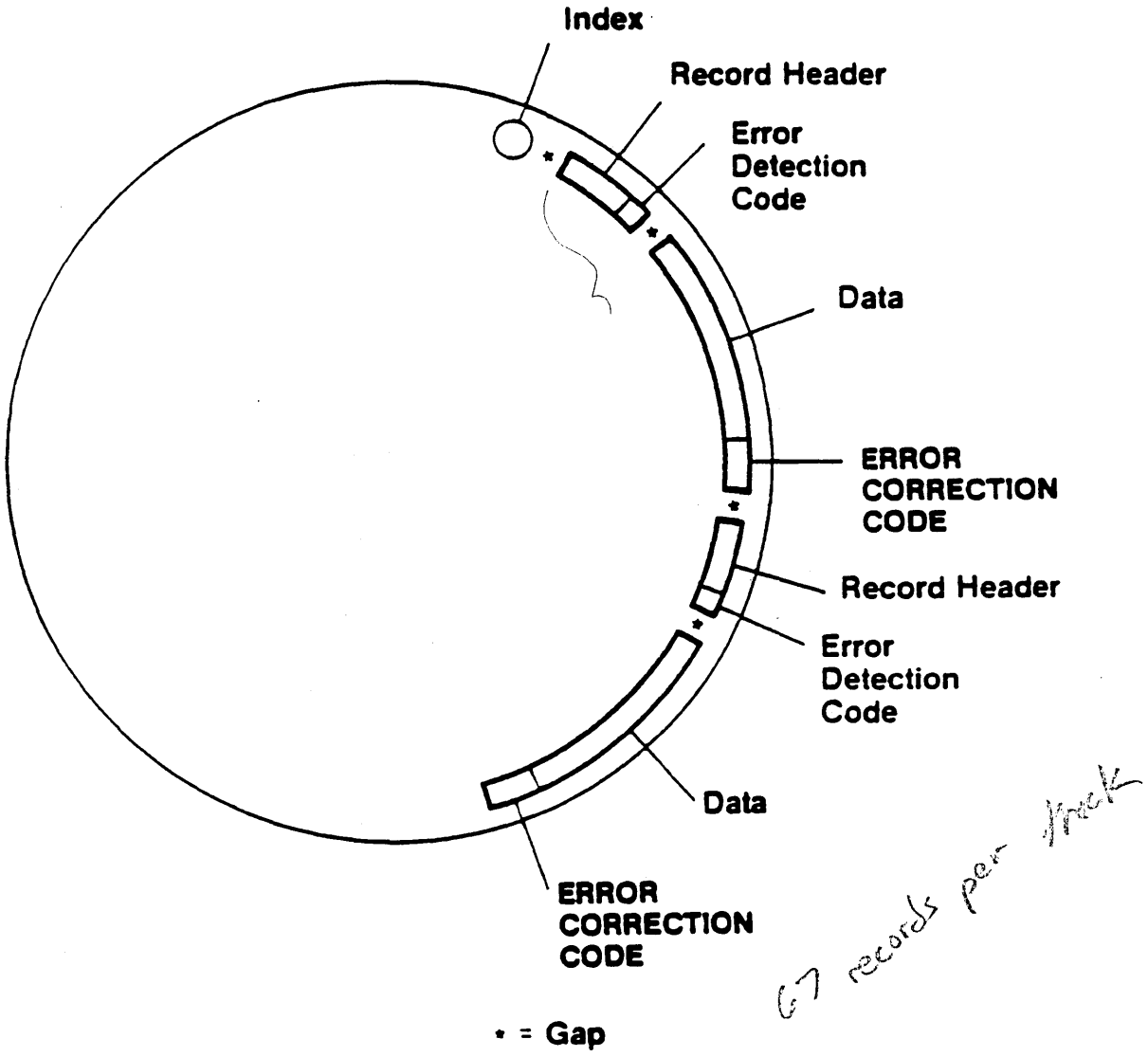


Figure 2-10
Track Organization

2.5 Operator Control Panel

Functions such as monitoring system status, system rest, changing drive states, and running offline system diagnostics are performed at the operator control panel (OCP). When commands are entered at the OCP, the user must have the appropriate level of clearance to execute a given command. Clearance is acquired by entering a correct password. There are three clearance levels:

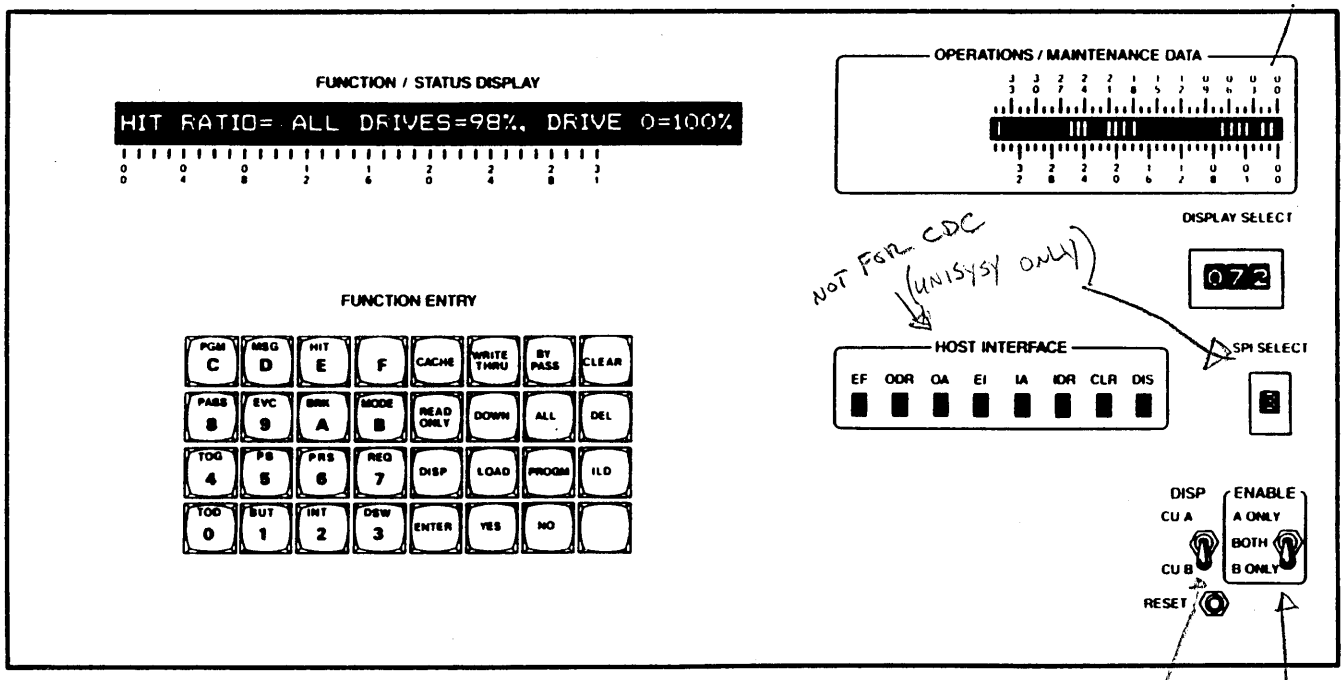
- o Monitoring
- o Operator
- o Engineering

To ensure protection of data during normal operation, the OCP can be set to disallow all system commands and allow only display functions. This is done by setting the clearance level to monitoring level clearance.

With operator level clearance, the operator may enter system commands such as setting time of dy or changing drive caching states. Maintenance and diagnostic routines may also be performed under operator level clearance.

Under engineering level clearance, all functions may be performed.

See figure 2-11 and 2-12 for illustrations of the OCP and gates.



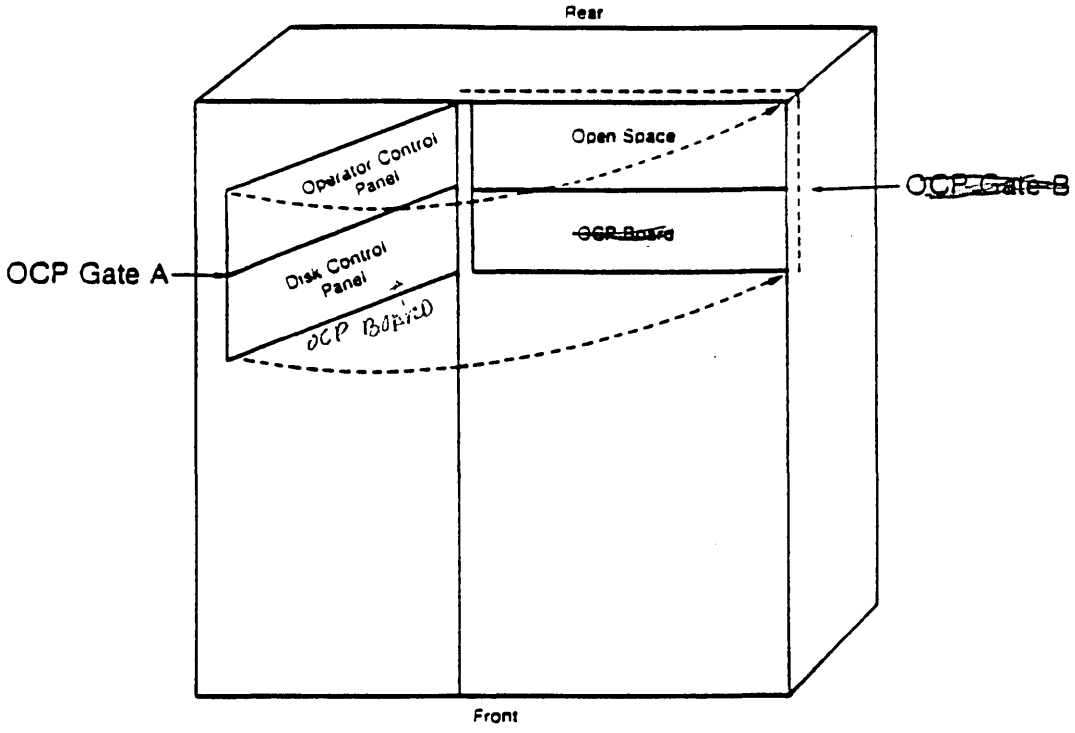
chap 8

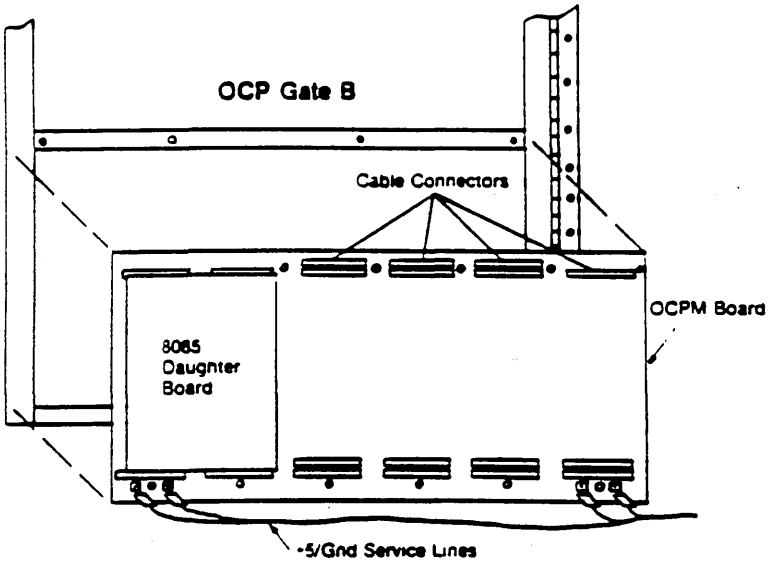
NOT FOR CDC (UNISYS ONLY)

display keypad

must have - DISP & ENABLE SET TO SAME CONT COR BOTH) to use keypad.

Figure 2-11
Operator Control Panel (OCP)





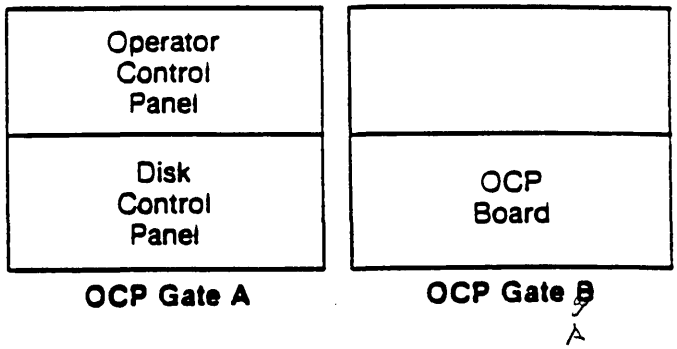


Figure 2-12
OCP Gates

2.6 Disk Drive Control Panel

The disk drive control panel contains six sets of switches and indicators which are used to operate the disk drives. Each set operates an individual disk drive and includes the following switches and indicators: (The expressions in parentheses are those which actually appear on the panel.)

Power switch (PWR)	When pushed in, this switch powers up the drive. – NOT TRUE FOR CDC UNIT (SABRES) DOES NOTHING
Ready indicator (RDY)	When lit, this indicator shows that the drive is ready.
Channel A enable switch (CHA)	When pushed in and lit, this switch allows controller A to interface with the drive.
Write protect switch (WP)	When pushed in and lit, this switch puts the drive in write protect mode so that neither controller can write to the drive.
Fault indicator (FLT)	When lit, this indicator shows that there is a fault on the drive. When pushed in, the system clears the fault and resets the indicator. (POWERING DOWN DRIVE ALWAYS CLEARS)
Channel B enable switch (CHB)	When pushed in and lit, this switch allows controller B to interface with the drive.

See figure 2-13 for an illustration of the disk drive control panel.

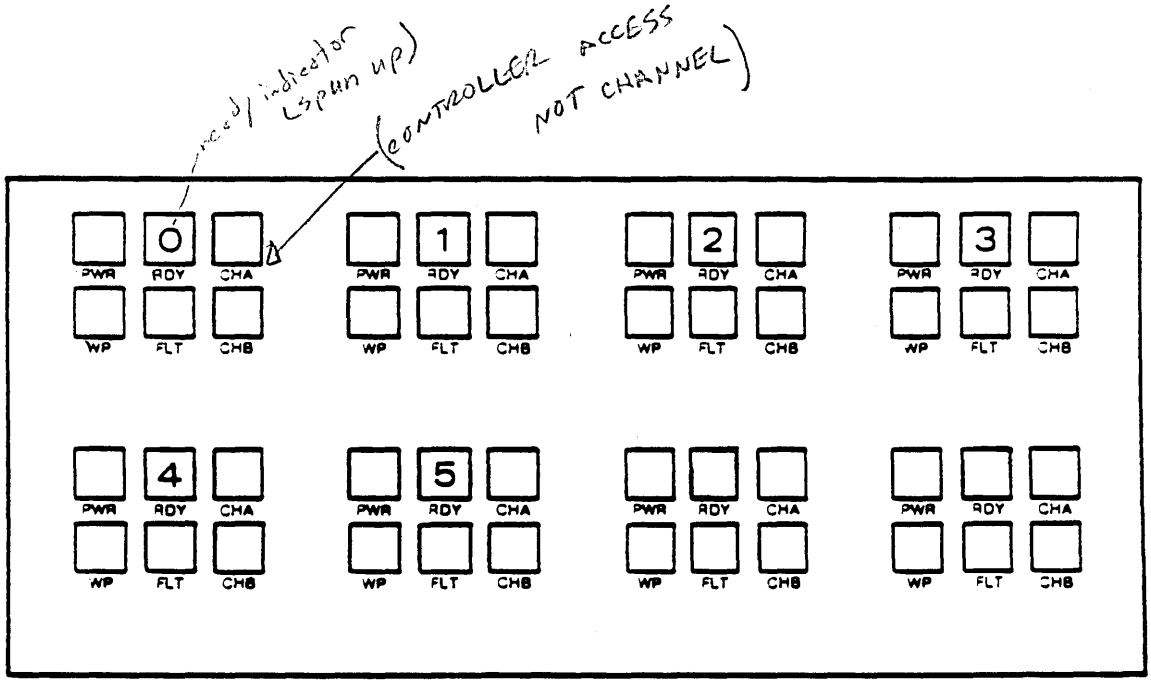
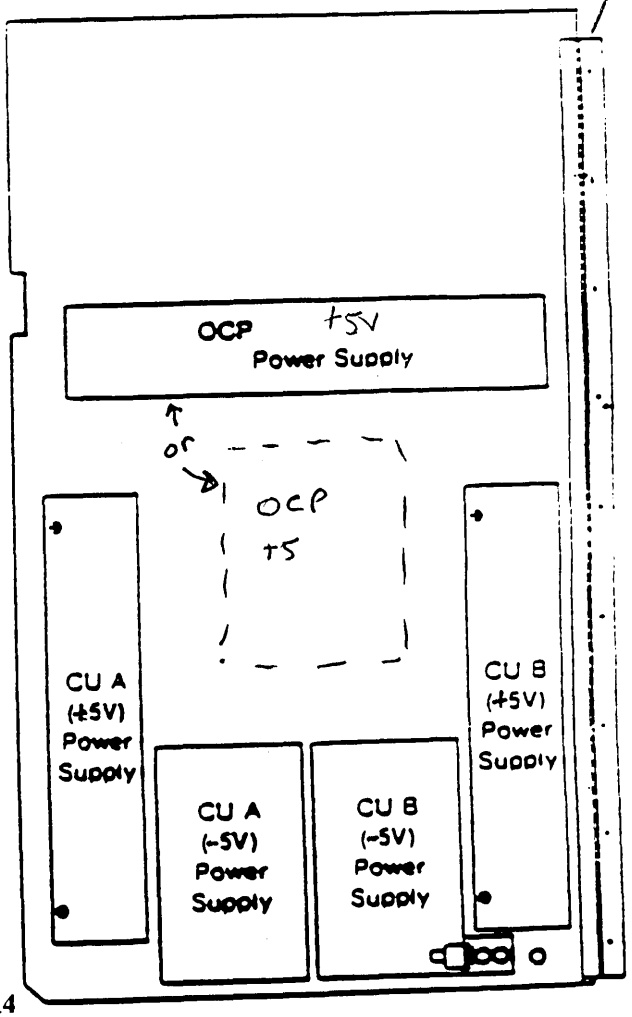


Figure 2-13
Disk Drive Control Panel

2.7 Power Supplies

There are five main power supplies in the 7001 (see figures 2-14 and 2-15). These power supplies supply the DC power to the entire 7001 system excluding the disk drives. The supplies, which are single phase, are capable of operating from a system three-phase source of 200-250 VAC at either 50 or 60 Hz.

1. OCP power supply
   Supplies +5V DC power to the OCP.
2. Controller A power supply, +5V
   Supplies +5V DC power for controller A, ESMD-I/O cardcage, EXXP cardcage, and the CDCIs.
3. Controller A power supply, -5V
   Supplies -5V DC power for the controller ESMD-I/O cardcage, and the EXXP cardcage.
4. Controller B power supply, +5V
   Supplies +5V DC power for controller B, ESMD-I/O cardcage, EXXP cardcage, and the CDCIs.
5. Controller B power supply, -5V
   Supplies -5V DC power for the controller ESMD-I/O cardcage, and the EXXP cardcage.



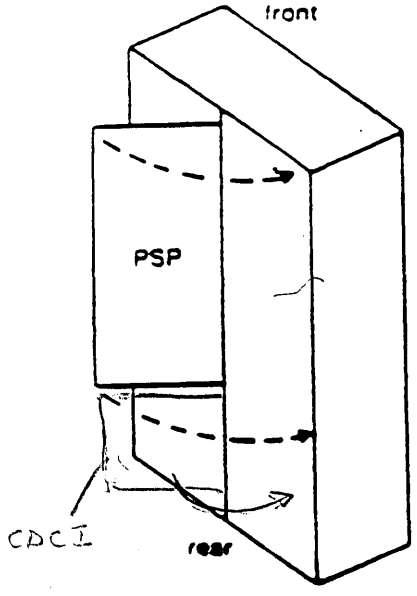


Figure 2-14
Power Supply Panel

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3. SYSTEM CONFIGURATION

The dual controller is basic and necessary to every 7001. In addition, the data storage base included consists of six disk drives. The configuration of the system components, illustrated in figure 3-1, is described below.

3.1 Dual Controller

This section describes the channel interface and the 7001 cabinet.

3.1.1 Channel Interface Configuration

The dual controller houses two I/O channel interface assemblies, one for each of the two controllers. These interfaces allow two 170/180 series I/O channels to access their respective controllers within the dual controller.

By selecting the channel interface expansion feature, the interface capability may be expanded to accommodate a maximum of eight I/O channels. With the maximum configuration, any one of a set of four I/O channels may access the first controller and any other one (of another set of four channels) may access the second controller.

3.1.2 7001 Cabinet

This cabinet houses all logic, wiring, channel interface assemblies, controls and indicators essential to dual controller operation. In addition, the cabinet provides space for six 9720 disk drives and individual power supplies. The drives are mounted on drive trays which can slide out of the cabinet and there are two drives per drive tray.

3.2 Storage Device Configuration

Both sides of the dual controller can access from one to six disk drives within the 7001 cabinet.

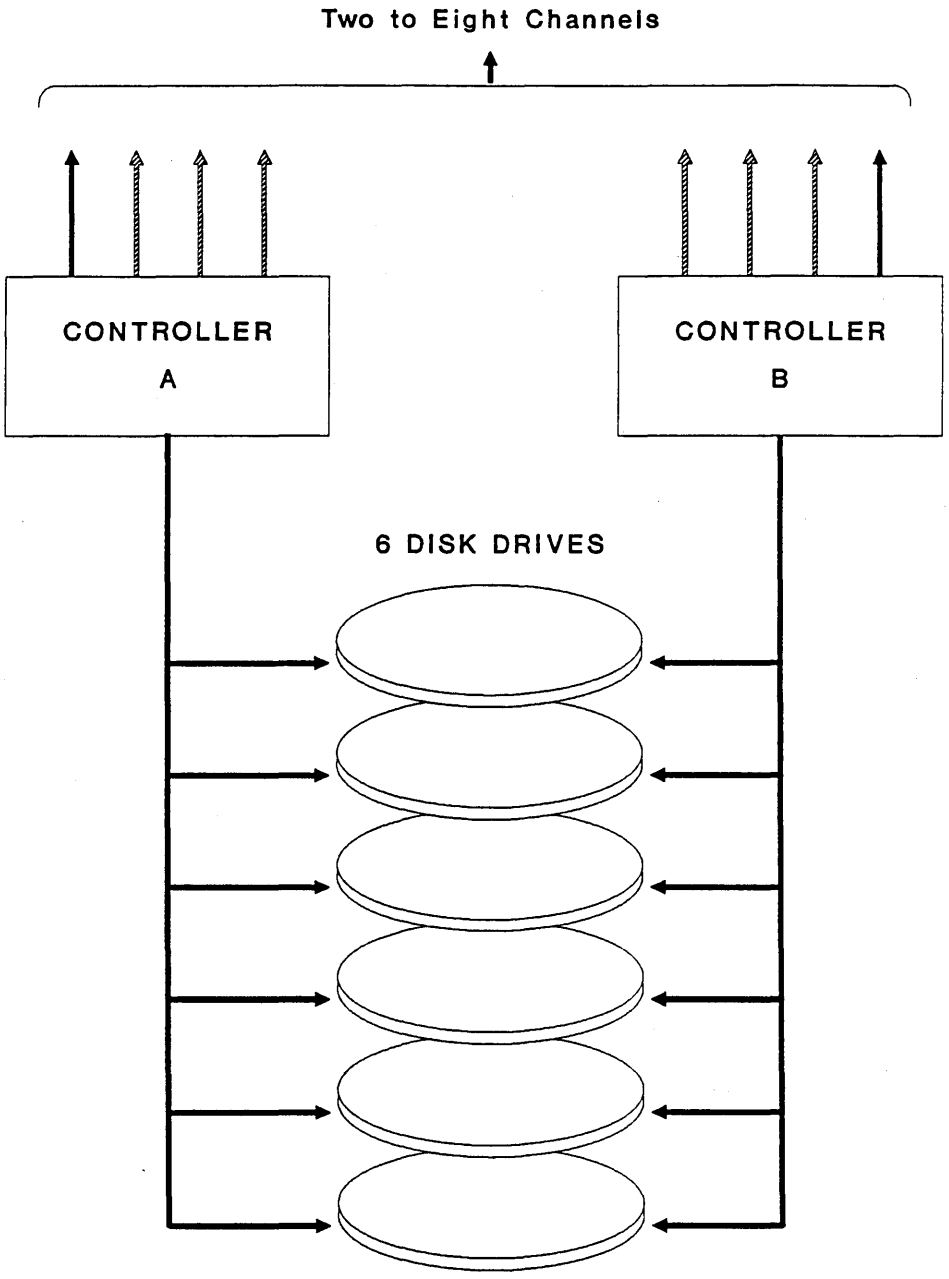
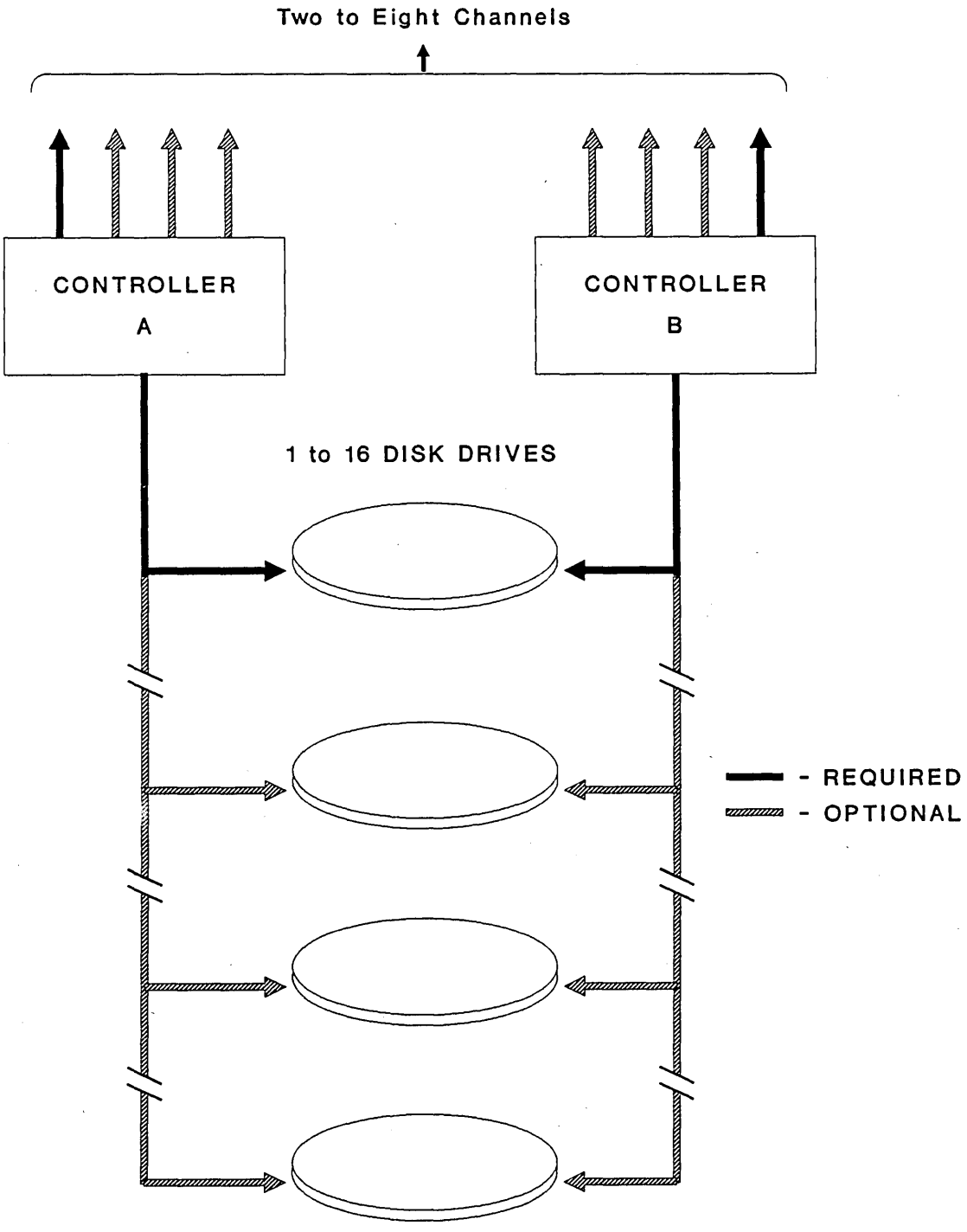
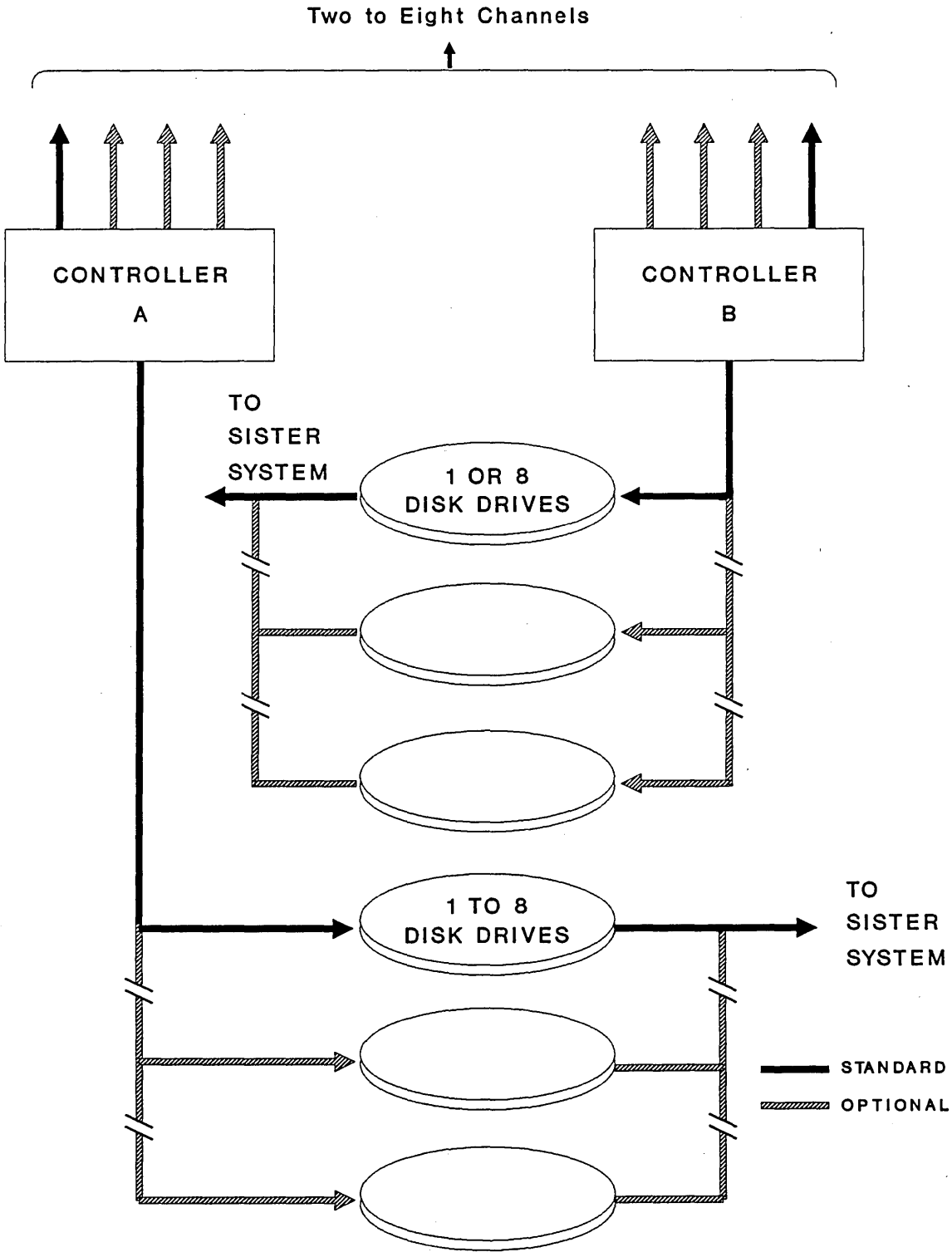


Figure 3-1
7001 Mass Storage System Configuration



7100-30 MASS STORAGE SYSTEM CONFIGURATION



7100-30 MASS STORAGE SUBSYSTEM CONFIGURATION

4. SYSTEM SPECIFICATIONS

This section contains specifications for the dual controller and the disk drives.

Dual Controller Performance

Characteristic	Specification
Microinstruction execution time	5 million instructions/second
System bus bandwidth	25.0 megabytes/second

Dual Controller Physical Characteristics

Dimensions

Height	72.5 inches
Width	44.5 inches
Depth	39.3 inches

Front/Rear Clearance 36/36 inches

Weight

Dual controller and cabinet (With 6 disk drives)	1400 lb.

Power Requirements

Voltage - 3 Phase-AC	208 delta	240 delta	220/ 380 Wye	240/ 415 Wye
Frequency - hertz	50/60 Hz	60 Hz	50 Hz	50 Hz
Current - amps	TBD	TBD	TBD	TBD
Apparent Power - kva	TBD	TBD	TBD	TBD
True Power - kw	TBD	TBD	TBD	TBD
Power Factor	TBD	TBD	TBD	TBD
Heat Dissipation- Btu/hr	TBD	TBD	TBD	TBD
User Circuit				
Wires	4	4	5	5
Circuit Breaker	30A-3P	30A-3P	30A-4P	30A-4P
Power Source Receptacles	L15-20P	L15-20P	TBD	TBD
Logic Ground Connections	Separate logic and ground connections.			

Environment

Operating Temperature	50°F to 90°F (10°C to 32°C)
Shipping Temperature	-40°F to 140°F (-40°C to 60°C)
Operating Humidity	20% to 80%
Shipping Humidity	5% to 90% noncondensing

Disk Drive Performance
(9720)

Characteristic	Specification
Minimum seek time	5 milliseconds
Average seek time	16 milliseconds
Maximum seek time	30 milliseconds
Average latency	8.33 milliseconds
Average access time	24.3 milliseconds
Instantaneous transfer rate	3.0 megabytes/second
Sustained transfer rate	2.6 megabytes/second
Rotational speed	3,600 rpm
Disk drive storage capacity	
formatted	552 megabytes (885 capacity)
unformatted	1.23 megabytes
Records per track	67 records @ 522 ~~mega~~bytes/record

Disk Drive Physical Characteristics
(9720)

Weight	
1 disk drive (including power supply)	40.8 lb.

For more detailed information, see Imprimis Product Specification #64402300.

OCP Keypad Function Matrix

Key	Display	Load	Program	ILD
0	Time of Day	Time of Day *	Introduction	ILD Halt
1	Back-up Time	Back-up Time *	Init Hit Rate	Format **
2	Interval Timer	Interval Timer *	- - - - - -	Verify *
3	Data Switch	Data Switch **	- - - - - -	Verify 1 trk **
4	Toggle Register	Toggle Register **	Init Controller *	Defective/Alt **
5	Push Button	Push Button **	Init Cache *	Osc Seek **
6	Present State	- - - - - -	- - - - - -	Random Seek **
7	Requested State	- - - - - -	- - - - - -	Seq Seek **
8	Password	Password	Init OCP **	Disk ECC Clr **
9	Event Counter	Event Counter	Init OCP Ram **	~~Mem ECC Clr~~ **
A	Breakpoint Addr.	Breakpoint Addr	8085 Editor **	~~Cache Verify~~ **
B	Mode Register	Mode Register **	- - - - - -	Data Restore *
C	Program Display	- - - - - -	Rpt XMC Reset **	~~Data Copy~~ *
D	Message	Message Clear	- - - - - -	- - - - - -
E	Hit Ratio	Hit Ratio	Slow Clock Run **	- - - - - -
F	- - - - - -	- - - - - -	Clk Single Step **	- - - - - -

* Requires Operator Level Clearance
** Requires Engineering Level Clearance

5. OCP INDICATORS AND OPERATING FUNCTIONS

5.1 Operator Control Panel

Except for the power switches, all controls for the mass storage system are handled through the Operator Control Panel (OCP). The OCP (see figure 5-1) displays the system status and allows system functions and commands to be initiated.

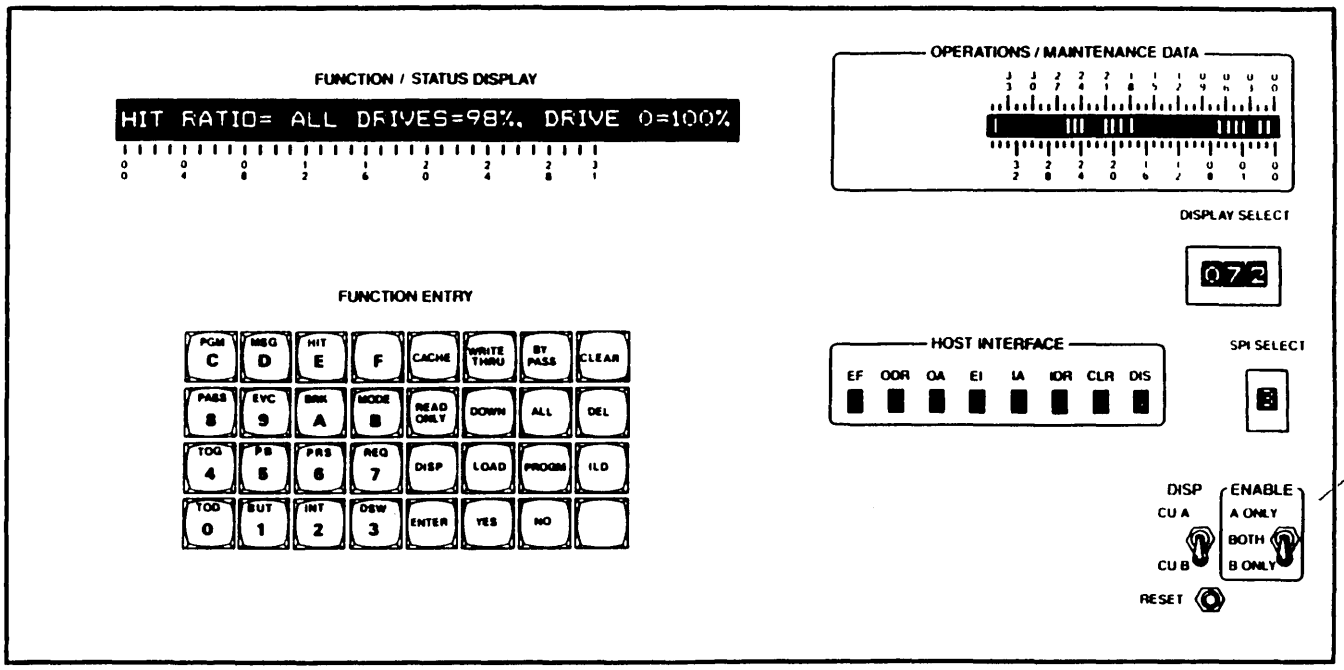


Figure 5-1
Operator Control Panel

5.1.1 Function/Status Display

The Function/Status display, located at the upper left of the OCP, shows one line of up to 40 alphanumeric characters. It communicates information directly to the operator. This information may be data, messages, or requests for operator response. It also echoes data and responses typed by the operator.

5.1.2 Function Entry Keypad

The Function Entry keypad, located at the lower left of the OCP, has 16 numeric keys and 16 function keys. These keys are used to initiate display functions, enter data, respond to questions, or initiate system commands.

Numeric Keys

The numeric keys (0 through F) are used to enter decimal or hexadecimal data. When used in conjunction with one of the function keys, the numeric key specifies which of several subfunctions is to be performed.

Function Keys

The function keys are used to enter specific commands. There are three types of function keys:

- Unit state request keys
- Master function keys
- Special response keys

Unit State Request Keys. The unit state request keys are CACHE, WRITE THRU, BYPASS, READ ONLY, and DOWN. Pressing one of these keys followed by a number (0 through 5) or followed by the ALL key initiates a command requesting the system to change the present state of one or all drives to the state specified. The numbers 0 through 5 represent one of 6 possible disk drives. See section 5.2.8 for a description of the unit state request keys.

CACHE	This key has no function in the 7001.
WRITE THRU	This key has no function in the 7001.
BYPASS	All operations are directed to the drive.
READ ONLY	Write operations are not allowed.
DOWN	No operations are allowed.

Master Function Keys. The master function keys are DISP, LOAD, PROGM, and ILD.

DISP/LOAD

Pressing the DISP key or the LOAD key followed by a numeric key specifies a certain register, data, status, or message to be displayed or loaded. The abbreviated word above each numeric key identifies the subfunctions for DISP and LOAD master function keys only.

Below is a list of keys associated with the corresponding DISP and LOAD functions. See section 5.2 (Operating Functions) for a detailed description of the display functions which may be performed by an operator.

Key/Code	DISP Function	LOAD Function
0/TOD	Time of day	Time of day
1/BUT	Backup time	Backup time
2/INT	Interval time	Interval time
3/DSW	Data switches	Data switches
4/TOG	Toggle register	Toggle register
5/PB	Push button register	Push button register
6/PRS	Present unit state	not applicable
7/REQ	Requested unit state	not applicable
8/PASS	Password/clearance status	Password/clearance status
9/EVC	Event counter	Clear event counter
A/BRK	Breakpoint address	Breakpoint address
B/MODE	Operating mode (for ILDs)	Operating mode (for ILDs)
C/PGM	Program display	Clear message display
D/MSG	System message	Clear message display

PROGM

The PROGM key, followed by the number 1, specifies that the initialize controller program be performed. See section 5.2 for a detailed description of this function.

ILD

The ILD key, followed by a number, specifies an In-Line Diagnostic (ILD) or operator function to be performed. These include verifying the disks, assigning alternate tracks, diagnosing drive and system problems, and performing special maintenance programs.

Two ILD routines may be run simultaneously, one on each controller. All ILD routines may be run while the system is online, but ILD processing is given a low priority so that it interferes minimally with normal system operations.

For this reason, when an ILD routine is started, the message "ILD PENDING" may appear on the display. This means that the controller is busy, and will start the ILD when time is available, usually within a few seconds. An ILD running on a drive takes that drive offline. It is therefore recommended that ILDs not be performed for an online drive without full intent and knowledge of the resulting effect. ILD routines which can be performed by an operator are discussed in section 5.2.

Below is a list of keys associated with the ILD function which may be performed by an Engineer:

Key	ILD Function
0	ILD Halt
1	Format disk drive
2	Verify disk drive
3	Verify a track
4	Assign alternate tracks
5	Perform oscillating seek test
6	Perform random seek test
7	Perform sequential seek test
8	Clear disk ECC display

Special Response Keys. These proper use of each of these six keys is explained below.

ALL — This is a response to a question that asks for a drive number. Answering ALL means all of the drives are to be acted upon, not just one.

DEL — Deletes the last numeric key entered so that it can be replaced with a new entry.

ENTER — This key is pressed when the numeric data entered does not equal the default parameters. Any data that was not specified is set to zero.

YES/NO — These keys are used when responding to yes/no questions.

CLEAR — This key clears the data entered at the OCP before the ENTER key is pressed. The current operating routine or function is stopped and the panel reverts to the last used display function. The CLEAR key does not affect any current operating system command or ILD; it terminates an ILD only during the parameter entry phase.

5.1.3 Operations/Maintenance Data Display

The Operations/Maintenance Data display, located at the upper right of the OCP, consists of 36 light-emitting diodes (LEDs). The octal scale above the display and the hex scale below the display help you to interpret the data displayed on the LEDs. This display is used primarily by customer engineers for diagnostic purposes.

5.1.4 DISPLAY/SELECT Thumbwheel Switches

The DISPLAY/SELECT thumbwheel switches, located at the upper right of the OCP, are used in conjunction with the operations/maintenance data display. The thumbwheel switch setting selected determines the data which is displayed at the operations/maintenance data display. This display is used for diagnostic purposes.

The thumbwheel settings are shown below:

000 to 3FF	MDBP memory data, using a single 36-bit word format.
400 to 555	XMCP scratchpad memory data, using three 12-bit words as a format.
E00 to EFF	XMCP microcode address.

The display generated by each thumbwheel setting is explained in section 8.

5.1.5 Host Interface Display

This display is not functional in the 7001.

5.1.6 SPI Select Thumbwheel Switch

This switch is not functional in the 7001.

5.1.7 DISP Channel Select Switch

The position of the DISP channel select switch, located at the lower right of the OCP, determines which controller (CU A or CU B) is displayed and controlled at the OCP. All statuses, messages, and commands are from the specified controller, except for the ILD error messages and drive states.

5.1.8 Channel ENABLE Switch

This switch is not functional in the 7001.

5.1.9 RESET Button

The function of the red RESET button, located at the lower right of the OCP, depends on the value set by the toggle register on the Function Entry keypad (see paragraph 5.2.6). RESET will abort the operation of a controller and reinitialize the system; it may clear all interrupts, de-select the disk drives, or clear disk drive faults. The button affects only the controller selected at the DISP channel select switch.

CAUTION: The RESET button should be used with caution, since pressing it indiscriminately may cause loss of data.

The PROGM 4 key increases the extent of the initialization caused by pushing the RESET button. It does this by causing the reset to initialize the buffer and the display memory of the channel specified by the channel DISPLAY/SELECT switch.

5.2 Operating Functions

This section provides instructions explaining how to perform specific operating functions. The level of clearance assigned to a function determines who may access that particular function. The type of clearance level required for each function is indicated within the function descriptions. All functions can be accessed when in engineering level clearance. This section primarily explains functions which are engineering level functions.

5.2.1 Levels of Clearance

There are three clearance levels: monitoring, operator, and engineering. Each clearance level has restrictions limiting the information which can be accessed, thus preventing unauthorized personnel from altering system functions or commands.

Monitoring Level Clearance

Key/Code: DISP 8(PASS)

Monitoring level clearance allows functions which do not require operator or engineering intervention. It allows display functions only.

Operator Level Clearance

Key/Code: LOAD 8(PASS)

Operator level clearance enables an Operator to enter certain system commands.

Engineering Level Clearance

Key/Code: LOAD 8(PASS)

Engineering level clearance allows additional maintenance and diagnostic routines needed only by field service representative. The following procedure describes how to obtain engineering level clearance.

1. At the OCP keypad, press **LOAD 8.**
2. xxxxxxxx **LEVEL CLEARANCE CANCELLED** and **MONITORING LEVEL CLEARANCE** are consecutively displayed at the OCP. Note that "xxxxxxxx" denotes monitoring, operator or engineering level clearance.
3. At the OCP keypad, press **LOAD 8** again.
4. **ENTER PASSWORD** appears at the OCP display.
5. Key in **xCExCE**, where "x" represents any digit from 0 through F.
6. **ENGINEERING LEVEL CLEARANCE GRANTED** appears at the OCP display. After **ENGINEERING LEVEL CLEARANCE** is displayed the system is ready to accept engineering level commands.

5.2.2 Time of Day

Key/Code: DISP/LOAD 0(TOD)

Clearance: Operator

This is the system's day clock. When the system is powered-up, the Time of Day register should be loaded with the correct time. All system times are on a 24-hour clock, so 2 p.m. is 14:00:00. The system clock must be set each time the system is powered up, since the time of day is lost when power is lost.

5.2.3 Back-up Time

Key/Code: DISP/LOAD 1(BUT)

Clearance: Operator

This function does not apply to the 7001.

CACHE RELATED FUNCTIONS

5.2.4 Interval Time

Key/Code: DISP/LOAD 2(INT)

Clearance: Operator

This function does not apply to the 7001.

5.2.5 Data Switch

Key/Code: DISP/LOAD 3(DSW)

Clearance: Engineering

The data switches are used to make sure the ECC circuitry is correct. This register holds nine hex digits (36-bits), which come from a register in the OCP. The value of the data switch is written to the data field when the disk is formatted (ILD 1).

The following procedure describes how to set the value of the data switches.

1. At the OCP keypad, press **LOAD 3.**
2. **LOAD DATA SWITCHES:** is displayed at the OCP.
3. Enter a number up to 9 digits. Note if less than 9 digits are keyed in, press **ENTER**; the system automatically precedes the number with zeros.
4. **DATA SWITCH: nnnnnnnnn** is displayed at the OCP. Note "nnnnnnnnn" indicates the value of the 9 data switches. Each of the 9 switches contains four bits representing the 36-bit word.

WORST CASE DATA PATTERN

5.2.6 Toggle

Key/Code: DISP/LOAD 4(TOG)

Clearance: Monitoring (for display); Engineering (for load)

This register holds two hex digits (eight bits). It is read by the XMCP board to control the depth of initialization done when the RESET button is pushed. There are five settings, with settings 00 through 17 having a cumulative effect. For example, setting 07 has the effect of setting 00, 01, as well as 07.

Toggle (hex)	Action taken when RESET is pushed
00	Resets XMCP, clears interrupts, de-selects drives and clears faults.
01	Same as 00, plus clears error/usage log and ECC history.
07	Same as 01, plus initializes control unit memory and executes controller diagnostic tests; builds operating tables in SMB memory and determines drive types.
17	Same as 07.
83	Resets system when drives have not been previously formatted or when the drive header cannot be read.

Any other setting of the Toggle is treated as 00.

The following procedure describes how to set the value of the toggle switch.

1. At the OCP keypad, press **LOAD 4.**
2. **LOAD TOGGLE:** appears at the OCP display.
3. Key in a valid toggle number, as described above.
4. **TOGGLE REGISTER:nn** appears at the OCP display. Note "nn" represents the selected toggle register.

5.2.7 Push Button

Key/Code: DISP/LOAD 5(PB)

Clearance: Engineering

The Push Button holds two hex digits that are read by the XMC to initiate ILD routines. The following procedure describes how to initiate an ILD routine using the Push Button key.

1. At the OCP keypad, press **LOAD 5**.
2. **LOAD PUSHBUTTON** appears at the OCP display.
3. Key in an ILD number (**1**, **2**, **3**, **4**, **5**, **6**, **7**, or **8**) and press **ENTER**.
4. The ILD routine selected is initiated. See the appropriate ILD routine description for additional instructions.
5. Press **CLEAR** to terminate this procedure.

5.2.8 Present and Requested Drive States

Key/Code: DISP 6(PRS); DISP 7(REQ)

Clearance: These are display functions only; they have no meaning for LOAD.

The present drive state and requested drive state functions have the same format. The present drive state displays the states of the drives as they are when you are making the request. The requested drive state displays the states of the drives according to what you have requested they be changed to.

The first 32 spaces of the Function/Status display has a letter code for each of the drive units, indicating the state of that unit. The space farthest to the left displays the state of drive unit 0 (the unit numbers are printed underneath the Function/Status display on the panel).

Code	Unit State
B	Bypass
R	Read only
D	Down

A blank in the Request display indicates all requests for that unit have been processed, so the requested state is cleared.

- **Bypass** - All operations are directed to the drive.
  Key: BYPASS
  Clearance: Operator

- **Read Only** - Write operations are not allowed.
  Key: READ ONLY
  Clearance: Operator

- **Down** - No operations are allowed.
  Key: DOWN
  Clearance: Operator

5.2.9 Event Counter

Key/Code: DISP/LOAD 9(EVC)

Clearance: Monitoring

The event counter holds the running total of times the break point address or an externally attached hardware signal was triggered. Loading the event counter sets the count to zero.

5.2.10 Break Point Address

RESET: IDLE LOOP?

Key/Code: DISP/LOAD A(BRK)

Clearance: Monitoring

For monitoring purposes, any of the system's instruction code addresses can be set as the break point address. Whenever this address is triggered, the event counter is incremented by one. Used for troubleshooting, this function is used to trace the system code operation, to make sure it is going through certain parts of the microprogram. The following procedure describes how to load the break point address.

1. At the OCP keypad, press **LOAD A.**
2. **ENTER BREAK POINT ADDRESS** appears at the OCP display.
3. Key in a four-digit number representing a valid microprogram address.
4. **ADDRESS xxxx TRIGGERED yyyy TIMES** appears at the OCP display. Note "xxxx" represent the microprogram address selected and "yyyy" represents the number of times the microprogram was triggered.

5.2.11 Operating Mode Register

Key/Code: DISP/LOAD B(MODE)

Clearance: Monitoring (for display); Operator (for load)

The operating mode register is used to modify the way ILDs are run. It affects ILDs 1, 2, 5, 6, and 7. For example, an ILD may terminate on completion or run continuously until an error is encountered or until halted by the operator, depending on the mode selected. An operating mode can be selected at any time except while parameters are being entered.

Sections 5.2.27 through 5.2.31 explain how to perform ILDs using modes.

TOGGLE 7 — POWER UP

5.2.12 Program Display

Key/Code: DISP C(PGM)

Clearance: This is a display function only, it cannot be loaded.

The Program display is not functional in the 7001.

5.2.13 System Message

Key/Code: DISP D(MSG) brings back to ILD if you looked at another display while ILD running.

Clearance: Monitoring

This register holds a system generated message conveyed to the operator via the function/status display. Whenever a new message is generated, the OCP automatically displays this register. Loading this register causes the message to be erased.

5.2.14 Introduction Routine

Key/Code: PROGM 0

Clearance: Monitoring

This is an advertising and introduction program. It displays a series of messages, each for two seconds, then the program repeats. To exit this program, press **CLEAR**.

5.2.15 Initialize Channel

controller

see toggle register definition

Clearance: Operator

When used in conjunction with the RESET Button, this reset initializes one of the channels. The channel initialized, is the one selected at the DISP channel select switch at the time the RESET button is pressed.

5.2.16 Initialize Controller

Key/Code: PROGM 4 (TOGGLE 7 RESET)

Clearance: Operator

This program clears the memory of the controller.

5.2.17 Initialize OCP

Key/Code: PROGM 8

Clearance: Engineering

This operation is equivalent to powering off the system and then powering it on again. The following procedure describes how to initialize the OCP.

1. At the OCP keypad, press **PROGM 8.**
2. **INITIALIZE OCP, ARE YOU SURE?** appears at the OCP display.
3. Press **YES** to cause the OCP software to jump directly to its power-on initialization routine. This is equivalent to powering off and then powering on the OCP. (must have controller down to do this)
4. The system automatically places all drives in bypass mode. **PROGRAM DISPLAY: 00000000** is displayed at the OCP.
5. Press **NO** to abort the program. The display is cleared.

5.2.18 Initialize RAM Buffer

OCP ram used between controllers.

Key/Code: PROGM 9

Clearance: Engineering

The RAM Buffer contains all the drive states (they are set to bypass mode), the XMC/OCP communication area and the interchannel communication status. The following procedure describes how to initialize the RAM Buffer section of the power-on initialization routine.

1. At the OCP keypad, press **PROGM 9.**
2. **INITIALIZE RAM BUFFER, ARE YOU SURE?** appears at the OCP display.
3. Press **YES** to cause the OCP software to execute the Initialize RAM Buffer section of the power-on initialization routine.
4. The system automatically places all drives in bypass mode. **BBBBBBBBBBBBBBBBBBB PRSNT** is displayed at the OCP.
5. Press **NO** to abort the program. The display is cleared.

5.2.19 8085 Editor Mode

Key/Code: PROGM A

Clearance: Engineering

This program is used to examine and edit the OCP 8085 software. When the program is initiated, the display reads:

ADDR aaaa = dd

Where **aaaa** is an address of the 8085 software and **dd** is the content of that address.

The keypad is used to enter the commands to the editor:

Key	Command
ENTER	Increment to the next address
DEL	Decrement to the last address
DISP	Get a new address to display
LOAD	Change the data of the displayed address
PROGM	Jump the OCP software to the displayed address
CLEAR	Exit the editor

Addresses 0000 to 1FFF are the 8085 ROM and cannot be reloaded.
Addresses 8000 to 83FF are the 8085 RAM and may be reloaded.

5.2.20 Repeat XMC Reset

Key/Code: PROGM C

Clearance: Engineering

This program is used primarily as an in-house debugging aid. Running this program causes the OCP to re-issue an XMC reset every 100 milliseconds. The following procedure describes how to repeat the XMC reset.

1. At the OCP keypad, press **PROGM C**.
2. **RESETTING XMC EVERY 100 MS** appears at the OCP display.
3. Press **CLEAR** to cancel the program.

5.2.21 Slow Run Mode

Key/Code: PROGM E JUMPER 28-30 ON XMC BOARD (TJ3-28 TO 30)

Clearance: Engineering

This program enables the XMC instructions to be run very slowly for diagnostic purposes.

NOTE: *In a dual channel configuration, both channels are affected by this program.*

1. At the OCP keypad, press **PROGM E.**
2. **ENTER DELAY IN TICKS** appears at the OCP display. A tick is one tenth of a second.
3. Enter a number from 1 to 255 (.1 to 25.5 seconds). One XMC instruction is executed per delay time.
4. **HIT CLEAR TO RESUME NORMAL MODE** is displayed at the OCP while the system is in slow run mode.
5. Press **CLEAR** to cancel the program.

5.2.22 Step Run Mode

need jumper on Xmc board TJ3 28-30

Key/Code: PROGM F

Clearance: Engineering

Enables execution of XMC instructions one at a time, or halts the XMC completely. The following procedure describes how to execute one XMC instruction at a time.

NOTE: *In a dual channel configuration, both channels are affected by this program.*

1. At the OCP keypad, press **PROGM F.**
2. **SINGLE STEP MODE** is displayed at the OCP.
3. **STEP ?** appears at the OCP display indicating the XMC is halted.
4. Press **YES** each time the next instruction is to be executed.
5. Press **NO** to abort the program. The display is cleared.

5.2.23 Halt ILD Routine

Key/Code: ILD 0

Clearance: Monitoring

This procedure aborts an ILD routine while it is running.

5.2.24 Format and Verify a Disk Drive

Key/Code: ILD 1

Clearance: Engineering

ILD 1 formats disk drives and in the formatting process writes header information to each record. This information includes the logical drive i.d. number. ILD 1 automatically starts ILD 2, regardless of the mode selected. ILD 2 then verifies header information, data, and ECC. Since headers include drive i.d. numbers, the verification process ensures that data is being read or written from the correct disk.

When ILD 1 is running, mode 0, 1, 2, or 4 can be used. See table 5-1 for a description of mode functions.

Conditions: The operator may format and/or verify any selected range of cylinders and heads. Parameters for that function (drive unit, starting and ending cylinder and starting and ending head) must be specified by the operator. Unless mode 4 or 6 is set when ILD 1 is initiated, ILD 2 then performs a data verification upon successful completion of the ILD 1 formatting routine.

The mode may be set before an ILD key is pressed, or after the formatting procedure has actually begun. It may not be set while the ILD routine is prompting for drive number, cylinder number, etc. The example below sets the mode while ILD 1 is formatting a drive.

Default Parameters:

Drive Unit = Last one used in the last executed ILD function.

Cylinders and Heads = Last used range for the default drive unit, or the full range if a new drive is specified.

When the format function is initiated, the system displays the default parameters it has, then asks if the operator wants to use them.

If the operator responds with a NO, or the system has no default parameters, the system requests the operator to enter new parameters using the keypad.

Run Format and Verify:

The following procedure describes how to run the format and verify routine.

LOAD MODE REG ALSO

1. At the OCP keypad, load the data switch register (see section 5.2.5) with nine hexadecimal digits (LOAD 3). These digits constitute a pattern that is written to disk when the disk is formatted with ILD 1. If no digits are specified, the data switch register is loaded with zeros by default. It is recommended that the drives be formatted with a worst-case data pattern to assist in detecting marginal disk surfaces while verifying. To accomplish this, load the data switches with the value 333086661. (SAME 5 VALUE) WORST CASE DATA PATTERN
2. At the OCP keypad, press **ILD 1.**
3. **ILD1,DR=nn OK?** appears at the OCP display. Note "nn" represents the drive number of the last ILD routine.
4. If the drive number is correct press **YES** and go to step 8.
5. If the drive number is incorrect press **NO.**
6. **ENTER DRIVE NO.** appears at the OCP display.
7. Key in a drive number (**0-31**) and press **ENTER.**
8. **START CYL=ccc,END CYL=ccc OK?** appears at the OCP display. Note "ccc" represents the cylinder number.
9. If the starting and ending cylinders are correct press **YES** and go to step 15.
10. If the starting and ending cylinders are incorrect press **NO.**
11. **ENTER STARTING CYL NO.** is displayed at the OCP. 0
12. Key in the desired starting cylinder number and press **ENTER,** if necessary.
13. **ENTER ENDING CYL NO.** is displayed at the OCP. 1633 (ENDING CY 1623 without alt tracks)
14. Key in the desired ending cylinder number and press **ENTER,** if necessary. If the entire disk is being formatted, including alternate tracks, steps 15 through 21 are skipped.
15. **START HEAD=hh, END HEAD=hh OK?** appears at the OCP display. Note "hh" represents the head number.
16. If the starting and ending head numbers are correct, press **YES** and go to step 32.
17. If the starting and ending head numbers are incorrect press **NO.**
18. **ENTER STARTING HEAD NO.** appears at the OCP display.
19. Key in the desired starting head number and press **ENTER,** if necessary.
20. **ENTER ENDING HEAD NO.** appears at the OCP display.
21. Key in the desired ending head number and press **ENTER,** if necessary.
22. **DO YOU WANT TO FORMAT DRIVE nn?** appears at the OCP display.
23. Press **YES.**

24. **FORMATTING DR.nn,CYL.ccc** is displayed at the OCP. The system formats the drive within the selected parameters. the cylinder (ccc) increments continuously until the drive has finished formatting. at this point, you may specify a mode. To do so, go to step ~~35~~ 25; if no mode is to be specified, go to step ~~38~~ 28.

25. Press **LOAD B** at the keypad.

26. LOAD MODE: appears at the OCP display.

27. Key in **0** to enter mode 0. (Mode 0 is the default mode for the ILDs.)

    To run ILD 1 with mode 2, use the above procedures, but key in **2** rather than 0 in step ~~37~~ 27.

    To run ILD 1 with mode 4, use the above procedures, but key in **4** rather than 0 in step ~~37~~ 27. Mode 4 will verify ECC, but not data, so there will be no data error message on the OCP display in step ~~39~~ 29.

28. After the drive has been formatted, the system automatically begins to verify the drive. **VERIFYING DR.nn,CYLccc** is displayed to indicate the verify procedure is in progress. As with the formatting procedure, the cylinder (ccc) increments continuously until the drive has finished verifying.

29. **VERIFY COMPLETE** appears at the OCP display if the ILD completes without encountering an error.

    or

    FORMAT ERROR DR.XX,CYL.XXXX, HEAD X appears at the OCP display if an error occurs during the formatting process

    or

    VERIFY ERROR DR.XX,CYL.XXXX, HEAD X appears at the OCP display if an error occurs during the verification process

    or

    DATA ERR:GOOD = XXXXXXXXX, BAD = XXXXXXXXX appears at the OCP display if a data error occurs.

30. If no error was encountered, press **ILD 0** to halt the ILD. If an error was encountered, press any key other than 1 or 2 to halt the ILD.

    or

    Press **1** to retry the error a predetermined number of times.

    or

    Press **2** to continuously retry the error.

NOTE: *If running ILD 1 after replacing disk drive, use procedure in section 10.14.*

RETRY MESSAGE.

Table 5-1

Mode Value Functions

Mode	ILD No.	Function
0,1	1	ILD 1 formats drives, then automatically starts ILD 2. ILD 2 terminates after it has been completed. (or error) aftr retry
0	2	ILD terminates after it has been completed. (or error)
1	2	ILD runs continuously until halted by the operator (ILD 0) or until an error is detected that cannot be corrected through retry. (1)
0	5,6,7	Seek operations are performed without verification of header information.
1	5,6,7	Header information is read from head 0 after each seek operation to confirm that the head is properly positioned. (seek problem test)
2	1	ILD 1 formats drives, then automatically starts ILD 2. The verify operation in ILD 2 stops when an error is detected or following normal completion. Error retry is not performed. no retry
2	2	Verify operation stops when an error is detected or following normal completion. Error retry is not performed. same as 0 except error retry
3	2	ILD runs continuously until halted by the operator or until an error is detected. Error retry is not performed. same as 1 except error retry
4	1	ILD 1 formats drives, then automatically starts ILD 2. The data verification phase of ILD 2 is disabled. Only ECC is verified.
6	1	ILD 1 formats drives, then automatically starts ILD 2. Mode 2 and mode 4 functions are combined.

DISP/LOAD B (mode)

mode
1 retry
2 no retry

ILD 2 (run in mode 1)

ILD 5,6,7 seeks (use mode 1)

5.2.25 Verify a Drive

Key/Code: ILD 2

Clearance: Operator

When ILD 2 is automatically run by starting ILD 1, ILD 2 verifies header information, data, and ECC. When ILD 2 is started alone, it verifies header information and data ECC, but not data. When ILD 2 is running, mode 0, 1, 2, or 3 can be used. See table 5-1 for an explanation of mode functions. The following procedures demonstrate how to run ILD 2 in mode 0:

1. Perform ILD 2 to verify the header and data ECC.
2. Press **LOAD B** at the keypad.
3. **LOAD MODE:** appears at the OCP display.
4. Key in **0** to run one cycle of ILD 2.
5. **VERIFY COMPLETE** appears at the OCP display if the ILD completes without encountering an error.

   or

   VERIFY ERROR DR. XX, CYL. XXXX, HEAD X appears at the OCP display if an error occurs during the verification process.
6. If no error was encountered, press **ILD 0** to halt the ILD; if an error was encountered, press any key other than 1 or 2 to halt the ILD.

   or

   Press **1** to retry the error a predetermined number of times.

   or

   Press **2** to continuously retry the error.

In order to run ILD 2 in mode 1, modify the above procedures by keying in **1** rather than **0** in step 4. This will enable ILD 2 to run continuously. If ILD 2 does not encounter an error, it can be terminated by entering **ILD 0.**

In order to run ILD 2 in mode 2, modify the above procedures by keying in **2** rather than **0** in step 4. This will enable ILD 2 to run one time and to stop on all data ECC errors.

In order to run ILD 2 in mode 3, modify the above procedures by keying in **3** rather than **0** in step 4. This will enable ILD 2 to run continuously. If the ILD does not encounter an error, it can be halted by entering **ILD 0.**

When ILD 2 is running in mode 2 or 3, it halts when it encounters an error and does not retry it automatically. However, if **2** is pressed when an error occurs, the ILD will no longer halt as soon as it encounters an error. Therefore, it is advisable to press **1** rather than **2** when an error occurs in order to retry an error.

5.2.26 Verify One Track

Key/Code: ILD 3

Clearance: Operator

This procedure verifies a single cylinder and head repeatedly.

Conditions: The procedure for entering the drive number, cylinder and head are similar to the Verify routine, except that the starting cylinder and head is considered the only cylinder and head.

Perform the following procedure to verify a single track.

1. At the OCP keypad, press **ILD 3.**
2. **ENTER DRIVE NUMBER** appears at the OCP display.
3. Key in a valid drive number.
4. **ENTER STARTING CYL NO.** appears at the OCP display. 0
5. Key in a valid starting cylinder number.
6. **ENTER STARTING HEAD NO.** appears at the OCP display.
7. Key in a valid starting head number.
8. **VERIFYING DR.nn,CYL.ccc,HEAD.hh** is displayed at the OCP. If the track being verified is defective and has been assigned an alternate track, it will only make one pass and then display VERIFY COMPLETE ALT. TRK.=cccc h where cccc h is the alternate cylinder and head assigned for this track. If the track is not defective, it will continuously verify until an error occurs or the routine is halted with ILD 0.

5.2.27 Assigning Alternate Tracks

Key/Code: ILD 4

Clearance: Engineering

ILD 4 automatically assigns an alternate track for a specified defective track. It also flags defective alternate tracks. The ILD prompts for the drive, cylinder, and head number to define the defective track. (This information is obtained from the disk manufacturer's flaw map program.) The ILD formats the alternate tracks, writing header information to each record that includes the logical drive i.d. number.

ILD 4 may be used online without downing the disk drive or the system, but ILD 4 will take the drive offline for the brief duration of this function. Data on the cylinder/head should be removed or backed up.

1. At the OCP keypad, load the data switch register (see 5.2.5) with nine hexadecimal digits (LOAD 3). These digits constitute a pattern that is written to the defective and alternate tracks of the disk when ILD 4 is run. It is recommended that the drives be formatted with a worst-case data pattern to assist in detecting marginal disk surfaces. To accomplish this, load the data switches with the value 333086661. If no digits are specified, the data switch register is loaded with zeros by default.
2. At the OCP keypad, press **ILD 4.**
3. **ILD 4, DR=nn OK?** ("nn" refers to the drive number.)

4. If the drive number is correct, press **YES** and go to step 8.

5. If the drive number is incorrect, press **NO.**

6. **ENTER DRIVE NO.** appears at the OCP display.

7. Key in a drive number (0-31) and press **ENTER,** if necessary.

8. **ENTER DEF. CYL. NO.** appears at the OCP display.

9. Key in the cylinder number of the defective track and press **ENTER,** if necessary.

10. **ENTER DEF. HEAD NO.** appears at the OCP display.

11. Key in the head number of the defective track and press **ENTER,** if necessary.

12. **DO YOU WANT TO FORMAT DR. nn?** appears at the OCP display (where "nn" is the drive number entered in step 7).

13. If you believe you entered the drive, cylinder, and head numbers correctly, press **YES** and go to step 16.

14. If you believe you entered the drive, cylinder, or head number incorrectly, press **NO.**

15. **ILD TERMINATED** appears at the OCP display. To assign an alternate track, start with step 1.

16. If a defective track was identified in the steps above, **VERIFY COMPLETE - ALT. TRK. = cccch** appears at the OCP display, where "cccc" identifies the alternate cylinder that has been assigned, and "h" represents the head number of the alternate track.

    If a defective alternate track was identified in the steps above, **DEFECTIVE ALTERNATE FORMAT COMPLETE** appears at the OCP display.

THE DRIVE WILL ASSIGN ALTERNATES TO 8 BITS INSTEAD OF 4 UP.

5.2.28 Oscillating Seek

Key/Code: ILD 5

Clearance: Operator

The Oscillating Seek test seeks back and forth between two selected tracks; it checks the performance of a drive. The following procedure describes how to run the Oscillating Seek routine.

NOTE: *With the seek routines, if mode 0 is enabled, a physical seek is done without verifying the header information. If mode 1 is enabled, after a seek is completed to a cylinder, the header information from head 0 is read to verify that the correct cylinder has been reached.*

1. At the OCP keypad, press **ILD 5.**
2. **ILD 5,DR=nn OK?** Note "nn" refers to the drive number.
3. If the drive number is correct, press **YES** and go to step 7.
4. If the drive number is incorrect, press **NO.**
5. **ENTER DRIVE NO.** appears at the OCP display.
6. Key in a drive number (**0-31**) and press **ENTER,** if necessary.
7. **START CYL=ccc,END CYL=ccc OK?** is displayed at the OCP. Note "ccc" represents the cylinder number.
8. If the starting and ending cylinders are correct, press **YES** and go to step 14.
9. If the starting and ending cylinders are incorrect, press **NO.**
10. **ENTER STARTING CYL NO.** appears at the OCP display.
11. Key in the starting cylinder number and press **ENTER,** if necessary.
12. **ENTER ENDING CYL NO.** appears at the OCP display.
13. Key in the ending cylinder number and press **ENTER,** if necessary.
14. OSCILLATING SEEK, DR.=n OK? is displayed at the OCP. Press **YES** to start the ILD. Press NO to terminate the ILD at this point.
15. **OSCILLATING SEEK RUNNING, DR nn** is displayed at the OCP. This indicates the system is performing the oscillating seek operation. This seek tests keeps repeating until an error is detected or the ILD Halt (ILD 0) routine is run. To stop this procedure press **ILD 0.**
16. Press **LOAD B** at the keypad.
17. **LOAD MODE:** appears at the OCP display.
18. Key in **0** to seek the drives without verifying headers, or key in **1** to enable the ILD to verify the header in addition to seeking the drive.

19. Press **ILD 0** to halt the seek routine.

    or

    If the drive has seeked the wrong cylinder, the following message will appear at the OCP display: **SEEK ERROR, DR. XX, CYL = XXXX, BAD = XXXX**. (CYL refers to the proper location and BAD refers to the actual location.)

    or

    With all other errors, the following message will appear at the OCP display: **SEEK ERROR, DR. XX, CYL XXXX**

20. Press **ILD 0** to halt the routine.

5.2.29 Random Seek

Key/Code: ILD 6

Clearance: Operator

The Random Seek test seeks from one randomly selected track to another. The following procedure describes how to run the Random Seek routine.

NOTE: *With the seek routines, if mode 0 is enabled, a physical seek is done without verifying the header information. If mode 1 is enabled, after a seek is completed to a cylinder, the header information from head 0 is read to verify that the correct cylinder has been reached. See 5.2.31 on running ILD 5 for an example of how to set modes with ILD 6.*

1. At the OCP keypad, press **ILD 6**.

2. **ILD 6,DR=nn OK?** appears at the OCP display. Note "nn" refers to the drive number.
3. If the drive number is correct, press **YES** and go to step 7.

4. If the drive number is incorrect, press **NO**.

5. **ENTER DRIVE NO.** is displayed at the OCP.

6. Key in a drive number (**0-31**) and press **ENTER**, if necessary.

7. **RANDOM SEEK, DR.=n OK?** appears at the OCP display. Press **YES** to start the ILD. Press NO to terminate at this time.

8. **RANDOM SEEK RUNNING,DR=nn** is displayed at the OCP. This indicates the system is performing the random seek operation. This seek test keeps repeating until an error is detected or the ILD Halt (ILD 0) routine is run. To stop this test press **ILD 0**.

5.2.30 Sequential Seek

Key/Code: ILD 7

Clearance: Operator

The Sequential Seek test seeks sequentially to all tracks between a starting track and an ending track, and then seeks sequentially back to the starting track.

NOTE: *With the seek routines, if mode 0 is enabled, a physical seek is done without verifying the header information. If mode 1 is enabled, after a seek is completed to a cylinder, the header information from head 0 is read to verify that the correct cylinder has been reached.*

See section 5.2.31 on running ILD 5 for an example of the way modes are used with ILD 7.

1. At the OCP keypad, press **ILD 7.**
2. **ILD 7,DR=nn OK?** Note "nn" refers to the drive number.
3. If the drive number is correct, press **YES** and go to step 7.
4. If the drive number is incorrect, press **NO.**
5. **ENTER DRIVE NO.** appears at the OCP display.
6. Key in a drive number (0-31) and press **ENTER,** if necessary.
7. **START CYL=ccc,END CYL=ccc OK?** is displayed at the OCP. Note "ccc" represents the cylinder number.
8. If the starting and ending cylinders are correct, press **YES** and go to step 14.
9. If the starting and ending cylinders are incorrect, press **NO.**
10. **ENTER STARTING CYL NO.** appears at the OCP display.
11. Key in the starting cylinder number and press **ENTER,** if necessary.
12. **ENTER ENDING CYL NO.** appears at the OCP display.
13. Key in the ending cylinder number and press **ENTER,** if necessary.
14. **SEQUENTIAL SEEK DR=nn OK?** is displayed at the OCP.
15. Press **YES** to run the seek.
16. **SEQUENTIAL SEEK RUNNING, DR nn** is displayed at the OCP. This indicates the system is performing the sequential seek operation.
17. This seek test keeps repeating until an error is detected or the ILD Halt routine is run. To stop this procedure press **ILD 0.**

5.2.31 Clear Disk ECC Display

ECC errors stored in memory

Key/Code: ILD 8

Clearance: Engineering

The log of the ECC errors for the disks may be cleared by following the procedure described below.

1. At the OCP keypad, press **ILD 8.**
2. **ILD 8 DISK ECC DISPLAY CLEAR, OK ?** appears at the OCP display.
3. Press **NO** to abort the routine.
4. Press **YES** to clear all previous disk ECC logging.
5. **DISK ECC DISPLAY CLEAR COMPLETE** is displayed at the OCP.

5.3 Error Messages Displayed at the OCP

Below is a list of error messages which may be displayed at the OCP. In most cases, these messages indicate a condition requiring the assistance of customer service.

OCP Messages	Description/Response
**** INVALID KEY**	This message appears when an OCP key is pressed illegally. Then the message disappears and the OCP returns to the last valid display or to the current time.
*** BAD COMMAND nn**	This appears when the XMC sends an illegal command to the OCP. "nn" represents the code of the illegal command in 2 hexadecimal characters. The operator should make note of this code, then press **DISP MSG** to display the contents of the message buffer and write down what is displayed for customer service's use in analyzing this problem.
**** BAD MSG ****	This message is displayed when the XMC instructs the OCP to send an illegal message. (The operator should make note of the message for customer service's use in analyzing this problem; the message remains until it is overwritten by another message.) Or, this message is displayed when the XMC attempts to store a message more than 40 characters long in the OCP message buffer. The message flashes on the display, then the first 40 characters in the OCP message buffer are displayed. (The operator should make note of the message for customer service's use in analyzing this problem; the message remains until the CLEAR key is pushed or until it is overwritten by another message.)
BAD ENTRY RE-ENTER ILD AND NO.	These messages are displayed when an incorrect ILD number is keyed into the system (for example, ILD F). Press **ILD** and the desired number.
DRIVE NEEDS FORMATTING. ILD TERMINATED	The specified drive type cannot be identified; the operator should contact customer service.
DRIVE NOT READY	This message is displayed if there is an internal fault with the drive, if the drive is powered off, or if the drive's channel enable switches are not depressed. If the drive is powered off, power it up to access the drive. If it is not powered off, verify that its channel enable switches are enabled. If they are, the operator should contact customer service.
UNABLE TO WRITE TRACK BACK ON nn UNIT	This indicates a severe error condition has occurred which is not allowing the data to be written back to disk. The operator should contact customer service.
VERIFY ERROR DR.nn, CYL.ccc,HEAD.hh	This indicates that an error occurred while performing the verify routine. The operator should contact customer service for assistance.

5.4 7001 Offline Diagnostics and Utilities

This section provides information about 7001 diagnostics and utilities. Offline diagnostics in the 7001 are resident in prom bank 0 of the Amperif 7155 emulation code. These routines can be started from the OCP by issuing an ILD on the Amperif controller. When an error is detected by the diagnostics, an error code is returned to the channel or the OCP.

Diagnostics are run under the following two conditions:

1. At start-up or after a reset. The following three tests are automatically run.

   - o HSP CPU register test
   - o HSP local memory test
   - o U bus interface FIFO check

   If these tests are run successfully, then thumbwheel switch 4D0 = 81F100000. If they do not run successfully, then thumbwheel switch 4D0 = (error code). Except for a listing of the error codes (see section 5.4.3), these tests are not discussed in this manual.

2. When executed by function. These diagnostics stop on hard errors and there is no ability to continue. These diagnostics are described in this section.

NOTE: *Do not run diagnostics unless thumbwheel switch 4D0 = 81F100000 after a reset.*

5.4.1 Operating Procedures

NOTE: *These procedures are written for the NOS operating system.*

CAUTION: **The diagnostics/utilities that perform a write will destroy customer data. Therefore, be sure that customer data is protected before proceeding.**

To run offline diagnostics to a device, a controller must be down. To run the diagnostics/utilities from the OCP, perform the following steps from the OCP:

ENTER: ILD B

DISPLAY: TEST OK?

ENTER: YES (to continue)
NO (to run data restore ILD)

DISPLAY: TEST CODE =

ENTER: Amperif function (in hex) for the appropriate diagnostic/utility
or
FFF (to exit diagnostic mode)

5.4.2 Descriptions of Utility and Diagnostic Functions

This section describes the single utility and the four diagnostic functions which are available on the 7001. They are as follows:

- o Write Manufacture Data (utility)
- o Read Data (diagnostic)
- o Write and Read (short) (diagnostic)
- o Write and Read (long) (diagnostic)
- o Write and Read (worst case) (diagnostic)

Write Manufacture Data (utility) formats the area on disk 3 CYLINDERS used by CDC for CE cylinder, etc.

CAUTION: Manufacture data is written prior to shipment and must be present prior to customer use. This data, however, will be destroyed by any offline diagnostic/utility performing a write. Therefore, make sure that the data is protected before proceeding.

When this utility is complete, thumbwheel switch 4D0 = 771728.

AMPERIF FUNCTION = (HEX)

0100 11[illegible] xxxx

Unit number 0-5 (see tables 5-2 and 5-3)

Example: to run to unit 5

0100 1111 0110 = ~~4E6 (hex)~~ 4E5

4EX → X = 0 to F drive

Read Data (diagnostic)

AMPERIF FUNCTION = (HEX)

2EX

0010 11YX XXXX

unit number 0 - 5 (see tables 5-2 and 5-3)

1 = large sector
0 = normal sector

adapter UBL, MSP, CDCE

This function will read the surface of the pack and then check the HP/A position and checksum. For this test to run without errors, the surface must have been written by a diagnostic routine or by customer data. This function will read in large sector mode if bit 6 is set in the function, and in normal sector mode if bit 6 is not set. This diagnostic will complete and stop by itself. (See the utility discussion above for an example.)

Write and Read (short) (diagnostic)

0011 11YX XXXX

unit number 0 - 5 (see tables 5-2 and 5-3)

1 = large sector
0 = normal sector

don't use these

The surface will be written and read back and data compared. The writes and the reads to the Amperif u bus will be a single record (sector) length, so no truncation will occur. Word lengths will be **116** (74 hex) in the command words. This diagnostic will run until an error occurs or until stopped by another function. (See the utility discussion above for an example.)

Write and Read (long) (diagnostic)

0100 00YX XXXX

unit number 0 - 5 (see tables 5-2 and 5-3)

1 = large sector
0 = normal sector

This diagnostic is the same as Write and Read (short) except the word length issued to the u bus will be 65,424 (FF90 hex) in the command word and truncation will occur after the first record. This diagnostic will run until an error occurs or until stopped by another function. (See the utility discussion above for an example.)

Write and Read (worst case) (diagnostic)

← 50x x = 0--F (drive 0 to 15)

Best to use this

0101 00YX XXXX

unit number 0 - 5 (see tables 5-2 and 5-3)

1 = large sector
0 = normal sector

This diagnostic is the worst case condition found during product development. There are five parts to this diagnostic:

1. The surface is written/read with a long write/read (65,424 for a command word count) and truncated after 500 records with a different data pattern for each record.

2. The surface is written/read with a truncation after 375 records and a different pattern is used.

3. The surface is written with the same pattern as before, but with a truncation after 125 records (read ahead).

4. A complete random mode of truncation length is write/read of the surface.

5. When the entire surface has been written and checked, a complete random write and read is entered which will run until errors occur or until stopped by another function.

(See the utility discussion above for an example.)

Table 5-2
Device Addresses

NOTE: *Device addresses 0 through 5 are the only ones which apply to the 7001.*

Device Address	Unit Bits 0-3	X (Hex)
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F
16	0000	0
17	0001	1
18	0010	2
19	0011	3
20	0100	4
21	0101	5
22	0110	6
23	0111	7
24	1000	8
25	1001	9
26	1010	A
27	1011	B
28	1100	C
29	1101	D
30	1110	E
31	1111	F

Table 5-3
Utility/Diagnostic and Hex Function**

NOTE: *Device addresses 0 through 5 are the only ones which apply to the 7001.*

Utility/Diagnostic	Function (Hex) Drive Address 0-15	Drive Address 16-31
Write Manufacture Data	4EX*	4FX*
Read Data	2EX*	2FX*
Write and Read (Short)	32X*	33X*
Write and Read (Long)	42X*	43X*
Write and Read (Worst Case)	50X*	51X*

* where X is defined in table 5-2
** for large sector only

HP/A adapter

5.4.3 Error Codes

The following error codes are common to all offline diagnostics/utilities. It is possible to have both upper and lower bit errors at the same time. To verify a valid error, rotate the thumbwheel switch (on the OCP) to 4D0. The right-hand 12 bits should be identical to the error code displayed.

When the diagnostics are initiated from the OCP, the error codes will be displayed on the OCP.

X	X	X	X	X	X	X	X	X	X	X	X
11	10	9	8	7	6	5	4	3	2	1	0
upper bit error							lower 5-bit error				

upper bit error codes:
In the chart below, if the bit shown is set, the explanation which follows describes the error.

bit set:	explanation:
5	The code is a start-up error.
6	The read data does not compare with the data written.
7	The HP/A detected an error.
8	A write error was detected.
9	A track or sector error occurred.
10	A cylinder error occurred.
11	A checkword error occurred.

lower 5-bit error codes:

bits 43210	
00001	No device end before seek command issued
00010	U bus parity error
00011	No status after a seek command
00100	Command reject status returned status action of 4
00101	Status action of F returned
00110	Issued command aborted
00111	Time-out data on U bus
01000	Unexpected status present on entry to issue command routine
01001	Unexpected data present on U bus interface card on entry to issue command routine
01010	Amperif control unit did not take command word
01011	Enable tags not set on entry to issue address word
01100	Amperif control unit did not take address word
01101	Amperif control unit presented status on entry to write routine
01110	HP/A timeout waiting for output data request from Amperif control unit
01111	HP/A timeout in the high-speed write because control unit stopped taking data
10000	HP/A timeout waiting for status after a write operation
10001	Amperif abnormal write termination (see status sent)
10010	Amperif status present on entry to read routine
10011	Amperif status present after read command issued
10100	HP/A timeout waiting for enable tags after read command issued
10101	HP/A timeout waiting for data after control unit enabled tags on read
10110	Amperif terminated read operation before sending data
10111	HP/A timeout in high-speed read loop because Amperif stopped sending data
11000	HP/A timeout waiting for status after a read operation
11001	Amperif abnormal read termination

drive not ready - chk. power

lower 5-bit error codes: (continued)

bits 43210	
11010	Enable tags not present on entry to truncation routine
11011	HP/A timeout waiting for Amperif to take data before truncation
11100	Amperif input data present on entry to issued command routine

Start-up Diagnostics Error Codes (Adapter only)

Bits 543210		FRU
100001	CPU Register Test Failed	HSP
100010	Local memory/address failed	HSP
100100	Not used	---
101000	U bus interface FIFO failed	UBI

ILD B 7000 DIAGNOSTICS

OPERATION FROM 7000 OCP

To run HP/A diagnostics, perform an ILD B and answer YES to the HP/A OK? message. Enter one of the following hexadecimal codes at the HP/A CODE= prompt. Small 'n' equals unit number up to 'F'.

CODE	FUNCTION DESCRIPTION	SECTOR SIZE	TRANSFER SIZE
4En	Write Manufacturing Data	Small	N/A
2Cn	Full Pack Verify	Small	?
2En	Full Pack Verify	Large	65K words (564 S)
30n	Write, Read, Verify Full Pack	Small	1 Sector
32n	Write, Read, Verify Full Pack	Large	1 Sector
40n	Write, Read, Verify Full Pack	Small	1 Sector(w/trunc)
42n	Write, Read, Verify Full Pack	Large	1 Sector(w/trunc)
50n	Write, Read, Verify Worst Case	Small	Variable
52n	Write, Read, Verify Worst Case	Small	Variable

ERROR CODES

DISPLAYED AT THE 7000 OCP

The error code will automatically be displayed in hex at the OCP if any errors were detected. There may be more than one bit set in the Upper Codes (the first group) bits 5 - 11. The Lower Codes including Write/Read Errors should be a straight decode as listed.

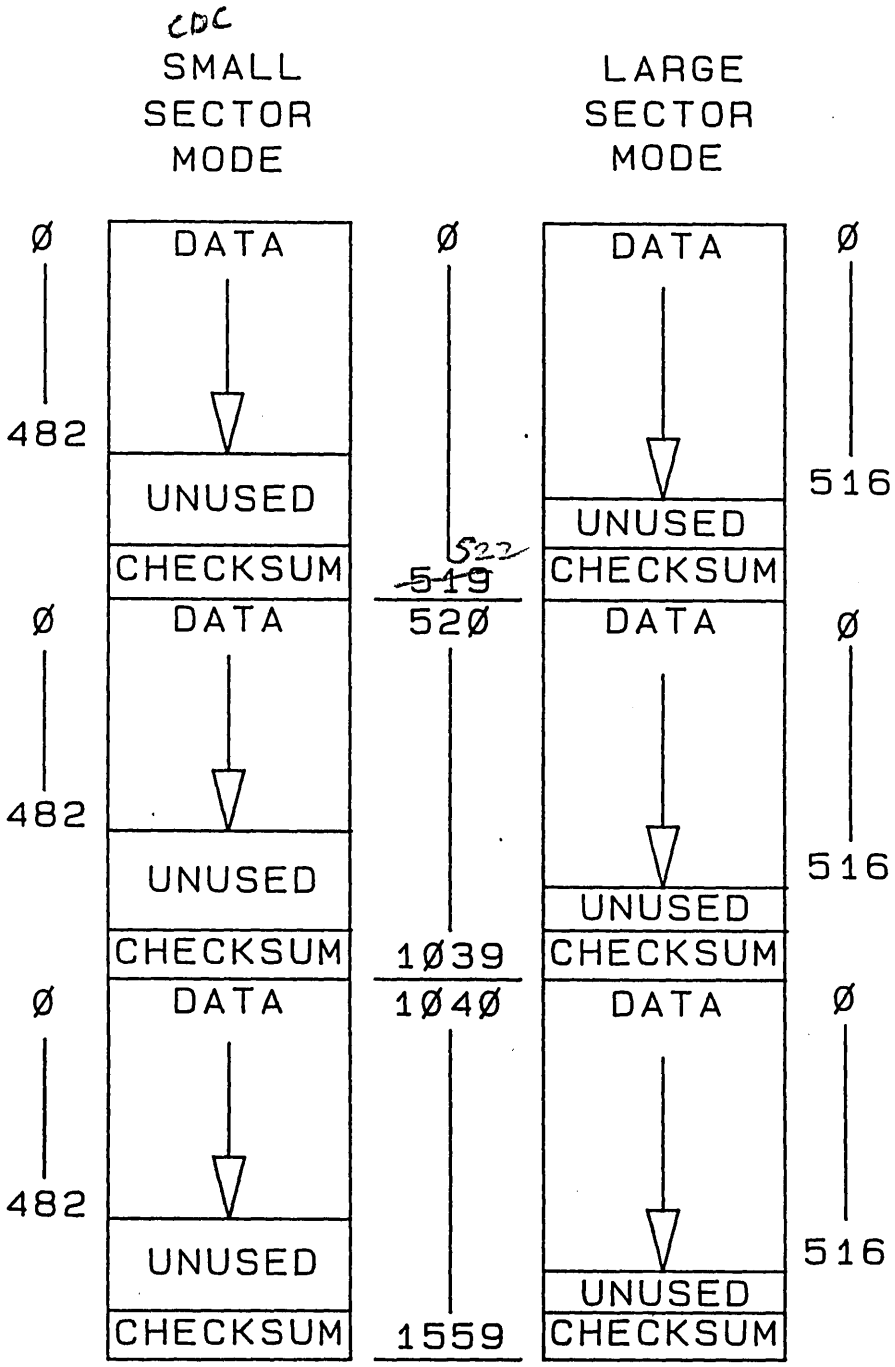
Upper Codes	Meaning
x2x	HP/A start up error
x4x	Data compare error
x8x	HP/A detected error
1xx	Write error was detected
2xx	Track or Sector compare error detected
4xx	Cylinder compare error detected
8xx	Checkword compare error detected

Lower Codes	Meaning
xx1	No device end before issuing a seek cmd
xx2	U-Bus parity error
xx3	No status after a seek command
xx4	Recovery action of 4, Command Reject
xx5	Status action 'F' returned
xx6	Command aborted
xx7	Time-out data on U-Bus

Write Errors	Meaning
xx8	Unexpected status present
xx9	Unexpected data present on U-Bus
xxA	Amperif did not take command word
xxB	Enable tags not set to accept address word
xxC	Amperif did not take address word
xxD	Amperif status presented on entry to write routine
xxE	HP/A time-out waiting for ODR signal
xxF	HP/A time-out, Amperif stopped accepting data
x10	HP/A time-out waiting for Amperif status
x11	Amperif abnormal write termination (see EI)

Read Errors	Meaning
x12	Amperif status present on entry to read routine
x13	Amperif status present after read command issued -- chk power or drive spinning
x14	Enable tags not set to accept address word
x15	HP/A time-out waiting on IDR signal
x16	Amperif terminated read before sending data
x17	HP/A time-out Amperif stopped sending data
x18	HP/A time-out waiting for Amperif status
x19	Amperif abnormal read termination
x1A	Enable tags not present on entry to truncation rtn
x1B	HP/A time-out Amperif did not accept all data
x1C	Amperif input data present on entry to issue cmd

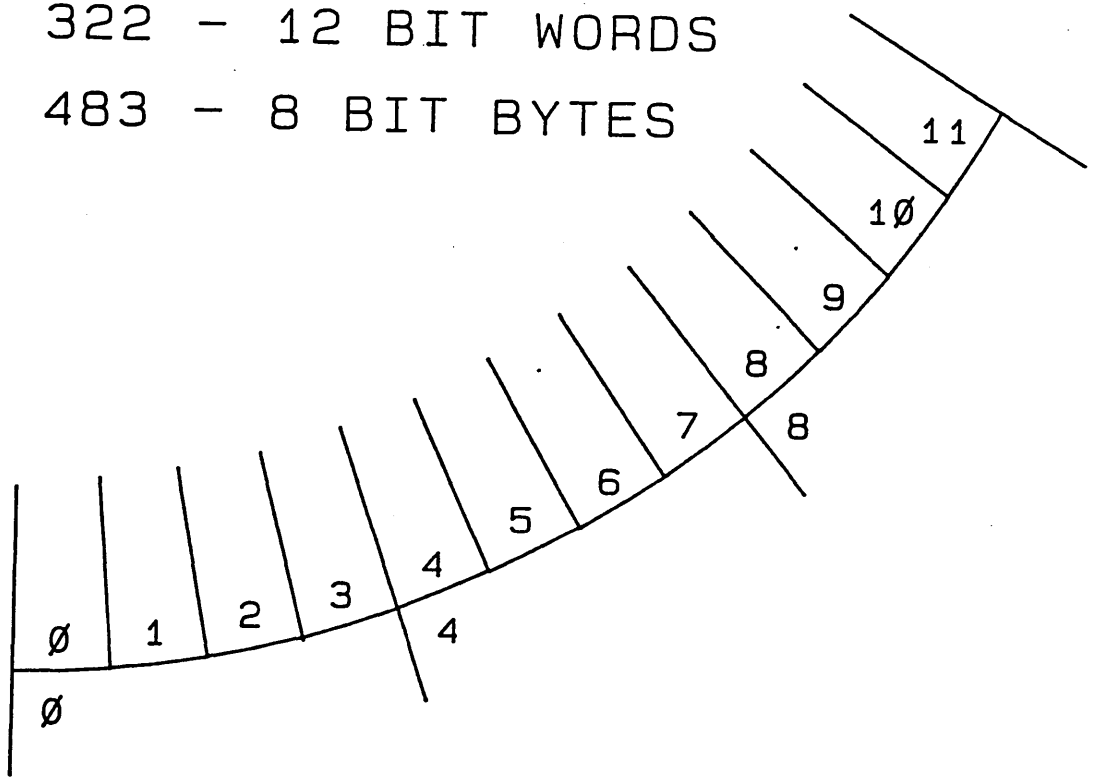
DATA PARTITIONS



SMALL SECTOR

322 - 12 BIT WORDS

483 - 8 BIT BYTES

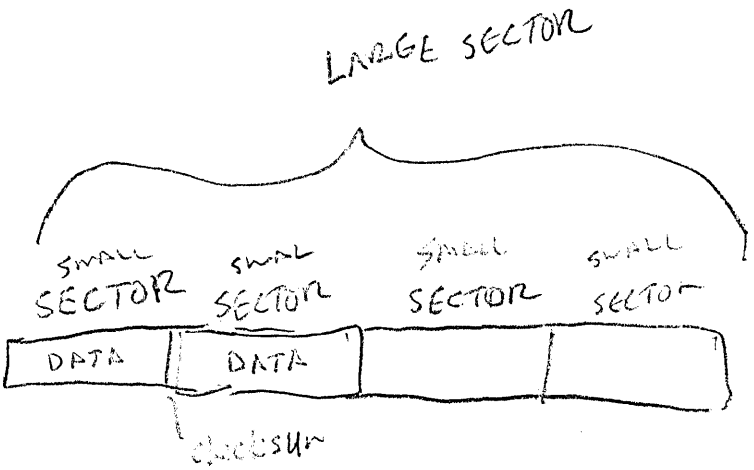


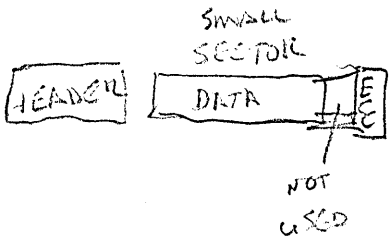
LARGE SECTOR

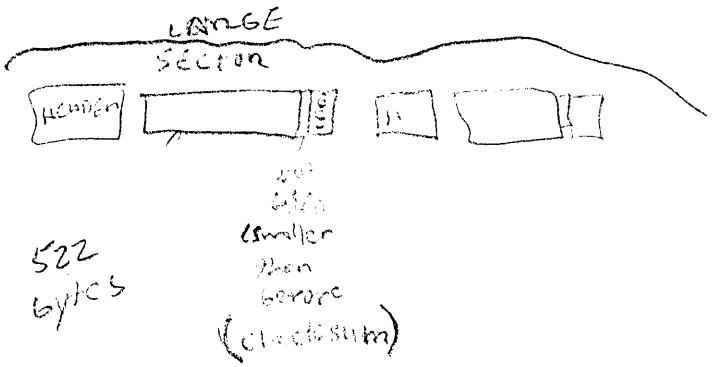
1376 - 12 BIT WORDS

2Ø64 - 8 BIT BYTES

CDC







records are formatted as large sector in AMPEX

CDC requires reformat of pack to change large ↔ small

5.4.4 Console Commands

Descriptions of the following commands are included in this section:

- o System Display Commands
- o Dayfile Commands
- o Job Processing Control Commands
- o Equipment Control Commands
- o Subsystem Control Commands
- o System Control Commands
- o Memory Entry Commands
- o Channel Control Commands

DSD is an interpretive display driver; When a console operator is typing a command, DSD completes the command as soon as it recognizes enough characters to establish the uniqueness of the command. DSD does not accept or display invalid characters.

The system displays are selected by the command. An example follows:

xy. CR

where x and y represent the letter designations of the displays; x appears on the left and y appears on the right.

Letter	Description
A	Dayfile display. This is a chronological history of system operations. It includes the system display (A,. or A.), the account display (A,ACCOUNT FILE.), the error log display (A,ERROR LOG.), the operator message display (A,OPERATOR), and the job dayfile display (DAYFILE,jsn.).
B	System status display. This is the current status of all jobs assigned to control points. It includes the system status displays (B.O. and B,A.).
C,D	Central memory display. These are portions of the contents of central memory in five groups of four octal digits and their display code equivalents.
E	Equipment status display. This is the status of peripheral devices. It includes the equipment status table display (E,. or E.A.), the disk configuration display (E,C.), the family status display (E,F.), the disk status display (E,M.), the resource requests display (E,P.), and the tape status display (E,T.).
F,G	Central memory display. These are the portions of the contents of central memory in four groups of five octal digits and display code equivalents.
J	Individual job status display. Status of the specified job sequence name.
K	CPU programmable display. This is the dynamic operator/CPU program communication.
P	PP registers display. Current contents of PP registers or PPs active for a particular job.
Q	Queue status display. Status of active input and output queues in the queued file table. This includes all Queues (Q.), input queue (Q,IN.), plot queue (Q,PL.), print queue (Q,PR.), punch queue (Q,PU.), or wait queue (Q,WT.).
R	Rollout queue status display. Current status of all executing jobs including those that the system has rolled out.

Letter	Description
T	Interactive status display (IAF). Status of interactive users.
W	System information display. Status of the system. Includes channel status (W,C.), request queues (W,Q.), resource information (W.R.), and miscellaneous parameters (W,M.).
Y	Monitor function display. List of all monitor function mnemonics and codes.
Z	Directory display. List of the latter designations and description of all DSD displays.

There are a few special first character entries which are explained below.

Character	Description
*	Alternates display control between DSD and another console program each time * key is pressed.
+	Advances left screen display. For E,Q,R,S,T, or W display, advances to the next page of display. For memory display (C,D,F, or G), advances display address by 40 octal locations.
-	Reverses left screen display. For E,Q,R,S,T, or W display, reverses to previous or first page of display. For memory display (E,D,F, or G), decrements display address by 40 octal locations.
(	Advances right screen as described for + key.
)	Reverses right screen as described for - key.
CR	Carriage return key. Sets repeat entry flag. Subsequent entry is processed, but not erased after completion. Flag is cleared by pressing left blank key.
left blank	Clears current keyboard entry and any resultant error messages.
BKSP	Deletes last character entered and clears error message if one exists.
CR	Initiates processing of command entered.

System Display Commands

Command	Description
m,jsn	Sets display m (C,D,F,G,J, or K) to display only information for job with job sequence number jsn.
xz,addr.	x = letter designation of a storage display (C,D,F, or G). z = type of display modification. 4 changes the entire display to display the memory contents beginning at location addr. 5 increments the display by addr locations. 6 decrements the display by addr locations.

Dayfile Commands

Command	Description
A.	Resets the A display to the beginning of the dayfile buffer.
A,.	Resets the A display to the system dayfile when the error log account dayfile, or a job dayfile is currently being displayed.
A,ACCOUNT FILE.	Displays the account dayfile buffer on the left screen.
A,ERROR LOG.	Displays the error log buffer on the left screen.
A,OPERATOR.	Displays system messages to the operator.
DAYFILE,jsn.	Displays the dayfile buffer for the job with job sequence name jsn.
LOG,ord.	Clears message ord from A,OPERATOR display.

Job Processing Control Commands

Command	Description
DROP,jsn.	Drops job with job sequence name jsn.
KILL, jsn.	Kills job with job sequence name jsn.
OVERRIDE,jsn.	Drops job with job sequence name jsn.
ROLLIN,jsn,L.	Allows job with job sequence name jsn to be scheduled to a control point. L is optional; if omitted, the job can be selected by the scheduler for rollout.
ROLLOUT,jsn.	Causes job with job sequence name jsn to be rolled out and remain rolled out until the operator rolls the job in via the ROLLIN command or terminates it via the DROP, KILL, or OVERRIDE command.
ROLLOUT,jsn,n.	Causes job with job sequence name jsn to be rolled out and remain rolled out for n scheduler cycles. When n scheduler cycles have elapsed, the job becomes eligible for scheduling.
GO,jsn.	Clears the pause and status flags for job with job sequence name jsn.

Equipment Control Commands

Command	Description
ASSIGN,jsn,est.	Assigns device with EST ordinal est to job with job sequence name js.
DOWN,CHcc	Discontinues use of channel cc for all I/O operations. If channel cc is the only channel available to a mass storage device, its use is not discontinued for that device.
DOWN,EQest.	Discontinue use of device with EST ordinal est for all channels.
OFF,est.	Logically turns off device with EST ordinal est.
ON,est.	Logically turns on device with EST ordinal est.
UNLOAD,est.	Physically unloads the magnetic tape on EST ordinal est or logically remove the removable mass storage device on EST ordinal est from the operating environment while the operator dismounts a tape or disk pack.
UP,CHcc	Reverses the effect of DOWN command for channel cc and resumes normal use of the channel for all tape and mass storage I/O operations.
UP,EQest.	Reverses the effect of DOWN command for device with EST ordinal est. Device remains in OFF state.
VSN,est.	Clears current VSN for tape unit with EST ordinal est and checks if a VSN is specified on the tape. Valid only if the unit is not currently assigned.
VSN,est,vsn.	Assigns one- to six-character VSN vsn to magnetic tape unit with EST ordinal est.

Subsystem Control Commands

Command	Description
IAF.	Initiates the interactive facility subsystem.
IDLE,sub.	Terminates the subsystem sub.
MAG.	Initiate the magnetic tape subsystem.
NAM.	Initiates the network access method subsystem.
STOP,sub.	Drops (terminates) subsystem sub.

System Control Commands

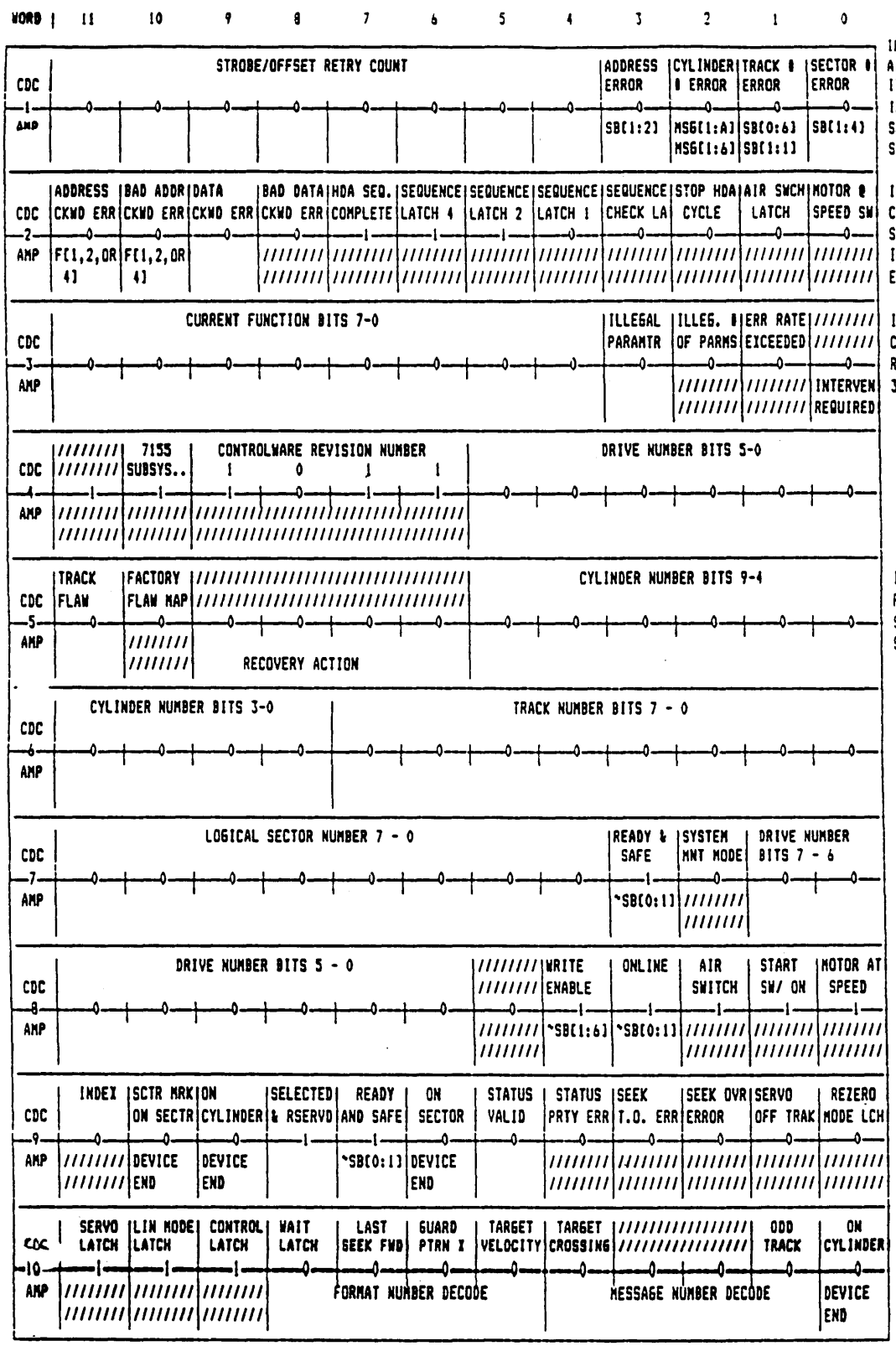
Command	Description
AUTO.	Initiates all currently enabled subsystems to control points and initiates automatic job processing.
CHECK POINT SYSTEM.	Rolls out all jobs and transfers contents of central memory tables to mass storage.
DIS,jsn.	Initiates job display package (DIS) to job with job sequence name jsn. (Console keyboard must be unlocked.)
LOCK.	Locks the console keyboard.
MAINTENANCE.	Performs the same functions as the AUTO command, but also initiates several maintenance service class jobs to perform online hardware checkout.
STEP.	Sets monitoring step mode. Stops all central memory I/O operations and prevents the system from processing PP requests when the next monitor function is encountered.
UNLOCK.	Unlocks the console keyboard.
UNSTEP.	Clears step mode. (Console keyboard must be unlocked.)

Memory Entry Commands (These commands can only be entered when the location to be changed is currently displayed on the left screen.)

Command	Description
loc,val.	Changes contents of central memory location loc to val (20 digits).
loc,b,val.	Changes contents of byte b at central memory location loc to val.

Channel Control Commands

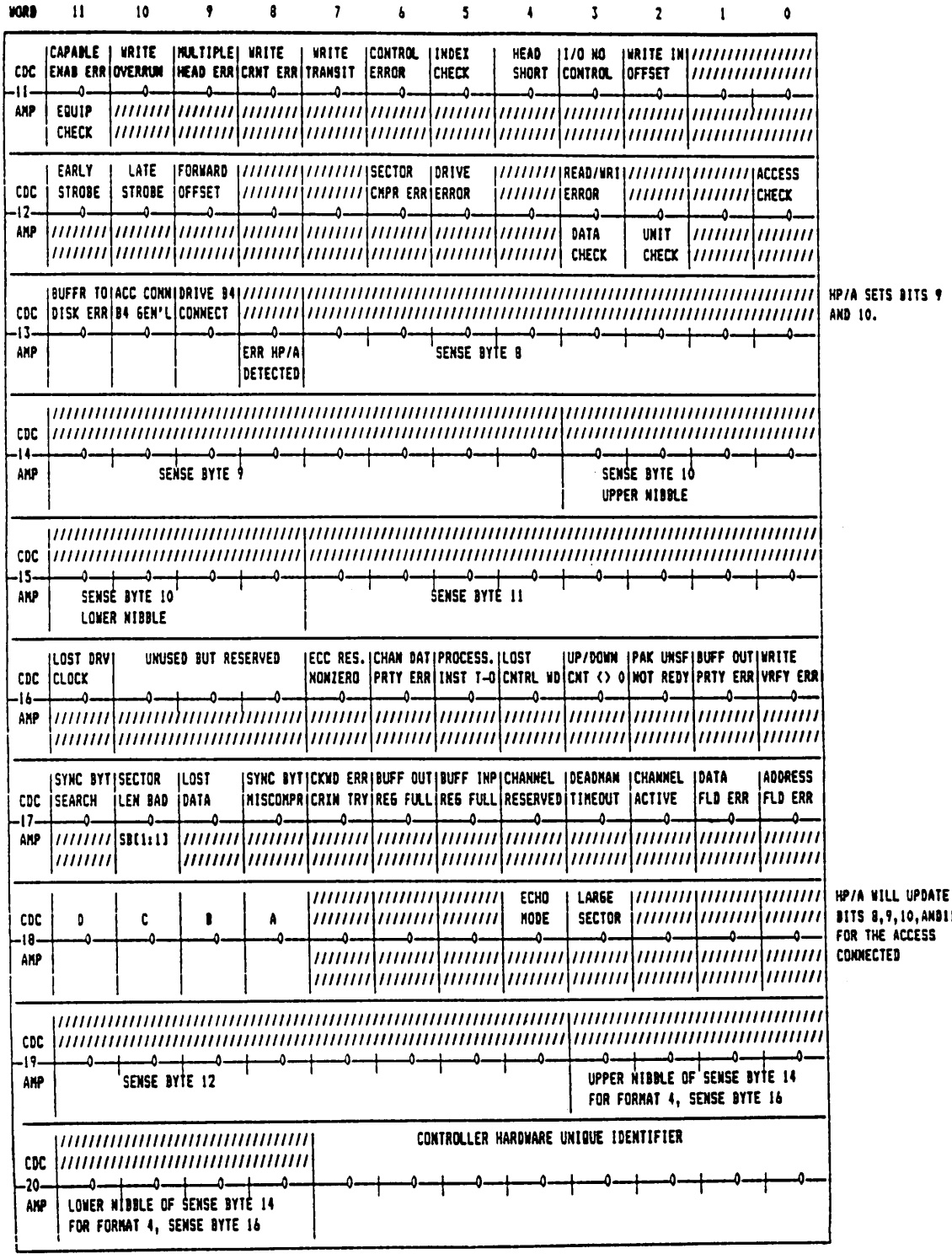
Command	Description
ACN,cc.	Activates channel cc.
DCN,cc.	Deactivates channel cc.
FCN,cc,func.	Outputs functions code func to channel cc. If func is not specified, this command outputs a zero function code (no activity) to channel cc.
IAN,cc.	Inputs to pseudo A register from channel cc.
LDC,nnnn.	Loads pseudo A register with nnnn. (nnnn is normally a peripheral equipment function code.)
OAN,cc.	Outputs contents of pseudo A register to channel cc.



NOTES:

(1) Wherever you see a tilde ( ), read "not".
(2) SB[x:y] means Amperif sense byte x, bit y.
(3) MSG[j:k] means Amperif sense byte 7, format j, message k.
(4) FSB[n:x:y] means Amperif format n sense byte x, bit y.
(5) WD[m:n] means CDC extended status byte m, bit n.

Figure 5-2
CDC Extended Status Report (part 1 of 2)



NOTES:

(1) Wherever you see a tilde ( ), read "not".
(2) SB[x:y] means Amperif sense byte x, bit y.
(3) MSG[j:k] means Amperif sense byte 7, format j, message k.
(4) FSB[n:x:y] means Amperif format n sense byte x, bit y.
(5) WD[m:n] means CDC extended status byte m, bit n.

Figure 5-3
CDC Extended Status Report (part 2 of 2)

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DSD Displays 4

Display Selection 4-1

Display Screen Headers 4-3

Dayfile Displays (A) 4-4
- System Dayfile Display (A. or A,.) 4-7
- Account Dayfile Diaplay (A,ACCOUNT FILE.) 4-8
- Error Log Display (A,ERROR LOG.) 4-9
- Operator Action Display (A,OPERATOR.) 4-10
- Job Dayfile Display (DAYFILE,jsn.) 4-12

System Status Displays (B,A. and B,O.) 4-13

Storage Displays (C, D, F, G, and M) 4-19

Equipment Status Displays (E) 4-24

Equipment Status Table Display (E,. or E,A.) 4-24
- Disk Configuration Display (E,C.) 4-28
- Disk Errors Display (E,E.) 4-30
- Family Status Display (E,F.) 4-33
- Disk Thresholds Display (E,H.) 4-35
- Disk Status Display (E,M.) 4-37
- Resource Requests Display (E,P.) 4-41
- Tape Status Display (E,T.) 4-44

System and Local Files Display (H) 4-47
- BIO Status Display (I) 4-50
- Job Status Display (J) 4-52

Central Programmable Display (K) 4-54

Transaction Facility (TAF) Displays (O) 4-55
- Subcontrol Point Status Display (O,SCP.) 4-56
- Task Library Directories Display (O,TLD.) 4-58
- TAF Status Table Display (O,TST.) 4-60

PP Registers Display (P) 4-62

Queue Status Displays (Q) 4-64

Rollout Status Display (R) 4-67

System Control Display (S) 4-70

Interactive Status Display (T) 4-74

System Information Displays (W) 4-76

Memory Allocation Display (W,A.) 4-76
- Channel Status Display (W,C.) 4-78
- Miscellaneous Parameters Display (W,M.) 4-81
- System Queues Display (W,Q.) 4-82
- System Resources Display (W,R.) 4-84

Monitor Functions Display (Y) 4-86

Directory Display (Z) 4-87

DSD Displays 4

You communicate with the system through the console keyboard. The system provides information about job and system status through displays on the console screens. Data entered from the keyboard is also displayed. You can request a permanent record, called a system dayfile, of all system and console communication.

There are two major display programs: DSD, which generates system-oriented displays, and DIS, which generates job-specific displays. The primary functions of DSD are:

- Maintain a current display of system status.
- Process keyboard entries from the operator.

At the console keyboard, you can:

- Assign equipment to the job.
- Control job scheduling and execution.
- Initiate utility programs through the L display.
- Select displays.

A DSD Display Index is provided at the back of this manual for quick reference. The NOS Version 2 Analysis Handbook describes DIS commands and displays.

Display Selection

Select any of the DSD displays with the console command

xy.

where x and y represent the letter designation of the displays.

Display x appears on the left screen and display y appears on the right. If x and y are identical, both screens display the same information except for the B or P display. A single B display may use both screens on the CC596A and CC634B consoles. The P display uses both screens on the CC545, CC596A, and CC634B consoles.

You can specify a sequence of DSD displays to display on the left screen. To preselect the left screen display sequence, enter the DSD command

SET,screen.

where screen represents letters designating any four DSD displays.

Four display identifiers (see following list) must be specified. Usually you specify four different displays, although DSD accepts any four valid screen identifiers.

After entering this command, press the right blank key (CC545 console), or TAB key (CC596A console), or forward arrow key (CC634B console). The first display specified appears on the left console screen. Press the appropriate key for your console again to select the second display. Each time you press this key, the next display in the specified sequence appears on the left console screen.

The following displays are available under DSD.

Display	Description
A	Dayfile. Chronological history of system operations. There are five subdisplays.
B	System status. Current status of all jobs assigned to control points. There are two subdisplays.
C,D	Central memory. Contents of central memory words (two or four selectable eight-word groups) in five columns of four octal digits with display code equivalents.
E	Equipment status. Status of peripheral devices. There are eight sub-displays.
F,G	Central memory. Contents of central memory words (two or four selectable eight-word groups) in four columns of five octal digits with display code equivalents.
H	System FNT. List of system FNT entries for all fast attach and system files in the system. H,jsn lists the local files for that jsn.
I	BIO status. Status of central site unit record devices.
J	Individual job status. Status of the specified job sequence name.
K	CPU programmable. Dynamic operator and CPU communication. Refer to the NOS Version 2 Analysis Handbook for further information.
L	CMR buffer interface programmable. System utility interface communication. Refer to chapter 5 for further information.
M	Extended memory. Contents of 60-bit words of extended memory (two or four selectable eight-word groups) in five columns of four octal digits with display code equivalents.
O	Transaction status. Status of the transaction subsystem. There are three subdisplays.
P	PP registers. Current contents of PP registers.
Q	Queue status. Status of active input and output queue in the queued file table. There are six subdisplays.
R	Rollout status. Status of all executing jobs.
S	System control information. Parameters used to control job flow.
T	IAF status. Status of interactive users.
W	System information. Memory allocation, channel status, request queues, resource information, and miscellaneous parameters. There are five subdisplays.
Y	Monitor functions. List of all monitor mnemonics and codes.
Z	Directory. List of the letter designators and descriptions of all DSD displays.

6. REFERENCE

This section provides a reference for the following:

	page
1. AIO	6.2
2. AIX	6.3
3. BIOE	6.4
4. BIX	6.5
5. CDCI (CDC Interface)	6.6
6. DIFE (Disk Interface Expansion)	6.7
7. EXXP	6.9
8. HSP (High-Speed Processor)	6.10
9. MDBP	6.11
10. MPCP (Microprogram Controller Plugin)	6.13
11. OCP (Operator Control Panel)	6.15
12. UBI (U-Bus Interface)	6.17
13. XMCIP (Expanded Microcontroller Interface Plugin)	6.18
14. XMCP (Expanded Microcontroller Plugin)	6.20
15. XM16KP (Expanded Memory 16K Plugin)	6.27

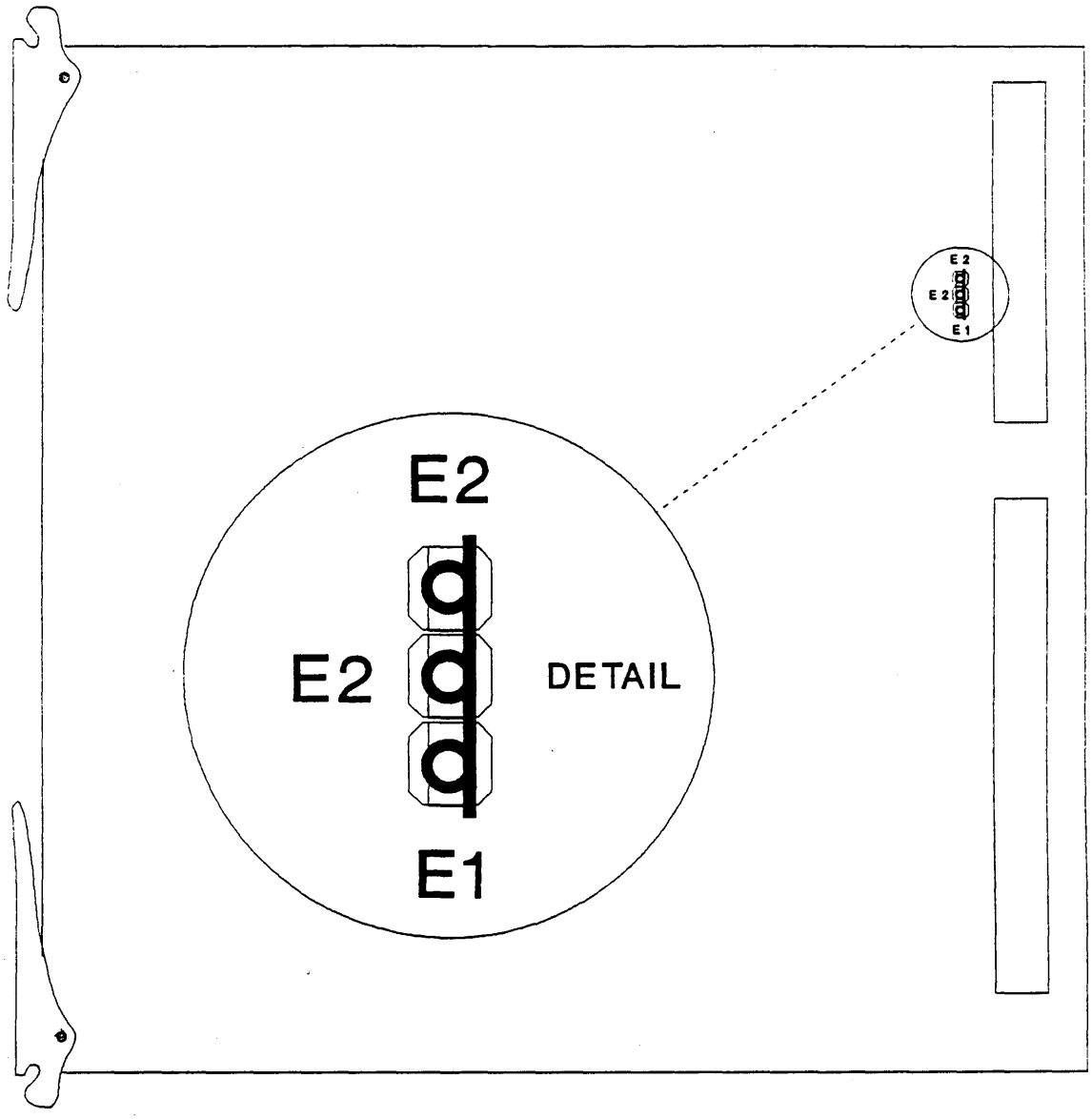


Figure 6-1
AIO Jumpers

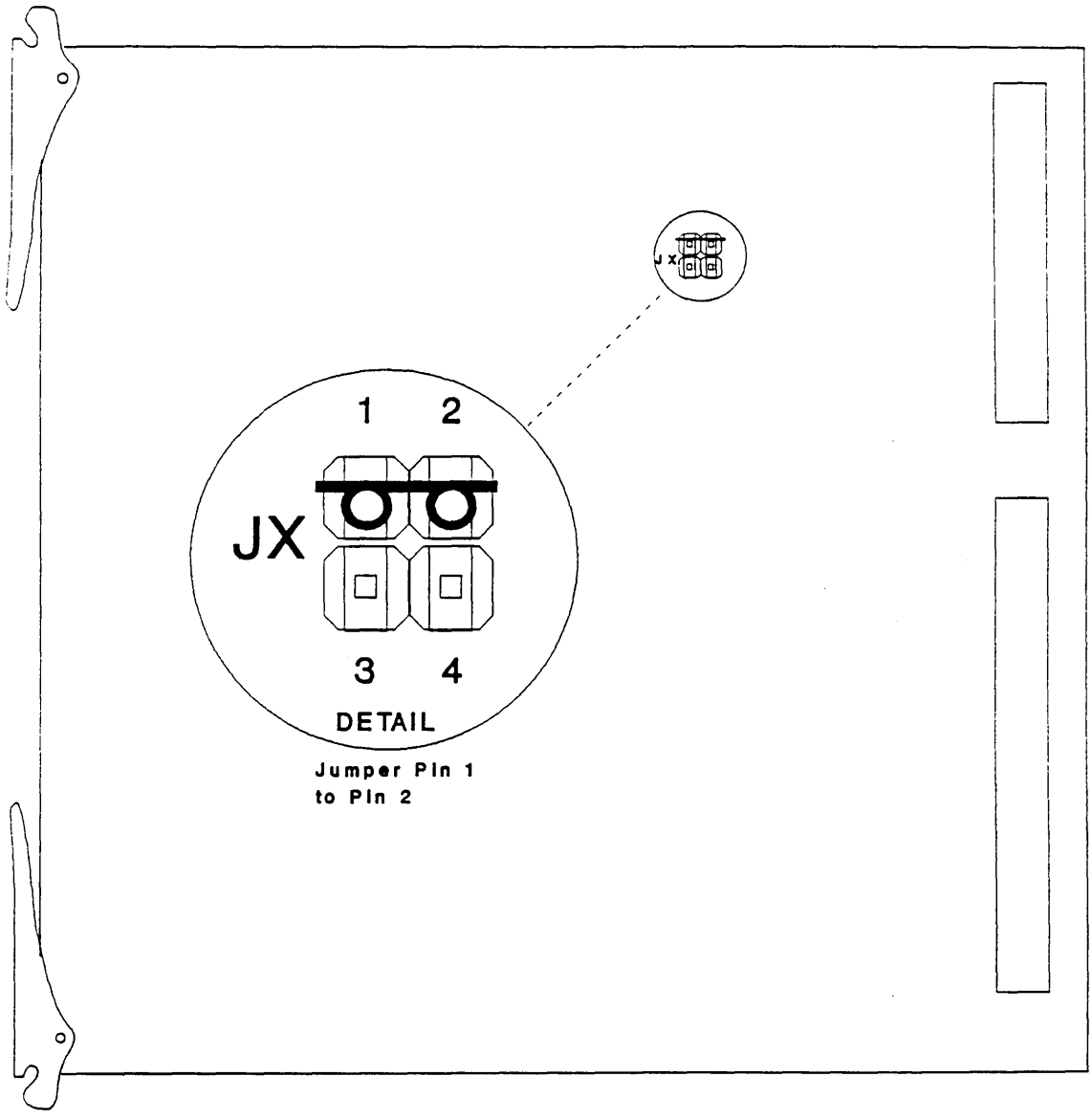
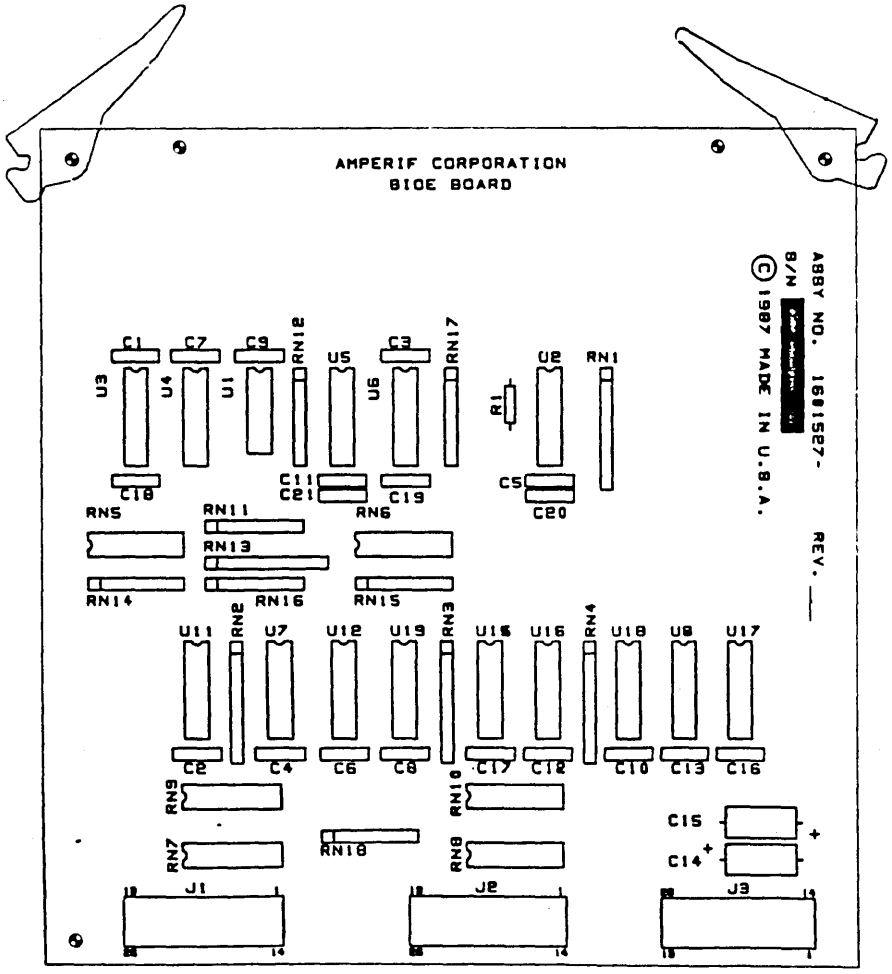


Figure 6-2
AIX Jumpers



COMPONENT SIDE

NO JUMPERS

Figure 6-3
BIOE

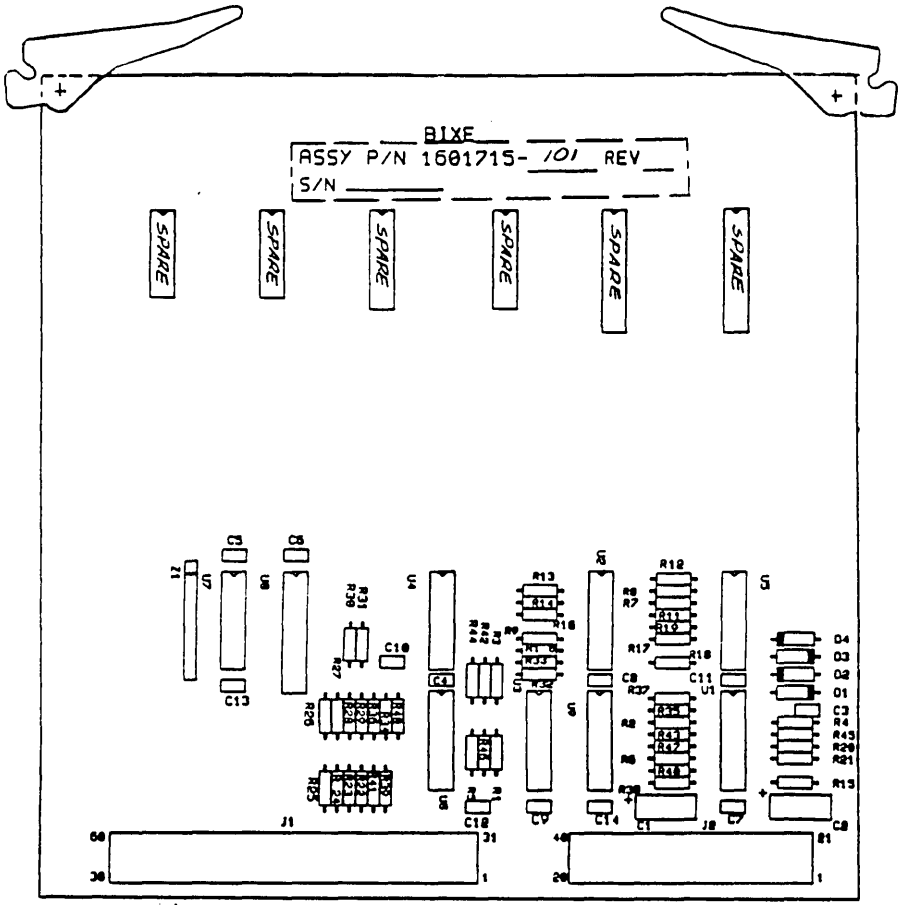


Figure 6-4
BIX

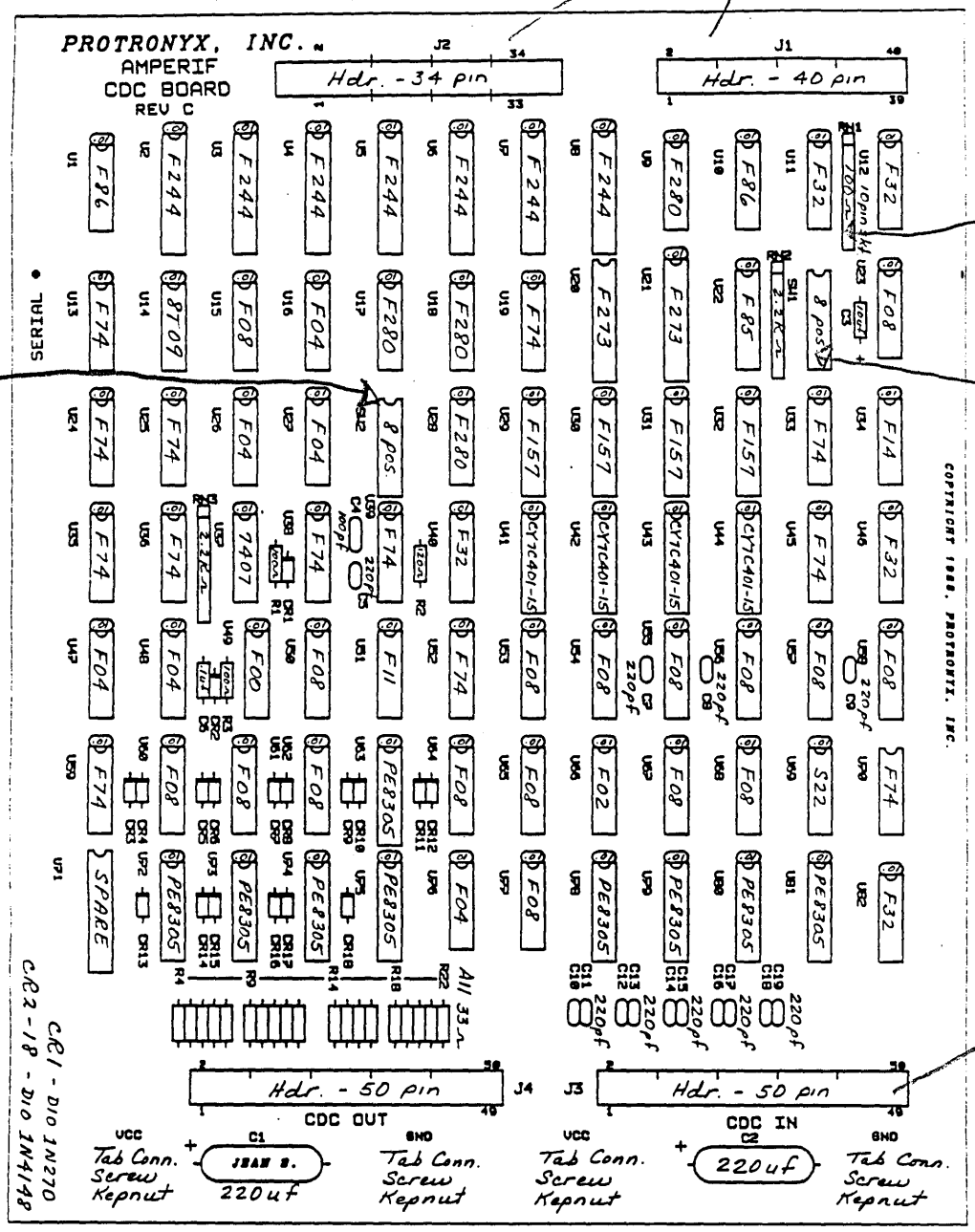


Figure 6-5
CDCI

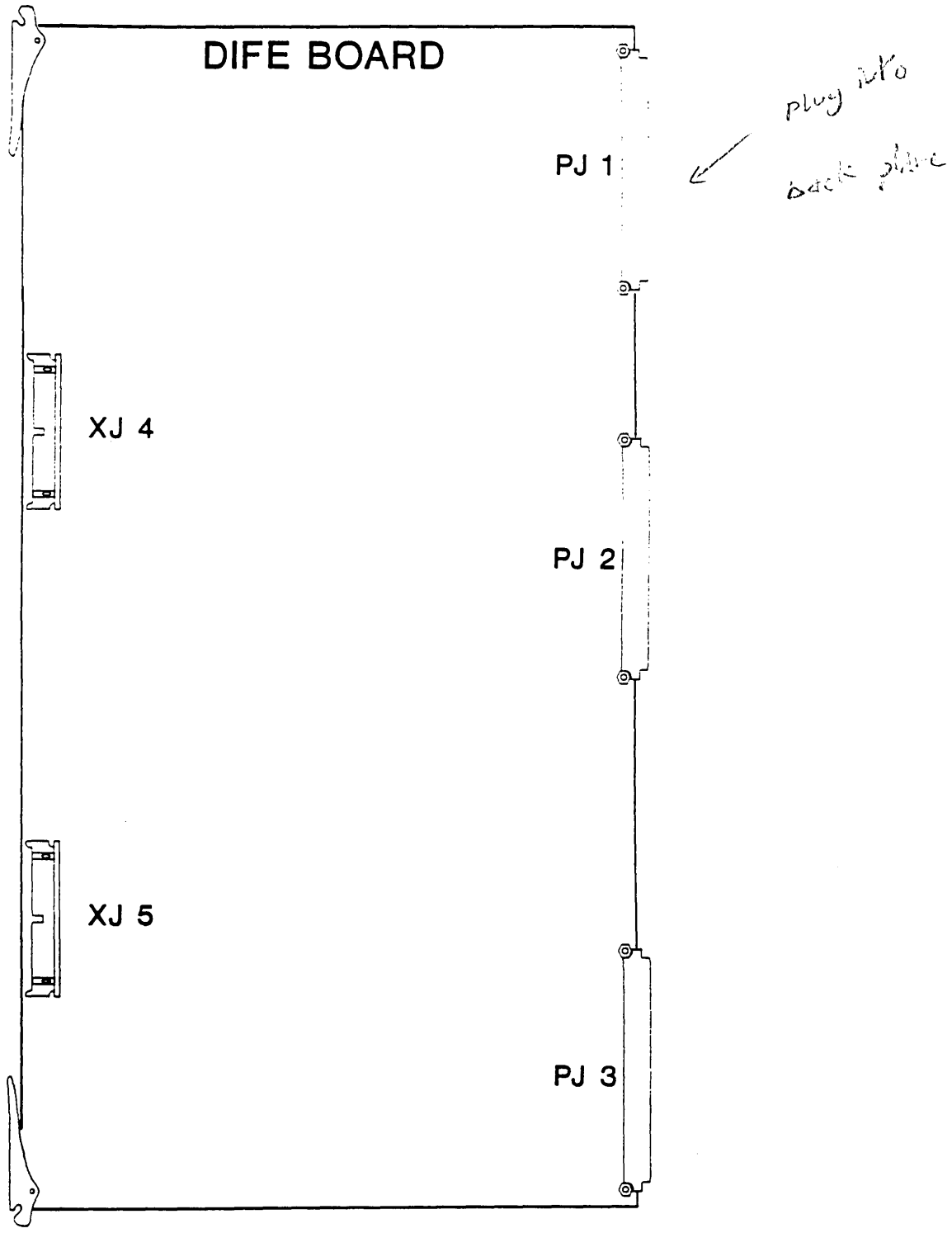
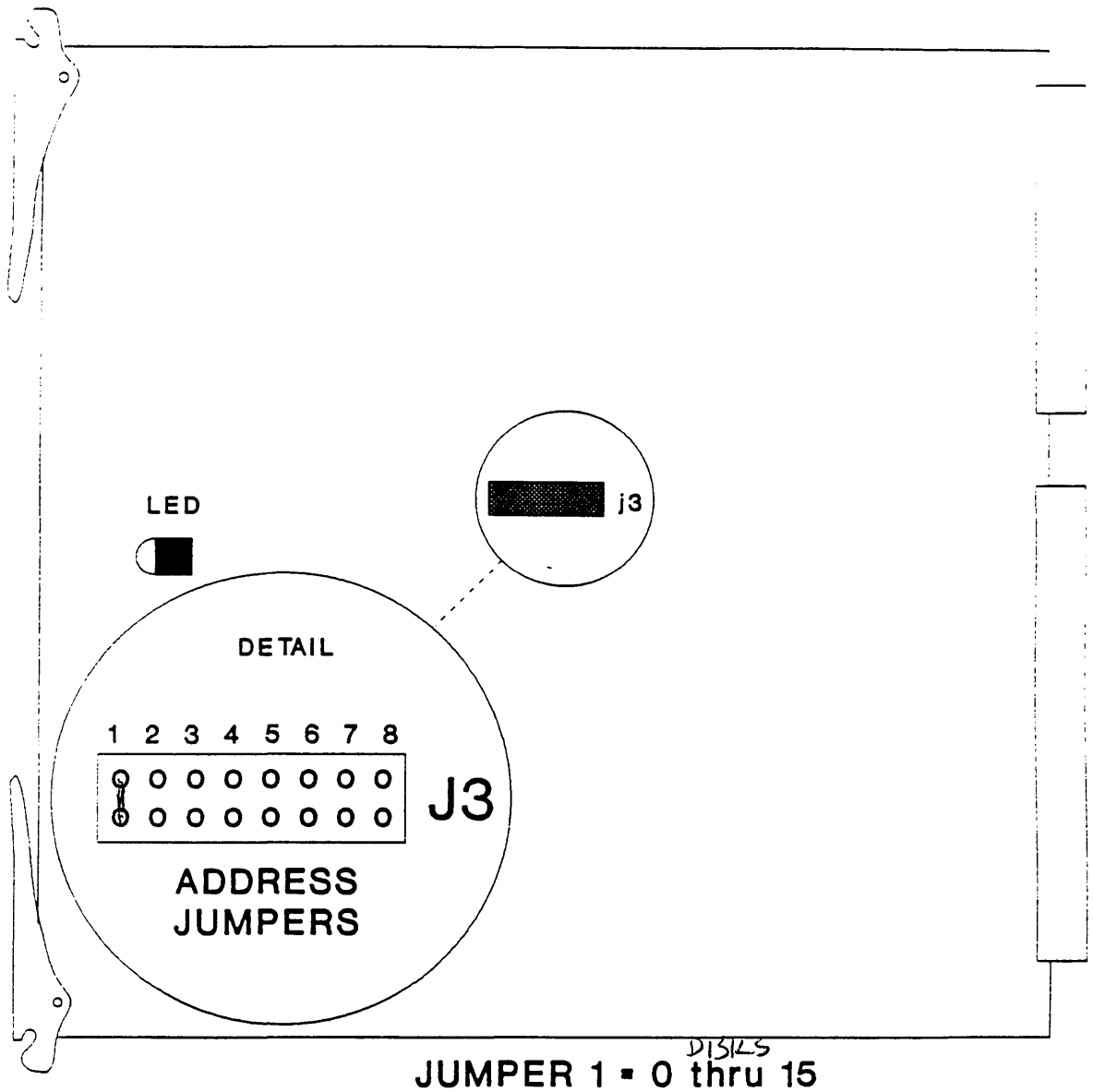


Figure 6-6
DIFE Test Points

DIFE TEST POINTS

Test Points	Signal Name	Purpose
J4A-01	3INDEX	Index mark
J4A-02	4AMDET	Address mark detected.
J4A-03	4RETRY	
J4A-04	9DIFER	DIFE error - indicates DIFE experienced an error during operation.
J4A-05	9OPCMPL	Operation completed normally.
J4B-01	4FILB00	File bus bits 00-07. ← inputs file register
J4B-02	4FILB01	
J4B-03	4FILB02	
J4B-04	4FILB03	
J4B-05	4FILB04	
J4B-06	4FILB05	
J4B-07	4FILB06	
J4B-08	4FILB07	
J5A-01	9DRCLK	Drive clock - can be either read clock or servo clock from drive.
J5A-02	9SMDATI	Storage module data in - serial read data line
J5A-03	9SMDATO	Storage module data out - serial write data line
J5A-04	N/A	
J5A-05	4ENWRTGTE	Enable write gate at drive.
J5A-06	4ENRDGT	Enable read gate at drive.
J5A-07	4ENAM	Enable address mark detect at drive.
J5A-08	9SMDATA	
J5B-01	4FRWST00	
J5B-02	4FRWST01	
J5B-03	4FRWST02	
J5B-04	4FRWST03	
J5B-05	4ABREGEQ	
JB5-06	4ECC100	
JB5-07	4ECC101	
JB5-08	4ECC102	
JB5-09	4ECC103	
JB5-10	3ENFMWT	Enable format write.
JB5-11	3ENRDHDA	Enable read header.

NOTE: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.



AS SHOWN 1 DISKS 0-15

2 DISKS 16-31

Figure 6-7
EXXP Jumpers

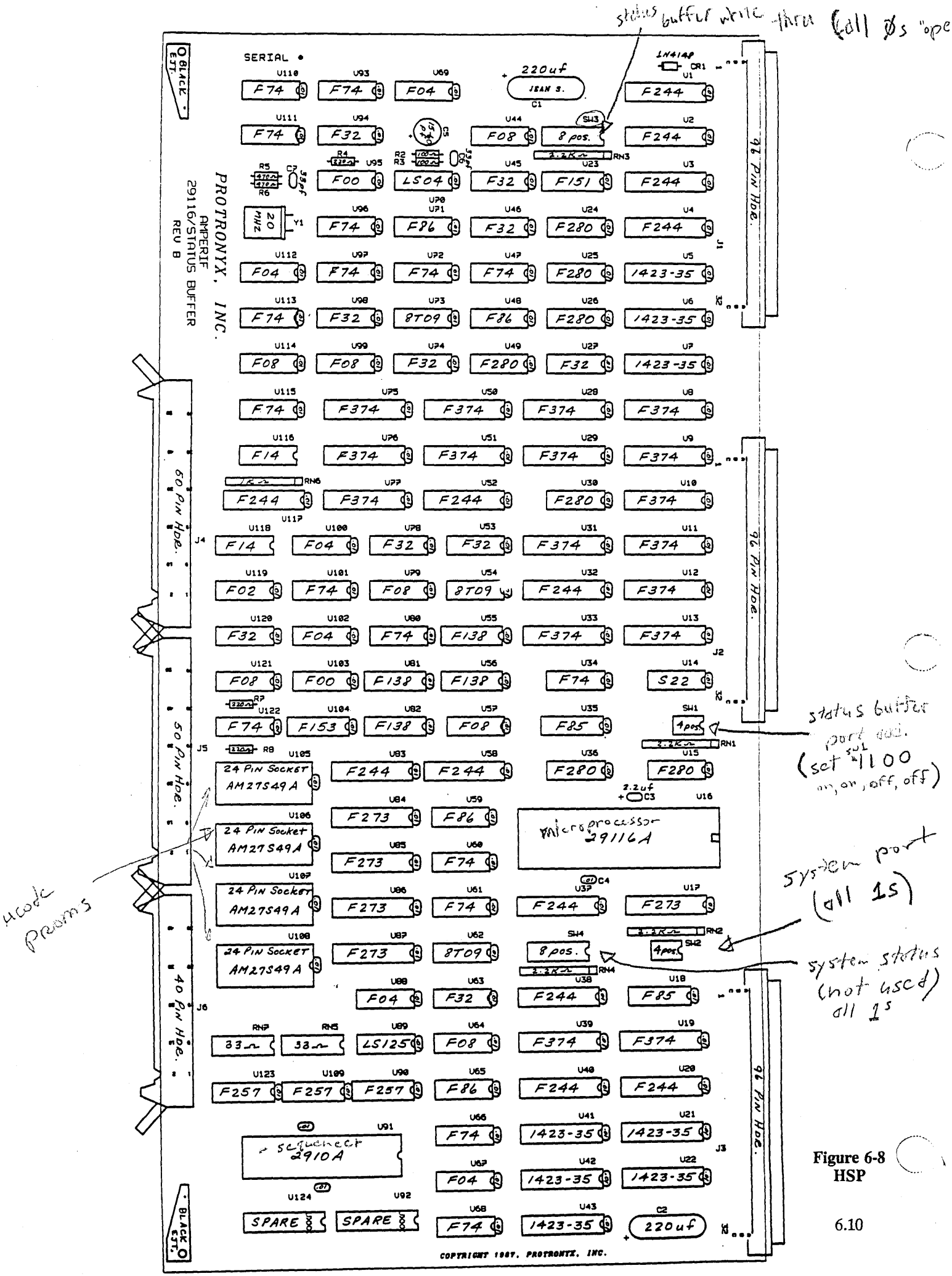


Figure 6-8
HSP

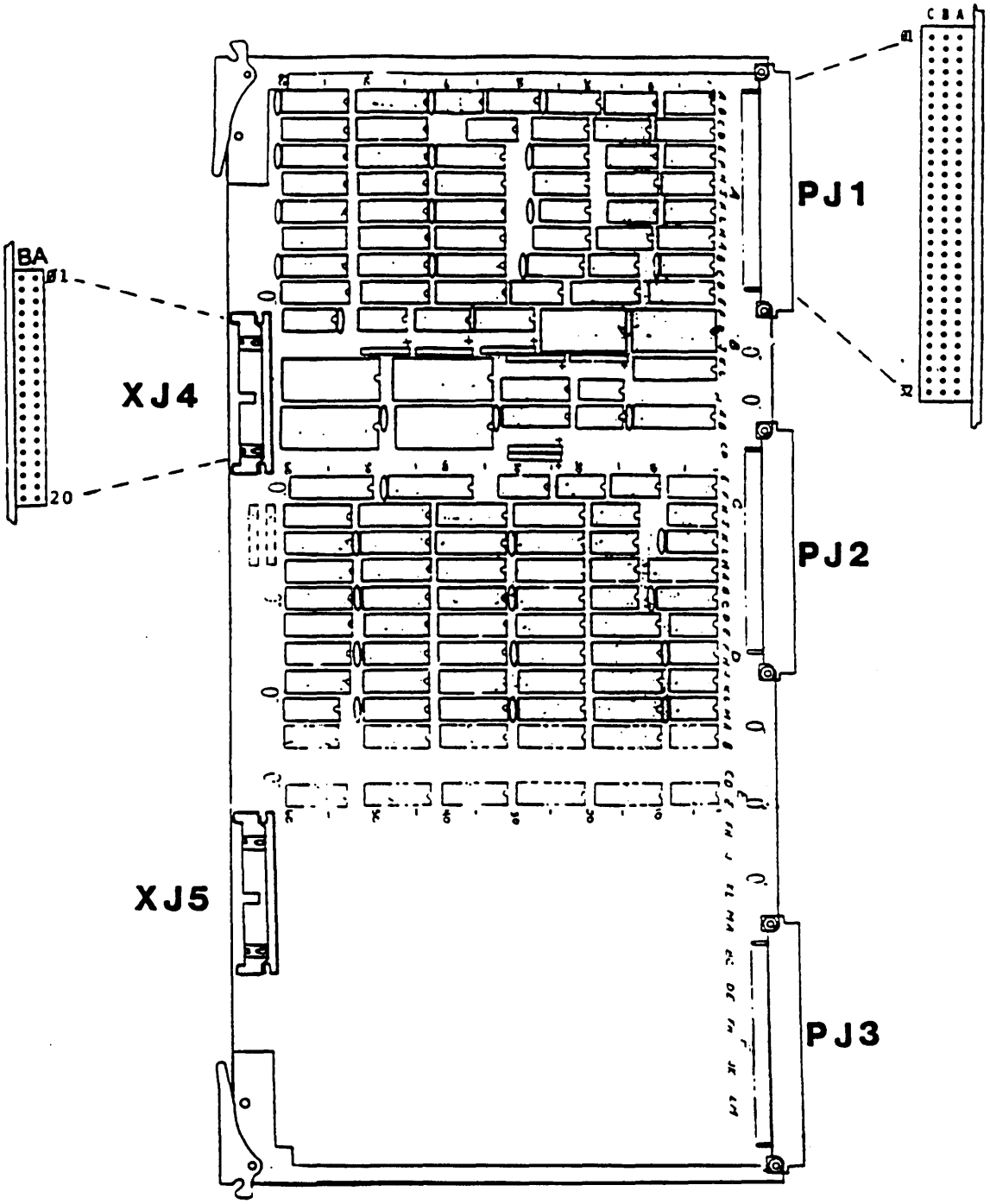


Figure 6-9
MDBP

MDBP TEST POINTS

Test Points	Signal Name	Purpose
J4A-01	7WDCNT00	HSSM Control Signals
J4A-02	7WDCNT01	
J4A-03	2UBREQ	
J4A-04	2BWCI00	
J4A-05	2BWCI01	
J4A-06	2BWCI02	
J4A-07	2BWCI03	
J4A-08	2UDONE	
J4A-09	2UCMPL	
J4A-10	7USREQMC	
J4A-11	7DMCTSEQ	
J4A-12	7MDBACK	
J4A-13	9HREQMC	
J4A-14	3MDBMDEO	
J4A-15	3MDBMDEI	
J4A-16	N/A	
J4A-17	N/A	
J4A018	2SMCMPL	
J4A-19	2SDONE	

Test Points	Signal Name	Purpose
J4B-01	2DMAIO00	DMA Address Generator Input Lines
J4B-02	2DMAIO01	
J4B-03	2DMAIO02	
J4B-04	2DMAIO03	
J4B-05	2DMAIO04	
J4B-06	2DMAIO05	
J4B-07	2DMAIO06	
J4B-08	2DMAIO07	

J5A-01	2MAR00	Data Buffer Memory Address Lines
J5A-02	2MAR01	
J5A-03	2MAR02	
J5A-04	2MAR03	
J5A-05	2MAR04	
J5A-06	2MAR05	
J5A-07	2MAR06	
J5A-08	2MAR07	
J5A-09	2MAR08	
J5A-10	2MAR09	
J5A-11	2MAR10	
J5A-12	2MAR11	
J5A-13	2MAR12	
J5A-14	2MAR13	
J5A-15	2MAR14	
J5A-16	2MAR15	

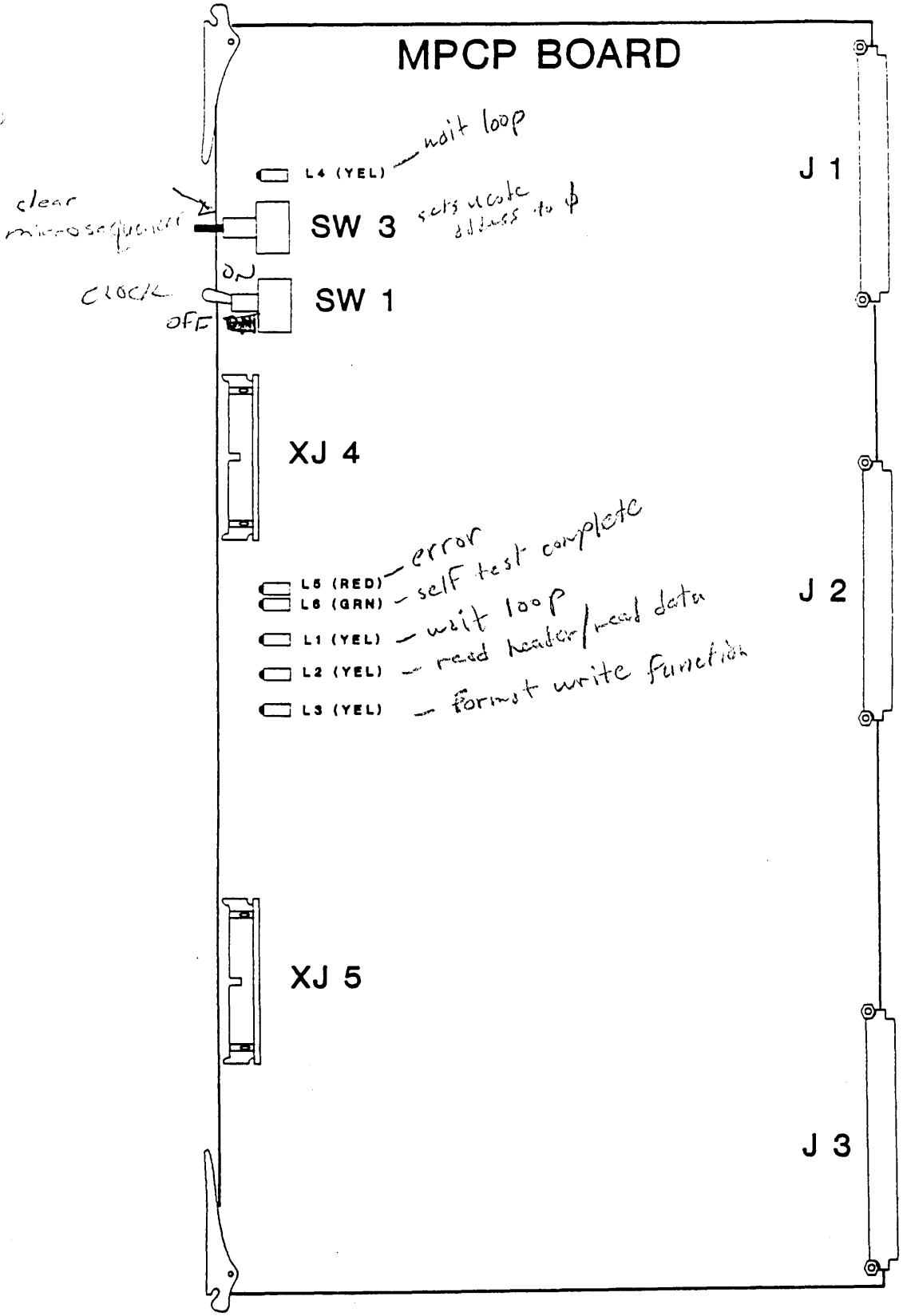


Figure 6-10
MPCP - Layout of Test Points, Switches, and LEDs

MPCP TEST POINTS, SWITCHES AND LEDs

Test Points	Signal Name	Purpose	Test Points	Signal Name	Purpose
J4A-01	3MPC00	MPCP	J4B-01	3ALUO00	
J4A-02	3MPC01	Microprogram	J4B-02	3ALUO01	
J4A-03	3MPC02	Address	J4B-03	3ALUO02	2901B
J4A-04	3MPC03	Lines	J4B-04	3ALUO03	ALU "Y"
J4A-05	3MPC04		J4B-05	3ALUO04	Outputs
J4A-06	3MPC05		J4B-06	3ALUO05	
J4A-07	3MPC06		J4B-07	3ALUO06	
J4A-08	3MPC07		J4B-08	3ALUO07	
J4A-09	3MPC08		J4B-09	3ALUD00	
J4A-10	3MPC09		J4B-10	3ALUD01	
J4A-11	3MPC10		J4B-11	3ALUD02	2901B ALU
J4A-12	3MPC11		J4B-12	3ALUD03	Data Inputs
J4A-13	N/A		J4B-13	3ALUD04	
J4A-14	N/A		J4B-14	3ALUD05	
J4A-15	N/A		J4B-15	3ALUD06	
J4A-16	N/A		J4B-16	3ALUD07	
J4A-17	8MCLKO	MPCP System Clock			

Switches (~~momentary push-buttons~~)

SW1	BD65	BD65-01...8HALT	MPCP clock start/stop switch
	BD65	BE65-01...8RUN	
SW3 (Reset)	AM65	AM65-01...8SWRS0	Clears microsequencer to 0
	AM65	BA65-03...8SWRS0	

LEDs

LED-4 (YELLOW)	3IDLEL	When on, a wait loop condition exists.
LED-5 (RED)	3ERRL	When on, an error has occurred.
LED-6 (GREEN)	3CMPL	When on, self-test has completed successfully.
LED-1 (YELLOW)	3ENMDRDM	When on, a wait loop condition exists.
LED-2 (YELLOW)	3ENRDHDA	When on, the Read Header/Read Data function is active.
LED-3 (YELLOW)	3ENFMWT	When on, the Format Write function is active.

LED3	LED2
0	0 Read Header
0	1 Read Data
1	0 Write Data
1	1 Format

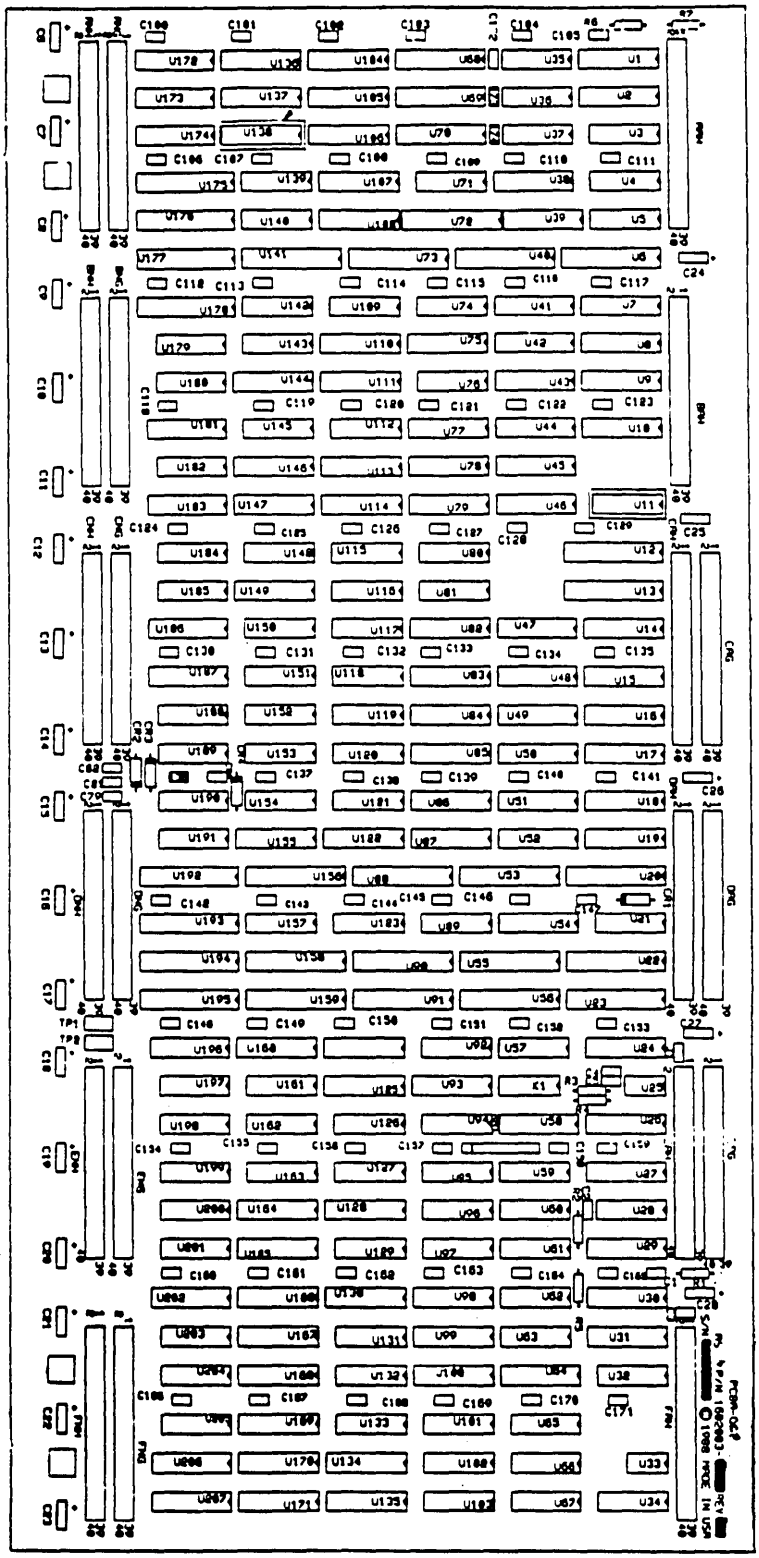


Figure 6-11
OCP
COMPONENT SIDE

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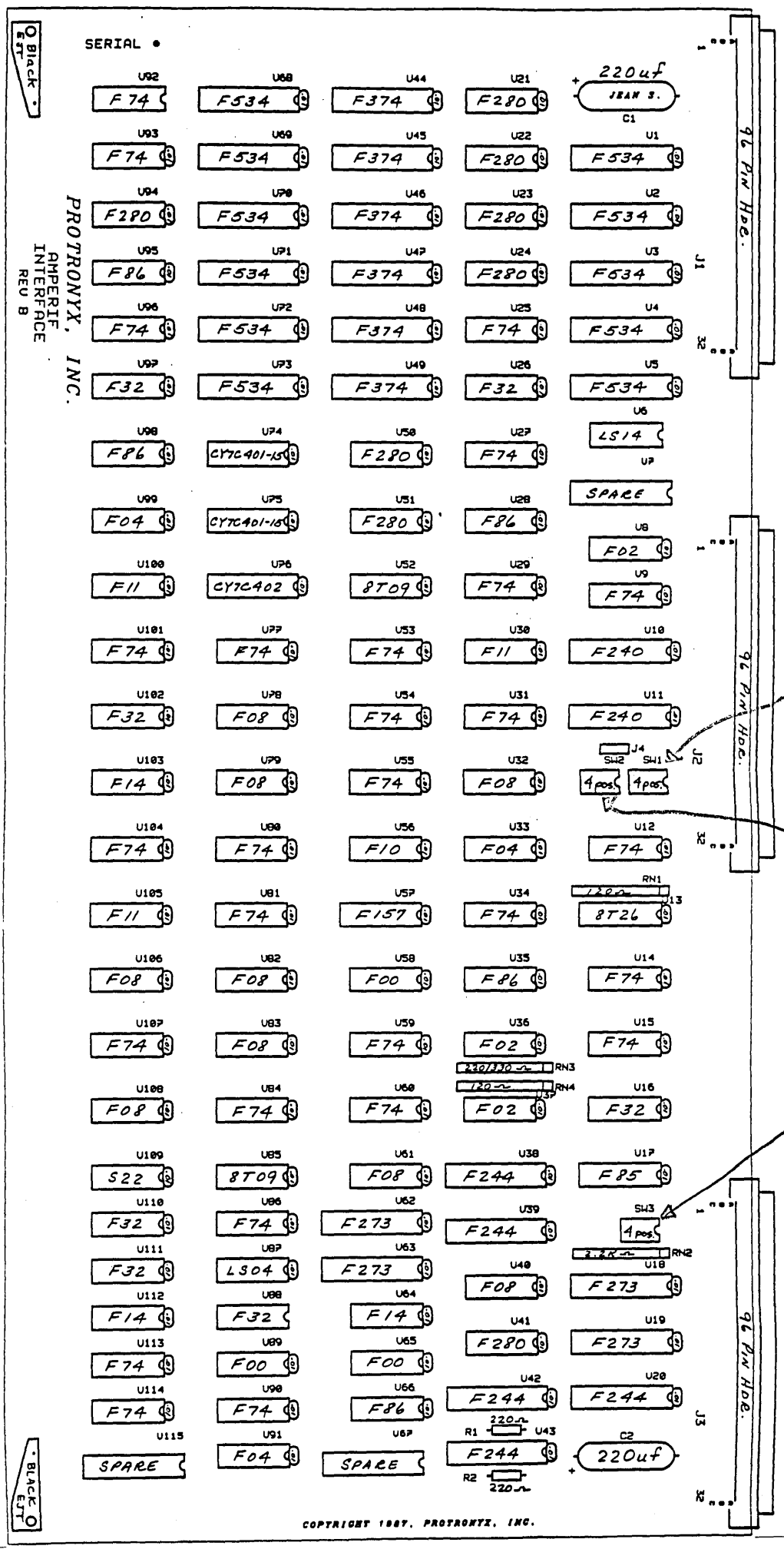


Figure 6-12
UBI

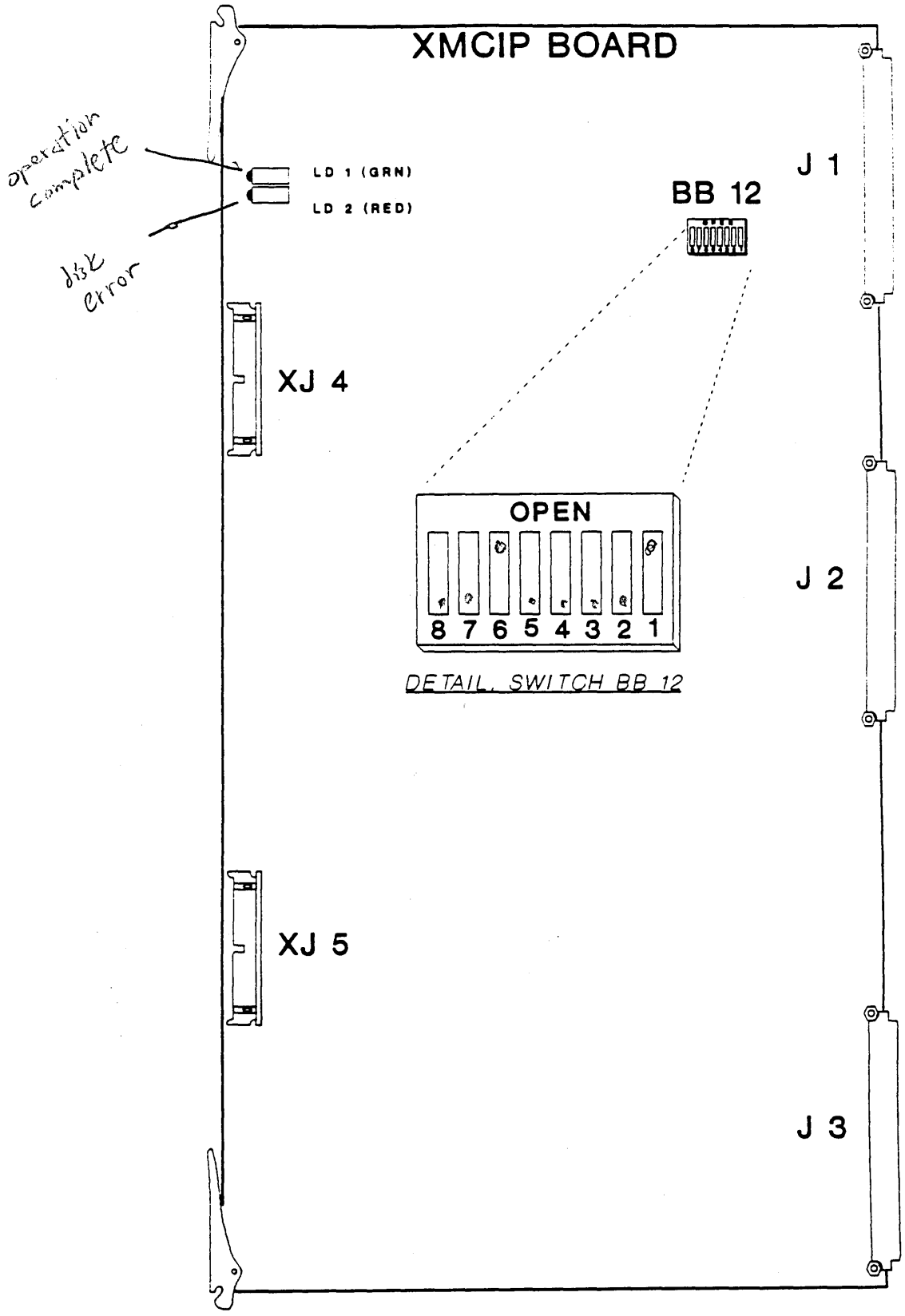


Figure 6-13
XMCIP - Layout of Test Points, Switches, and LEDs

XMCIP TEST POINTS, SWITCHES, LEDs

Test Points	Signal Name	Purpose
J4A-15	10DACK	Output data acknowledge tag for U-bus.
J5A-01	6CMCB00	CMC bus bits 00-07 + parity.
J5A-02	6CMCB01	
J5A-03	6CMCB02	
J5A-04	6CMCB03	
J5A-05	6CMCB04	
J5A-06	6CMCB05	
J5A-07	6CMCB06	
J5A-08	6CMCB07	
J5A-09	6CMCBP	
J5B-01	6CTB00	CT-bus bits 00-11 + parity.
J5B-02	6CTB01	
J5B-03	6CTB02	
J5B-04	6CTB03	
J5B-05	6CTB04	
J5B-06	6CTB05	
J5B-07	6CTB06	
J5B-08	6CTB07	
J5B-09	6CTB08	
J5B-10	6CTB09	
J5B-11	6CTB10	
J5B-12	6CTB11	
J5B-13	6CTBP	
JB5-17	6CLKIAA	

LEDs

LED-1 (GREEN)	AL62 AL62-01...6XMIFIB	When on, an operation has successfully completed.
LED-2 (RED)	AM62 AM62-01...6XMIFIA	When on, a disk error has occurred.

Switches

BB12-01	BC19-09...1SWXIF7	(BD ADR SW)	Switch 1 and 6 are always open.
BB12-02	BC18-10...1SWXIF6	(BD ADR SW)	Switches 2,3,4,5,7, and 8 are left closed.
BB12-03	BC17-11...1SWXIF5	(BD ADR SW)	
BB12-04	BC16-12...1SWXIF4	(BD ADR SW)	
BB12-05	BC15-13...1SWXIF3	(BD ADR SW)	
BB12-06	BC14-14...1SWXIF2	(BD ADR SW)	
BB12-07	BC13-15...1SWXIF1	(BD ADR SW)	
BB12-08	BC12-16...1SWXIF0	(BD ADR SW)	

Note: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.

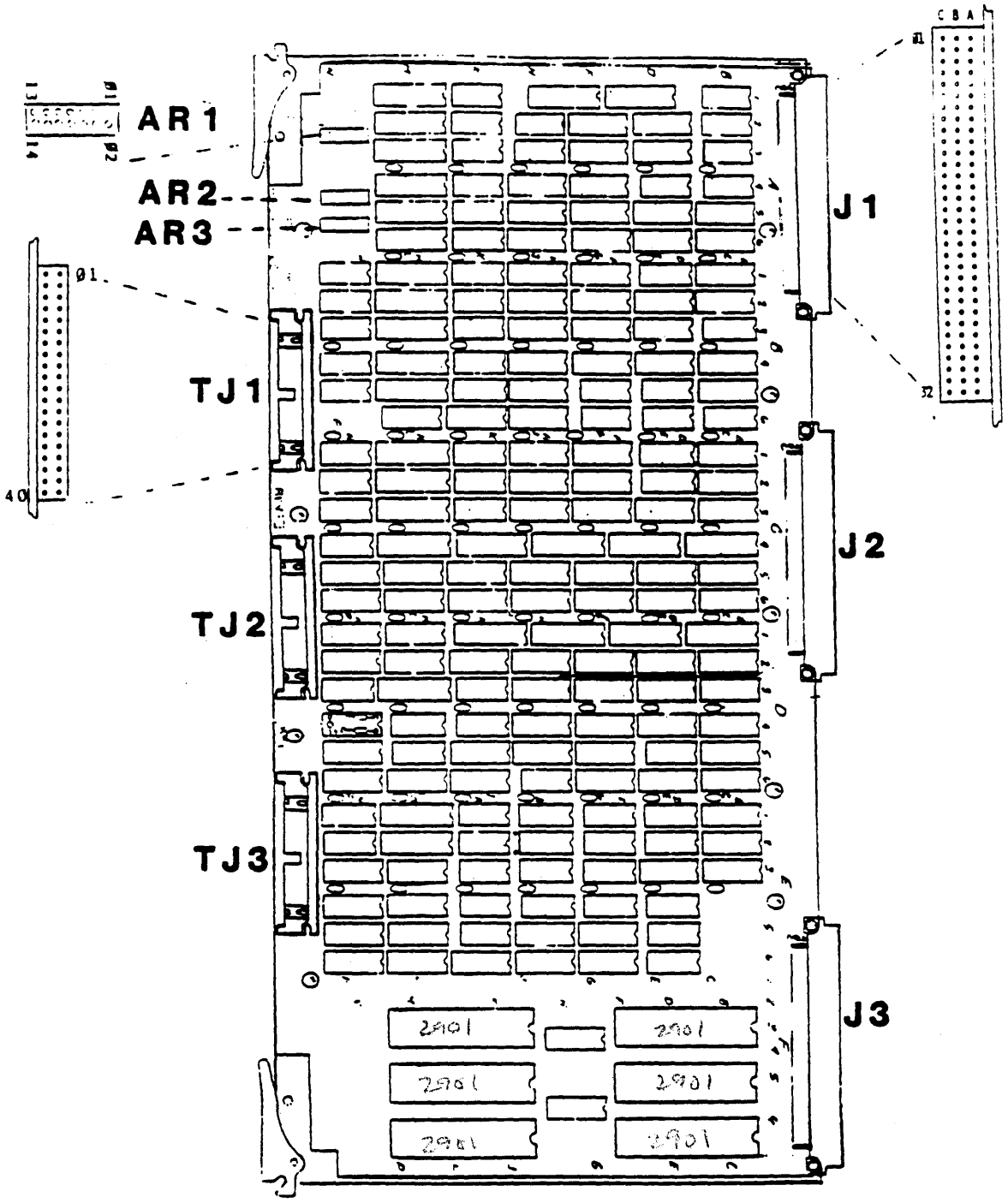


Figure 6-14
XMCP - Layout of Jumpers and Test Points

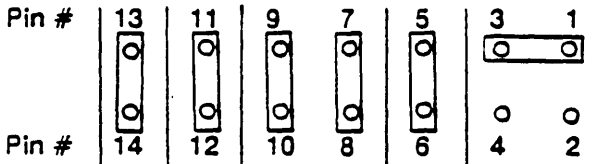
old bd - Jumpers instead of switches.

XMCP JUMPERS

AR1 Jumper	Signal Name
AR1-01	2URSPTOB
AR1-02	7SMDINER
AR1-03	6URSPTO
AR1-04	6URSPTOA
AR1-05	6SSS
AR1-06	GRD
AR1-07	6DISPL13
AR1-08	6DISPO13
AR1-09	6DISPL12
AR1-10	6DISPO12
AR1-11	2RAT
AR1-12	GRD
AR1-13	2CACHE
AR1-14	GRD

NOTE: *Solid state storage (SSS) and Data Save do not pertain to the 7001.*

Description



Pins 1 to 3 should always be jumpered. This allows XMCP to detect a response timeout condition. This condition occurs when the controller has ODR or IDR active and does not receive OA or IA from the channel within two milliseconds.

Jumper on for system with solid state storage.

Pins 7 to 8 and 9 to 10 should always be jumpered to allow display of bits 12 and 13 of the microprogram address at thumbwheel switch setting EXX.

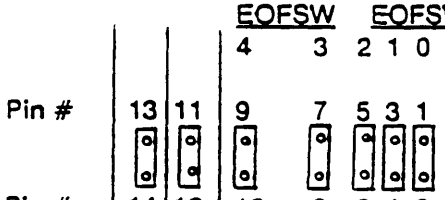
If jumper is on, it disables all caching and solid state storage microcode functions.

If jumper is on, it disables cache but does not disable solid state storage.

AR2 JUMPER

AR2-01...6EOFSWOO
AR2-02...GRD
AR2-03...6EOFSW01
AR2-04...GRD
AR2-05...6EOFSW02
AR2-06...GRD
AR2-07...6EOFSW03
AR2-08...GRD
AR2-09...6EOFSW04
AR2-10...GRD
AR2-11...6EOFSW05
AR2-12...GRD
AR2-13...7UCNTZ
AR2-14...7UXDTRDY

Description



1-32 solid state storage units

These pins are jumpered to indicate how many solid state storage (SSS) units are in the system. Jumper Off = 0, Jumper On = 1.

AR2
43210 EOFSW
00000 = 1 SSS unit
00001 = 2 SSS units
. .
. .
. .
11111 = 32 SSS units

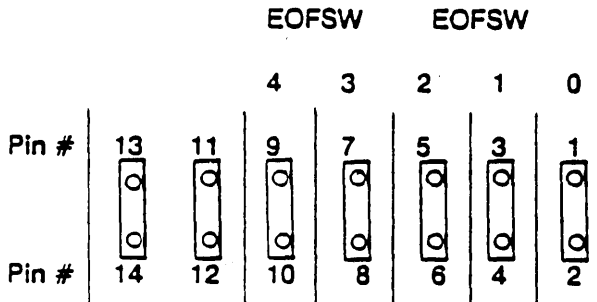
These pins are jumpered to indicate the starting device address of the first solid state storage (SSS) unit. Jumper Off = 0, Jumper On = 1. (All other units will increment.)

AR3 1/2	AR2 11/12	EOFSW 05	
0	0	1st SSS = unit 0	00 = first SSS is address 0
0	1	1st SSS = unit 8	01 = first SSS is address 8
1	0	1st SSS = unit 16	10 = first SSS is address 16
1	1	1st SSS = unit 24	11 = first SSS is address 24

Not used.

AR3 Jumper	Signal Name
AR3-01	6STSW00
AR3-02	GRD
AR3-03	6STSW01
AR3-04	GRD
AR3-05	6STSW02
AR3-06	GRD
AR3-07	6STSW03
AR3-08	GRD
AR3-09	6STSW04
AR3-10	6DCHAN
AR3-11	6STSW05
AR3-12	GRD
AR3-13	2SSDCMDL
AR3-14	8SMEERI

Description



MSB of SSS starting unit address.

Should not be jumpered. When jumpered it inhibits half rev. This disallows reading a disk track into cache until index has been reached. Used only as a factory debugging aid.

If jumpered this disables the Data Save feature. Should only be jumpered for systems without a Data Copy drive.

If jumpered Back Scan Seek is enabled. This should be jumpered for all systems with cache. Back Scan Seek updates cache tracks to disk during controller idle time.

If jumpered it indicates that the system has Dual Controllers.

Disables 2-for-1 drive configuration (2 drives = 1 logical unit) microcode.

XMCP TEST POINTS

Test Point TJ1	Signal Name	Purpose
TJ1-01	6CTB00	CT Bus bits 00-11 + parity.
TJ1-03	6CTB01	Refer to XMCP block diagram.
TJ1-05	6CTB02	
TJ1-07	6CTB03	
TJ1-09	6CTB04	
TJ1-11	6CTB05	
TJ1-13	6CTB06	
TJ1-15	6CTB07	
TJ1-17	6CTB08	
TJ1-19	6CTB09	
TJ1-21	6CTB10	
TJ1-23	6CTB11	
TJ1-25	6CTBP	
TJ1-27	N/A	
TJ1-29	N/A	
TJ1-31	7ODREQB	Output Data Request — U Bus Tags
TJ1-33	6ODACK	Output Data Acknowledge — U Bus Tags
TJ1-35	7SET1DRB	Set Input Data Request — U Bus Tags
TJ1-37	51DACKB	Input Data Acknowledge — U Bus Tags
TJ1-02	2SEQAR00	Sequencers address register bits
TJ1-04	2SEQAR01	00-13. This register outputs the
TJ1-06	2SEQAR02	current microprogram address.
TJ1-08	2SEQAR03	Refer to XMCP block diagram.
TJ1-10	2SEQAR04	
TJ1-12	2SEQAR05	
TJ1-14	2SEQAR06	
TJ1-16	2SEQAR07	
TJ1-18	2SEQAR08	
TJ1-20	2SEQAR09	
TJ1-22	2SEQAR10	
TJ1-24	2SEQAR11	
TJ1-26	2SEQAR12	
TJ1-28	2SEQAR13	
TJ1-30	N/A	
TJ1-32	2CLK1	
TJ1-34	6CLK1	
TJ1-36	2CLK2SYE	Clock to other system boards. Generated
TJ1-38	6CLK2SYE	from XMCP master clock circuitry.

Note: Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.

old 6d

Test Point TJ2	Signal Name	Purpose
TJ2-01	2SPAD00	Scratch pad memory Address Lines 00-09.
TJ2-03	2SPAD01	
TJ2-05	2SPAD02	
TJ2-07	2SPAD03	
TJ2-09	2SPAD04	
TJ2-11	2SPAD05	
TJ2-13	2SPAD06	
TJ2-15	2SPAD07	
TJ2-17	2SPAD08	
TJ2-19	2SPAD09	
TJ2-21	6RDSPAD	Scratch pad memory Read Enable.
TJ2-23	6SPWEN	Scratch pad memory Write Enable.
TJ2-25	N/A	
TJ2-27	2MINST16	Microinstruction bits 16-19 to next
TJ2-29	2MINST17	Address Control PROM. — function control prom
TJ2-31	2MINST18	
TJ2-33	2MINST19	
TJ2-35	N/A	
TJ2-37	N/A	
TJ2-02	2ALUY00	ALU Y Bus bits 00-11 + parity. This bus
TJ2-04	2ALUY01	is the output of the ALU. Refer to XMCP
TJ2-06	2ALUY02	block diagram.
TJ2-08	2ALUY03	
TJ2-10	2ALUY04	
TJ2-12	2ALUY05	
TJ2-14	2ALUY06	
TJ2-16	2ALUY07	
TJ2-18	2ALUY08	
TJ2-20	2ALUY09	
TJ2-22	2ALUY10	
TJ2-24	2ALUY11	
TJ2-26	2ALUYP	
TJ2-28	2UCZEROA	
TJ2-30	2CNDTST	Condition test bit to Next Address Control PROM.
TJ2-32	N/A	
TJ2-34	N/A	
TJ2-36	9CPRST	OCP reset signal to XMCP. Activated by button on maintenance panel. — reset button
TJ2-38	2ADRSYNC	Address sync signal to Event Count on OCP. Active for 200 nanoseconds when Break Point Address and Microprogram Address are the same.

Note: Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.
Signal names preceded by a 5, 6, 7, 8 or 9 are low (0V) when active.

old bd

Test Point TJ3	Signal Name	Purpose
TJ3-01	6ALUD00	ALU D Bus bits 00-11. This is the Direct Data Input lines to the ALU. This bus has multiple sources. Refer to XMCP block diagram.
TJ3-03	6ALUD01	
TJ3-05	6ALUD02	
TJ3-07	6ALUD03	
TJ3-09	6ALUD04	
TJ3-11	6ALUD05	
TJ3-13	6ALUD06	
TJ3-15	6AL7D07	
TJ3-17	6ALUD08	
TJ3-19	6ALUD09	
TJ3-21	6ALUD10	
TJ3-23	6ALUD11	
TJ3-25	N/A	
TJ3-27	N/A	
TJ3-29	N/A	
TJ3-31	2UPERL	U Bus parity error on lower bits (00-17) of the U bus.
TJ3-33	2UPERU	U Bus parity error on upper bits (18-36) of the U bus.
TJ3-35	2SPPER	Scratch pad parity error when reading out of Scratch Pad Memory.
TJ3-37	2CTSDPER	CT Bus parity error when XMC is receiving data on CT bus.
TJ3-28	3ENCLK1	To halt/run clocks from OCP. Remove jumper when running online.
TJ3-30	3ENCLK1A	
TJ3-36	5USYSCRR	To enable system clear signal from host CPU, jumper TJ3-36 and J3-38 together.
TJ3-38	5USYSCRB	

Note: Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.

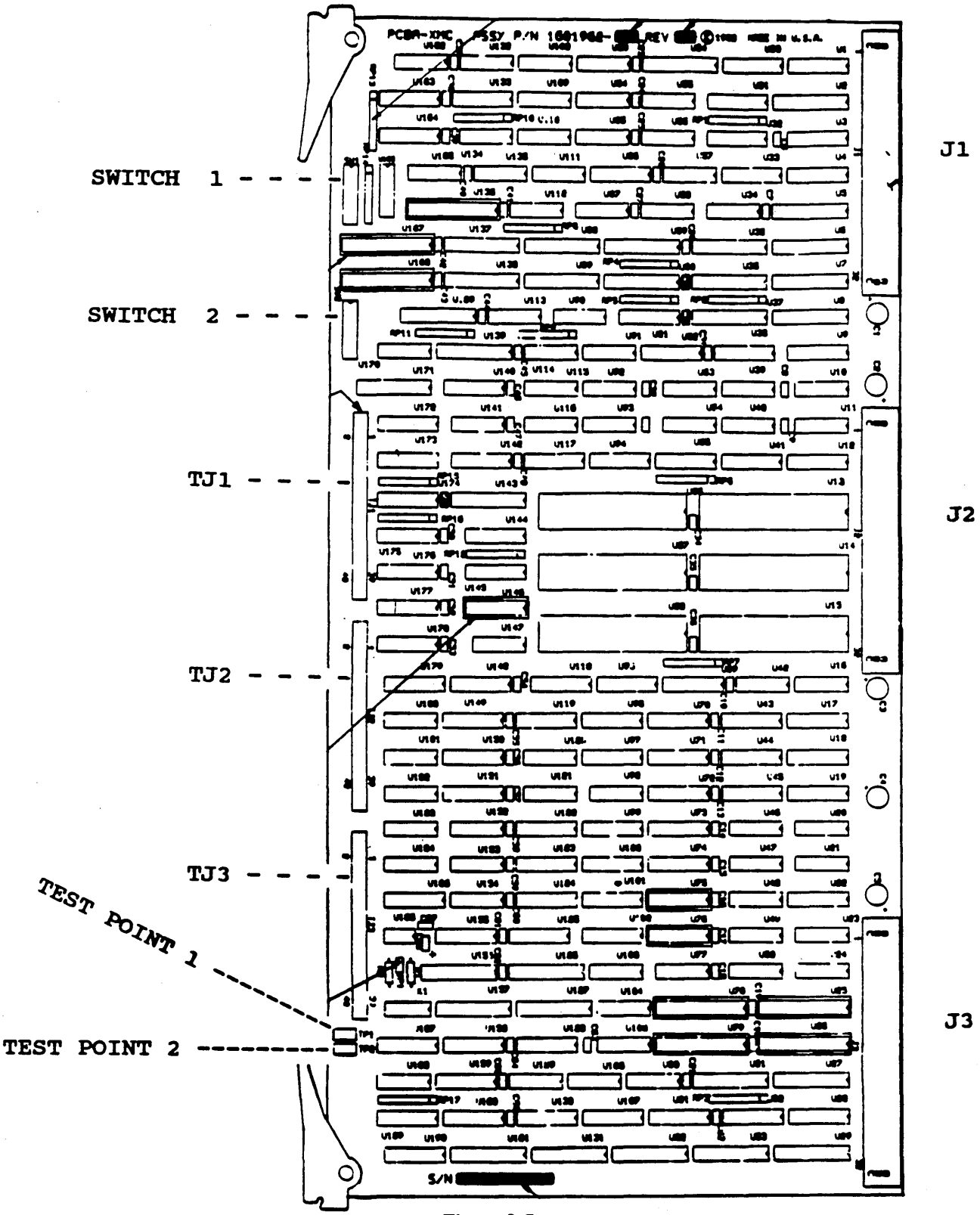


Figure 9-5
XMCP Layout of Switches and Test Connectors

XMCP SWITCH OPTIONS

SW1 - 1 and 2 SW1 switches 1 and 2 are set to indicate the starting address of the first Solid State Storage (SSS) unit.

switch open = 0
switch closed = 1

(All other units will increment.)

SW1 2	1		
0	0	1st SSS = unit 0	00 = first SSS is address 0
0	1	1st SSS = unit 8	00 = first SSS is address 8
1	0	1st SSS = unit 16	00 = first SSS is address 16
1	1	1st SSS = unit 24	00 = first SSS is address 24

SW1 - 3,4,5,6, and 7 There can be 1 to 32 solid state storage units in the system. SW1 switches 3,4,5,6, and 7 are set to indicate how many solid state storage units are in the system.

switch open = 0
switch closed = 1

SW1
76543
00000 = 1 SSS unit
00001 = 2 SSS units
. .
. .
11111 = 32 SSS units

SW1 - 8 At sites that operate in a multihost environment, closing SW1 switch 8 enables the multi-host file-sharing feature with microcode level 221AO and above. If SW1 switch 8 is open, multihost file-sharing is not operational.

SW2

switch 1 - If switch 1 is closed, it disables cache, but does not disable solid state storage.

switch 2 - If switch 2 is closed, backscan seek is enabled. Switch 2 should be closed for all systemswith cache. Backscan seek updates cache tracks to disk during controller idle time.

switch 3 - Switch 3 is closed for systems with solid state storage.

switch 4 - If switch 4 is closed, this disables the Data Save feature. Switch 4 should only be closed for systems without a Data Save drive.

switch 5 - If switch 5 is closed, all formatting is allowed (ILD 1 & 4.)

switch 6 - If switch 6 is closed, it indicates the system has dual controllers.

switch 7 - This switch has no effect in the 9200 system.

switch 8 - If switch 8 is closed, all caching and solid state storage microcode functions are disabled (always open).

XMCP TEST POINTS

Test Point TJ1	Signal Name	Purpose	
TJ1-01	6CTB00	CT-bus bits 00-11 + parity.	
TJ1-03	6CTB01	Refer to XMCP block diagram.	
TJ1-05	6CTB02		
TJ1-07	6CTB03		
TJ1-09	6CTB04		
TJ1-11	6CTB05		
TJ1-13	6CTB06		
TJ1-15	6CTB07		
TJ1-17	6CTB08		
TJ1-19	6CTB09		
TJ1-21	6CTB10		
TJ1-23	6CTB11		
TJ1-25	6CTBP		
TJ1-27	N/A		
TJ1-29	N/A		
TJ1-31	7ODREQB	Output Data Request	\
TJ1-33	6ODACK	Output Data Acknowledge	| U-bus
TJ1-35	7SET1DRB	Set Input Data Request	| Tags
TJ1-37	51DACKB	Input Data Acknowledge	/
TJ1-02	2SEQAR00	Sequencers address register bits	
TJ1-04	2SEQAR01	00-13. This register outputs the	
TJ1-06	2SEQAR02	current microprogram address.	
TJ1-08	2SEQAR03	Refer to XMCP block diagram.	
TJ1-10	2SEQAR04		
TJ1-12	2SEQAR05		
TJ1-14	2SEQAR06		
TJ1-16	2SEQAR07		
TJ1-18	2SEQAR08		
TJ1-20	2SEQAR09		
TJ1-22	2SEQAR10		
TJ1-24	2SEQAR11		
TJ1-26	2SEQAR12		
TJ1-28	2SEQAR13		
TJ1-30	N/A		
TJ1-32	2CLK1		
TJ1-34	6CLK1		
TJ1-36	2CLK2SYE	Clock to other system boards. Generated	
TJ1-38	6CLK2SYE	from XMCP master clock circuitry.	

NOTE: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.

Test Point TJ2	Signal Name	Purpose
TJ2-01	2SPAD00	Scratch pad memory Address Lines 00-09.
TJ2-03	2SPAD01	
TJ2-05	2SPAD02	
TJ2-07	2SPAD03	
TJ2-09	2SPAD04	
TJ2-11	2SPAD05	
TJ2-13	2SPAD06	
TJ2-15	2SPAD07	
TJ2-17	2SPAD08	
TJ2-19	2SPAD09	
TJ2-21	6RDSPAD	Scratch pad memory Read Enable.
TJ2-23	6SPWEN	Scratch pad memory Write Enable.
TJ2-25	2SPAD10	
TJ2-27	2SPAD11	
TJ2-29	N/A	
TJ2-31	N/A	
TJ2-33	N/A	
TJ2-35	N/A	
TJ2-37	N/A	
TJ2-02	2ALUY00	ALU Y-bus bits 00-11 + parity. This bus
TJ2-04	2ALUY01	is the output of the ALU. Refer to XMCP
TJ2-06	2ALUY02	block diagram.
TJ2-08	2ALUY03	
TJ2-10	2ALUY04	
TJ2-12	2ALUY05	
TJ2-14	2ALUY06	
TJ2-16	2ALUY07	
TJ2-18	2ALUY08	
TJ2-20	2ALUY09	
TJ2-22	2ALUY10	
TJ2-24	2ALUY11	
TJ2-26	2ALUYP	
TJ2-28	2UCZEROA	
TJ2-30	2CNDTST	Condition test bit to Next Address Control PROM.
TJ2-32	N/A	
TJ2-34	N/A	
TJ2-36	9CPRST	OCP reset signal to XMCP. Activated by button on maintenance panel.
TJ2-38	2ADRSYNC	Address sync signal to Event Count on OCP. Active for 200 nanoseconds when Break Point Address and Microprogram Address are the same.

NOTE: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8 or 9 are low (0V) when active.

Test Point TJ3	Signal Name	Purpose
TJ3-01	6ALUD00	ALU D-bus bits 00-11. This is the Direct Data Input lines to the ALU. This bus has multiple sources. Refer to XMCP block diagram.
TJ3-03	6ALUD01	
TJ3-05	6ALUD02	
TJ3-07	6ALUD03	
TJ3-09	6ALUD04	
TJ3-11	6ALUD05	
TJ3-13	6ALUD06	
TJ3-15	6AL7D07	
TJ3-17	6ALUD08	
TJ3-19	6ALUD09	
TJ3-21	6ALUD10	
TJ3-23	6ALUD11	
TJ3-25	N/A	
TJ3-27	N/A	
TJ3-29	N/A	
TJ3-31	2UPERL	U-bus parity error on lower bits (00-17) of the U-bus.
TJ3-33	2UPERU	U-bus parity error on upper bits (18-36) of the U-bus.
TJ3-35	2SPPER	Scratch pad parity error when reading out of Scratch Pad Memory.
TJ3-37	2CTSDPER	CT-bus parity error when XMC is receiving data on CT-bus.
TJ3-28	3ENCLK1	To halt/run clocks from OCP. Remove jumper when running online.
TJ3-30	3ENCLK1A	
TJ3-36	5USYSCRR	To enable system clear signal from host CPU, jumperTJ3-36 and J3-38 together.
TJ3-38	5USYSCRB	

NOTE: *Signal names preceded by a 1, 2, 3, or 4 are high (+5V) when active.*
Signal names preceded by a 5, 6, 7, 8, or 9 are low (0V) when active.

SECTION 4 EXPANDED MEMORY 16K PLUGIN (XM16KP)

4.1 DESCRIPTION

Numbering Conventions
In the following text, decimal, hexadecimal, and binary numbers are used. Unless otherwise noted, all numbers without a suffix are decimal. Numbers with the "H" suffix are hexadecimal. Binary numbers are identified each time they are used.

The XM16KP board's main functions are to provide the downloadable microprogram memory, code error detection, and microsubroutine nesting (stack) functions for the XMCP processor board. The board is made up of two separate parts which are normally connected: the main board (XM16KP), and the small removable daughter board (XM16KP-D) which inserts into a cut out in the main board and mates with it via a 48-pin DIN type connector (see Figure 4.1).

4.1.1 Main Board (XM16KP)

The main board contains the microprogram memory, microinstruction pipeline register, stack, daughter board EPROM interface, parity control, address and data multiplexers, power up circuit, control switches, status lights, and all sequential and combinatorial "glue" circuitry necessary to perform its functions.

The hardware of the XM16KP consists of the following parts:

1. SRAM microcode memory (16K x 4 bits, 22-pin 300 mil package, 45 ns access time: U117-U122, U140-U145)
2. SRAM address counter and decode logic (U22-U25, U47-U49)
3. XMCP address receivers (U32, U56)
4. Microinstruction pipeline register (U91-U95)
5. Microinstruction transmitters (U27-U31)
6. NOP transmitters (U51-U55)
7. Parity checking logic (U112-U116; U137)
8. Daughter board interface:
   - EPROM address counter and decode logic (U79-U83, U109)
   - EPROM data assembly circuitry (U70-75, U84, U110, U111)
   - 48-pin, 3-row, male DIN connector (J4)
9. Address stack logic (U2-U9, U26, U34-U41, U50)
10. Timing circuits (U10, U11, U42, U43)
11. Power up circuit (D1, R1, C150, U146, U147)
12. Sequential control (U19-U21, U44-U46)
13. Combinatorial control (U12-U18)
14. Manual controls (SW1-SW3) and debouncing circuits (U9,U148)
15. LEDs (DS6-DS9)
16. 96-pin, 3-row, female DIN backplane connectors (J1-J3)
17. Terminators (resistor networks)

Operation

The microprogram memory has a tri-state bidirectional 45-bit wide data bus and a 14-bit wide tri-state address bus. It is built from twelve 16K x 4 SRAM chips, with the three most

significant data bits of the highest order chip not used. The address comes either from the XMCP (online operation) or from the SRAM address counter (offline operation: load and dry run). The address source is selected by the control circuitry and depends on the board's mode of operation. Since the SRAM chips have a common I/O pin, all read and write operations are always performed on 45-bit words.

The data to be written into SRAM is supplied by the EPROM data assembly register U70-U75 (load operation). The function of this register is to assemble the 8-bit (EPROMs) into a 45-bit word suitable for SRAM. All parity bits are contained in the sixth consecutive byte of a microcode word.

During load, every 400 ns the EPROM address counter generates a 17-bit sequential address used to read a byte from one of two daughter board EPROMs. At the end of a 400 ns cycle, that byte is latched in the proper section of the assembly register (U70-U75). This is done by one of six signals (5PRWTEN0-5) derived from decoding a modulo-6 counter synchronized with the EPROM address counter. Every time the sixth consecutive byte of microcode data is latched, a 400 ns SRAM write cycle is initiated. The assembly register's output is enabled onto the SRAM data bus and a parity check is done. If errors are detected, the write strobe and the chip select signals are suppressed and the write does not take place.

To do parity checking, the data to be written into SRAM is first latched in the pipeline register (U91-U95) and then passed from there to the input of parity logic.

SRAM Read Cycles

The SRAM read cycles occur during online operation or dry run (SRAM parity scanning operation). During online operation, read cycles last 200 ns; 45 bits of microcode and parity data are read from the address received from the XMCP (via the backplane), and at the end of each cycle (i.e. on rising edge of 6CLK1 clock) they are latched into the pipeline register (U91-U95). Then, approximately 50 ns into the next processor cycle, the parity check results for that data are latched and examined. If no errors are found, the 40 microinstruction bits are allowed to pass to the XMCP through transmitters U27-U31. If errors are detected, these transmitters are immediately disabled (less than 100 ns into the cycle), and the "NOP" transmitters are turned on; the E008FE0000H (SYS RST & JMP 0) microinstruction is executed by the XMCP in each cycle for as long as the board is in this offline mode. It will continue until the error condition is cleared by reset (see Figure 4.6 for all different ways of resetting the circuitry).

During dry run (executed in the offline mode to scan the SRAM for parity errors), the read cycles last 400 ns with the SRAM address counter supplying the address. The data is latched in the pipeline register after 200 ns, and then is checked for parity at its output. 250 ns into the cycle the parity check results are latched: if they are bad, error LEDs are activated and the circuitry locks up (SRAM address counter preserves its value).

All control signal sequences are generated by D-type flip-flop chains interconnected through 20L8-type PALs. The sequences are triggered by various combinations of properly synchronized power up and manual switch signals. Depending on the position of the two "mode" toggle switches SW2 and SW3, the appearance of power, or activation of the reset pushbutton SW1 causes certain sequence(s) to occur (see Figure 4.6).

The stack is built using 16-deep register files and a synchronous counter serving as stack pointer. All signals controlling that circuit come from a 32 x 8 control PROM (U41), whose low order address line is driven by the 2CTEST signal from the XMCP (result of the

condition test), and four upper address lines are microinstruction bits 16 through 19.
During each processor cycle, the current microprogram address is latched and incremented to produce the proper linkage address. If directed by the five control signals mentioned above, it can then be stored in the register files at the location indicated by the counter (which in such a case is first incremented). This constitutes a PUSH operation.
A POP operation occurs when the linkage address stored at the last location written in the register file (always indicated by the counter) is read and sent back to the XMCP, and the stackpointer is decremented.

A READ operation is similar to a POP operation, except that the pointer is not decremented following a READ.

The stack RESET operation, last of the basic stack functions, consists in resetting the stack pointer to zero, thereby invalidating all linkage data in the register files.

Various combinations of these four basic stack operations are used in the XMCP microinstruction set.

4.1.2 Daughter Board (XM16KP-D)

The daughter board contains two EPROMs (which store the entire microcode for the XMCP processor) and logic to interface with the main board. The microcode is permanently stored and transported in the daughter board's EPROMs, and is downloaded to the main board's volatile SRAM-based memory either automatically upon power up, or manually at any time prior to starting the XMCP operation.

The hardware of the XM16KP-D consists of the following parts:

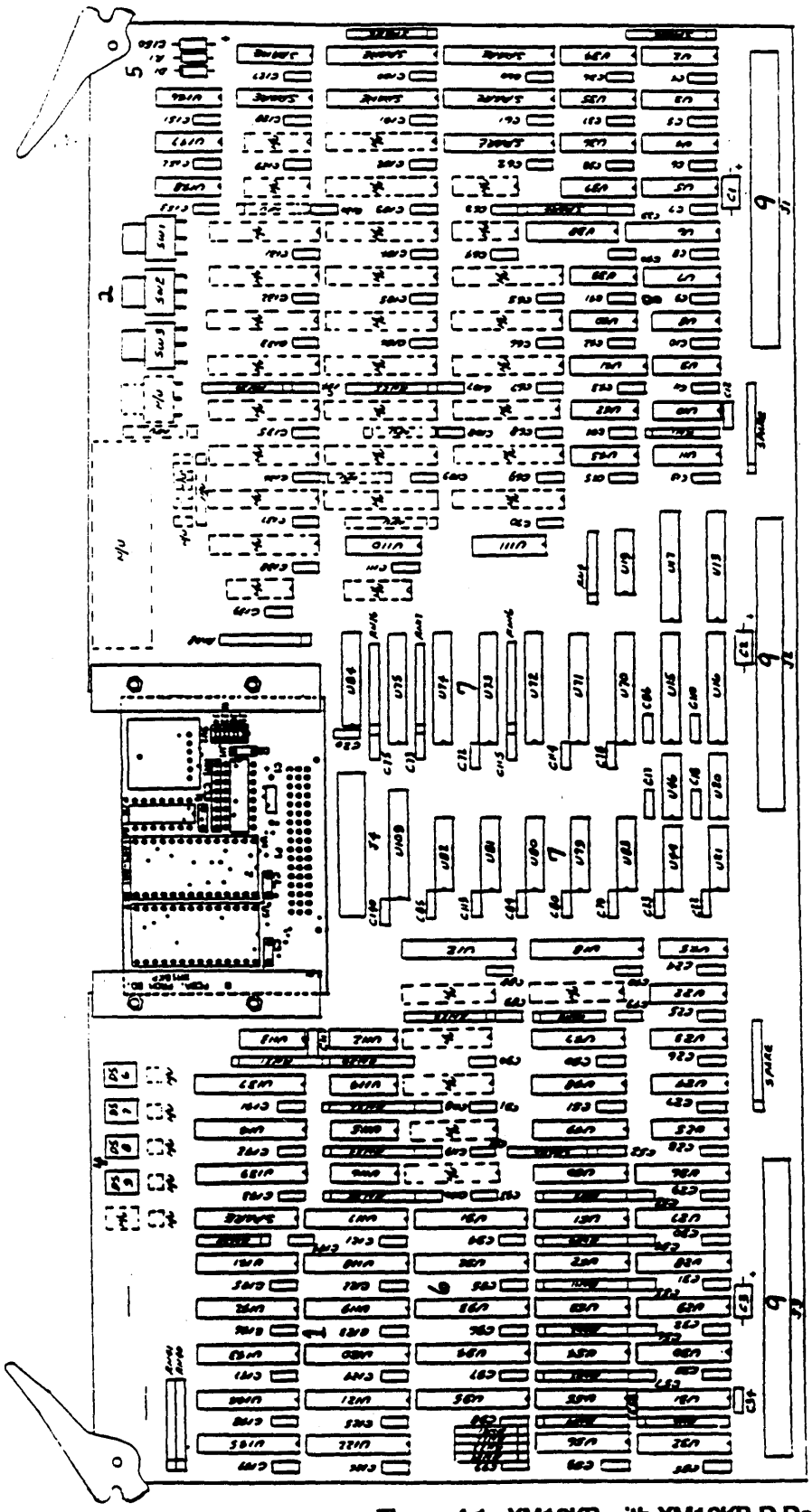
1. Two 64K x 8 EPROMs (AM27512, 28-pin 600 mil package, 250ns access time: EPROM #1 - U3, EPROM #2 - U4)
2. Chip select logic (U2)
3. Address offset logic (U1)
4. Terminators (resistor networks)

Operation

The only function of the daughter board is to decode the 17-bit address provided by the counters on the XM16KP board to access one of 128K bytes and send it back to the main board. This address always starts from 00000H and goes up to 17FFFH. It is decoded directly.

The chip select and output enable signals of both EPROMs are arranged to facilitate in-circuit programming on the DATA I/O Model 29B programmer, using an adapter developed for that purpose.

The control switches and status lights are used by the operator to direct the XM16KP to load the microcode, check its parity, reset the errors, and take the board on or offline. Loading and checking of the code can be performed only in the offline mode, while the XMCP processor constantly executes a "do nothing" command. When ready, the board can be placed in its normal operating (i.e. online) mode. In this mode, it receives an address from the XMCP during each processor cycle and responds by sending back an appropriate microinstruction. If a stack operation was performed in a given cycle, its result, if any, will also be sent to the XMCP.



XM16KP Component Layout

1 - Microprogram memory (SRAM)
2 - Manual control switches
3 - Daughter Board (XM16KP-D)
4 - Status LEDs
5 - Power up circuitry
6 - Pipeline register
7 - Control logic
8 - Stack logic
9 - Backplane connector

Figure 4.1 XM16KP with XM16KP-D Daughter Board

4.2 BLOCK DIAGRAM DESCRIPTION

Figure 4.2 shows the basic functional block diagram of the XM16KP and XM16KP-D boards (jointly referred to hereafter as XM16KP(-D)).

The heart of the device is the SRAM microprogram memory, organized as 16K (16,384) of 45-bit wide microcode words. The words are comprised of 6 bytes; 1MEMTD 00-39 (grouped as bytes 0 through 4) are the actual microinstruction bits controlling the XMCP circuitry, and 1MEMPA 00-04 (as byte 5) are the parity bits for the respective microinstruction bytes. The three most significant bits of byte 5 are not used.

Parity bits are loaded and stored in the SRAM together with the microinstruction bits, and checked every time a microinstruction is read back from the SRAM. Odd parity scheme is used throughout the design, i.e. the binary value of the parity bit is such that a total number of "1"s in all nine bits of information (eight bits of data plus one parity bit) is odd.

Address Sources

The address on the 14-bit wide tri-state memory address bus (1SRAD00 through 13) is supplied from one of two sources: XMCP (coming via the backplane) or an on-board counter. The 45-bit wide tri-state bidirectional memory data bus (1MEMDT00-39, 1MEMPA00-04) is used both to write data into and read it from the SRAM. During write cycles the data comes from the daughter board EPROMs. During read cycles the data goes to the microinstruction pipeline register. Parity is checked during both reads and writes, and the control logic is notified if an error is detected.

The inputs of the parity checking logic (2MEMDT00-39, 2MEMPA00-04) are driven either by the pipeline register outputs or, through a buffer, by the memory data bus. Normally (i.e. in online mode), at the end of each cycle, the data read from the SRAM is latched in the pipeline register. From there it is passed through a buffer on to the XMCP (via the backplane) as microinstruction. However, in the offline mode, the tri-state output of that buffer (2SEQMB00-39) is disabled, and a special "do nothing" ("NOP") microinstruction is forced upon the XMCP by an alternate set of drivers.

The address stack is 16 locations deep, which allows for nesting the same number of levels of microsubroutines. Its operation is controlled by five signals: four microinstruction bits (2SEQMB16-19), and a 2CTEST signal from the XMCP carrying the"true" or "false" result of the condition test (if one was performed in the current processor cycle).

During each processor cycle the address of the current microinstruction is incremented and latched, and only if so directed by those controlling bits - can then be stored in a 16-deep LIFO-type memory. In the subsequent processor cycles, that value can either be read off the top of the LIFO, or "popped" - i.e. read and deleted from it.

The synchronization and clocking for the XM16KP's operations are provided by two XMCP processor clock signals, 6CLK1 and 6CLK2. These are supplied via the backplane and used both directly and for generation of all slower clocks. All synchronous events on the board, including the memory cycles, are "in sync" with the processor clock 6CLK1, except parity error latching which is synchronized to 6CLK2. Both 6CLK1 and 6CLK2 clocks have a 200 nanosecond cycle.

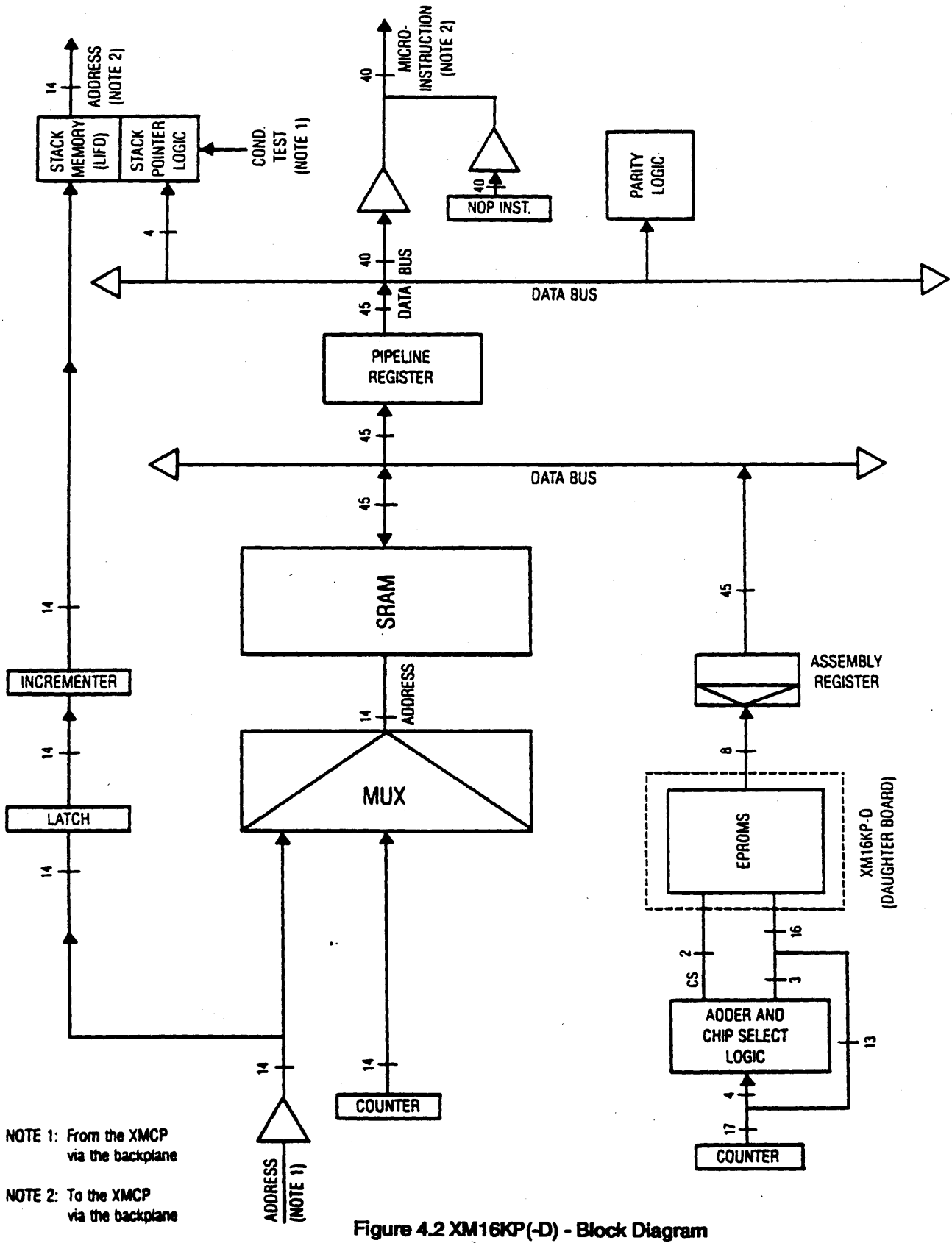


Figure 4.2 XM16KP(-D) - Block Diagram

4.3 OPERATING MODES

4.3.1 Functions and Controls

This section describes the operating modes and functions of the XM16KP(-D), and how to control them. Figures 4.3, 4.4, and 4.5 illustrate each operating mode by highlighting the applicable flow paths on the XM16KP(-D)'s block diagram.

The settings of two toggle switches select the operating mode of the board, which in turn determines what function or functions can be performed and in what sequence. The actual initiation of function(s) occurs either automatically upon power-up or by manually activating the RESET pushbutton switch (SW1). The "mode select" toggle switches are as follows:

ON/OFF LINE (SW2)
EPROM ENABLE/DISABLE (SW3)

The purpose and effect of each of these control switches is described below.

ON/OFF LINE Switch (SW2, Toggle)

This is the main control on the board. When ON, all other controls are defeated and the XM16KP(-D) is in a completely automatic, ONLINE mode of operation.

When the board is powered up in this mode (i.e. with the switch ON), a "kick-off" signal from the power up circuit initiates the process of loading the microcode from the daughter board EPROMs into the main board's SRAM memory. Six bytes at a time are pulled from the EPROMs and assembled into a full 45-bit microcode word (including 5 parity bits). This word is then checked for proper parity . If no errors are found, it is loaded into the consecutive SRAM location. This process, referred to as LOAD sequence, continues until 96K bytes are transferred from the EPROMs to fill the entire 16K-word capacity of the SRAM. This takes a little over 39 ms to complete.

The successful end of the load sequence immediately triggers another sequence, referred to as DRY RUN. During the DRY RUN, consecutive SRAM locations (0 through 3FFF) are read and each 45-bit wide microcode word is latched into the pipeline register (as in normal operation). Parity is then verified to double check the integrity of the microcode, as well as the proper functioning of the pipeline register. Since the latter is not used in the load process, its failure would otherwise not be detected. The DRY RUN takes less than 7 ms. It is important to note that during the load and dry run sequences the XM16KP(-D) is kept in the OFFLINE mode by its control circuitry. This means that the "NOP" microinstruction is being forced upon the XMCP, thereby holding it at address zero.

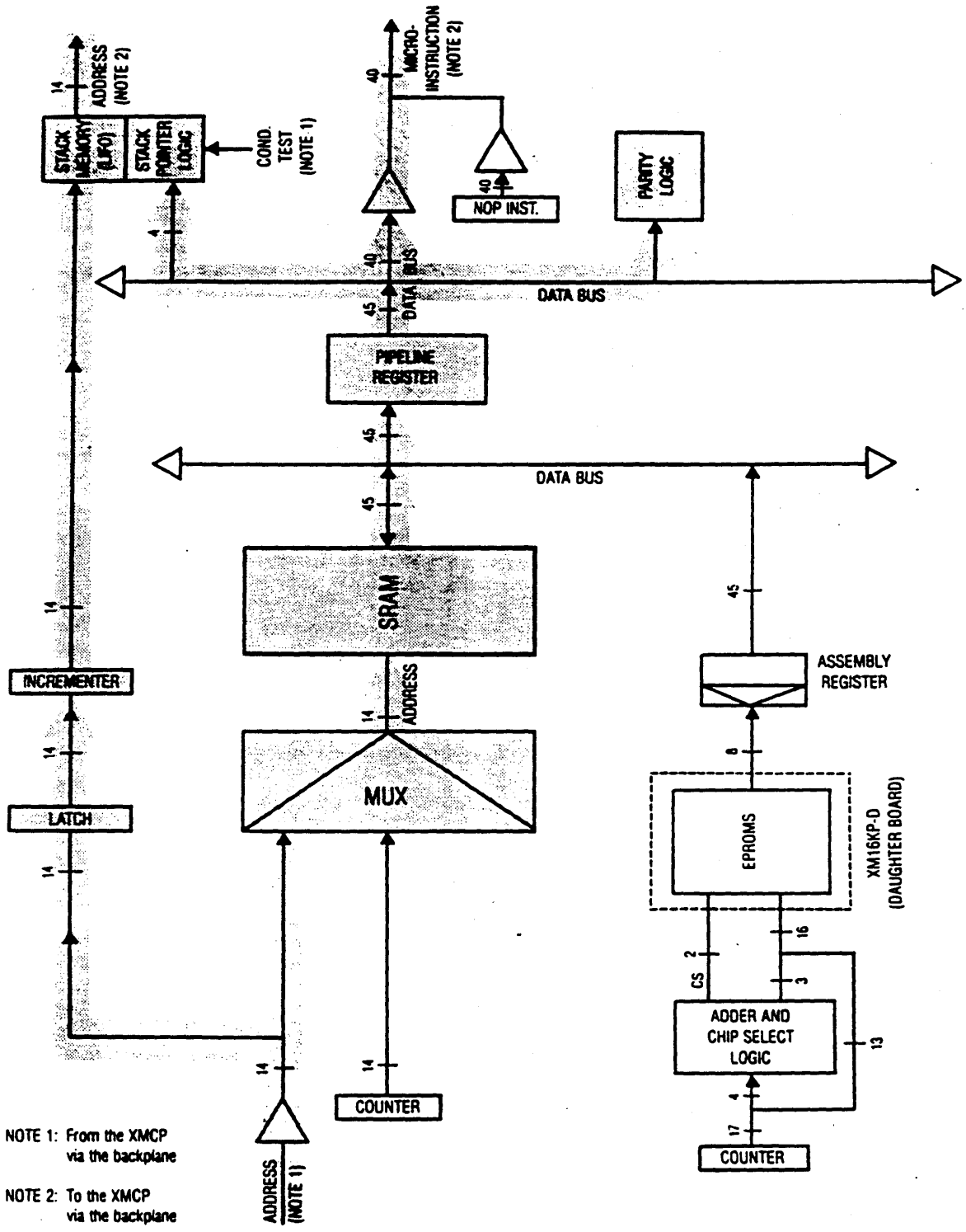


Figure 4.3 Online Mode of Operation

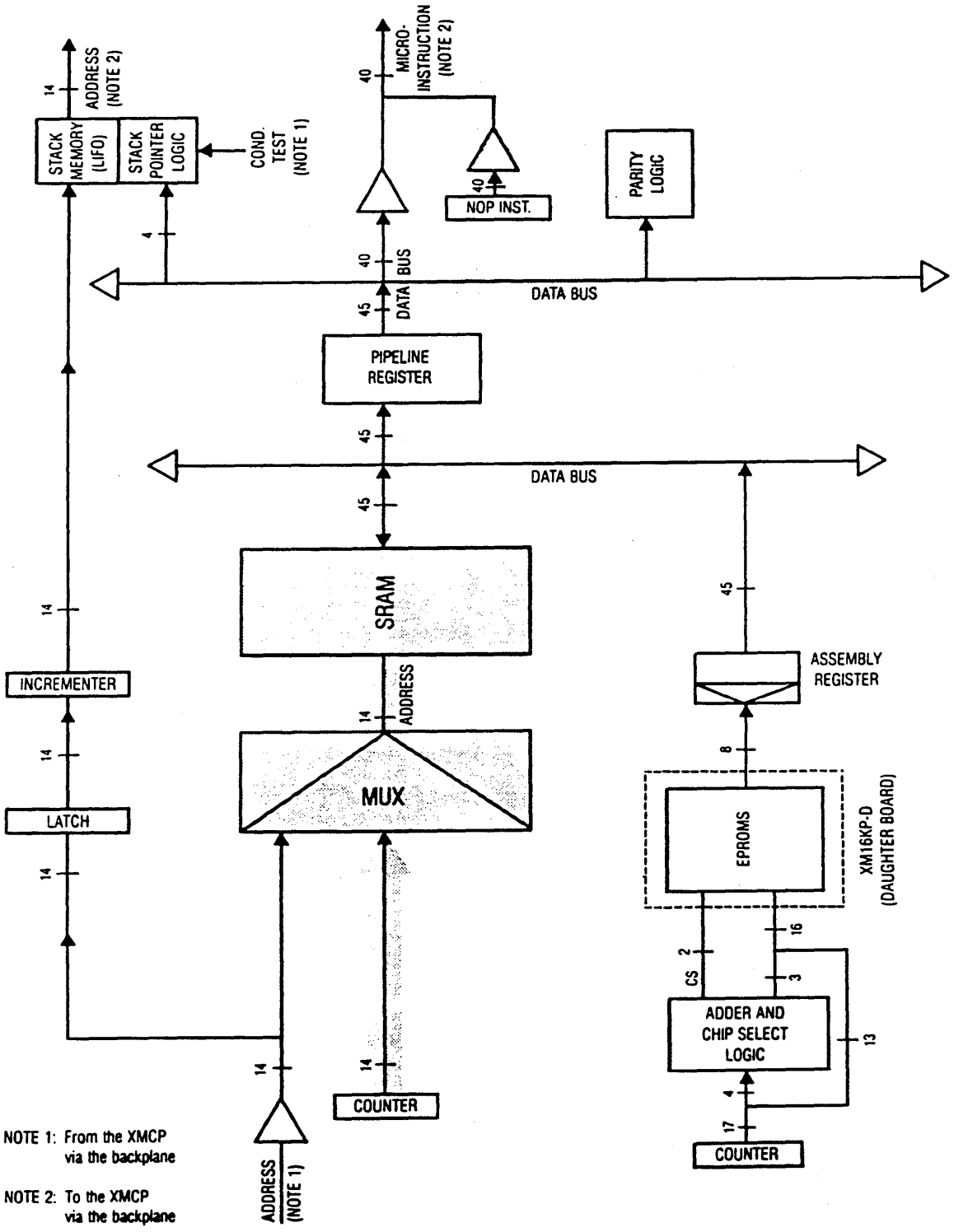


Figure 4.4 Dry Run Mode of Operation

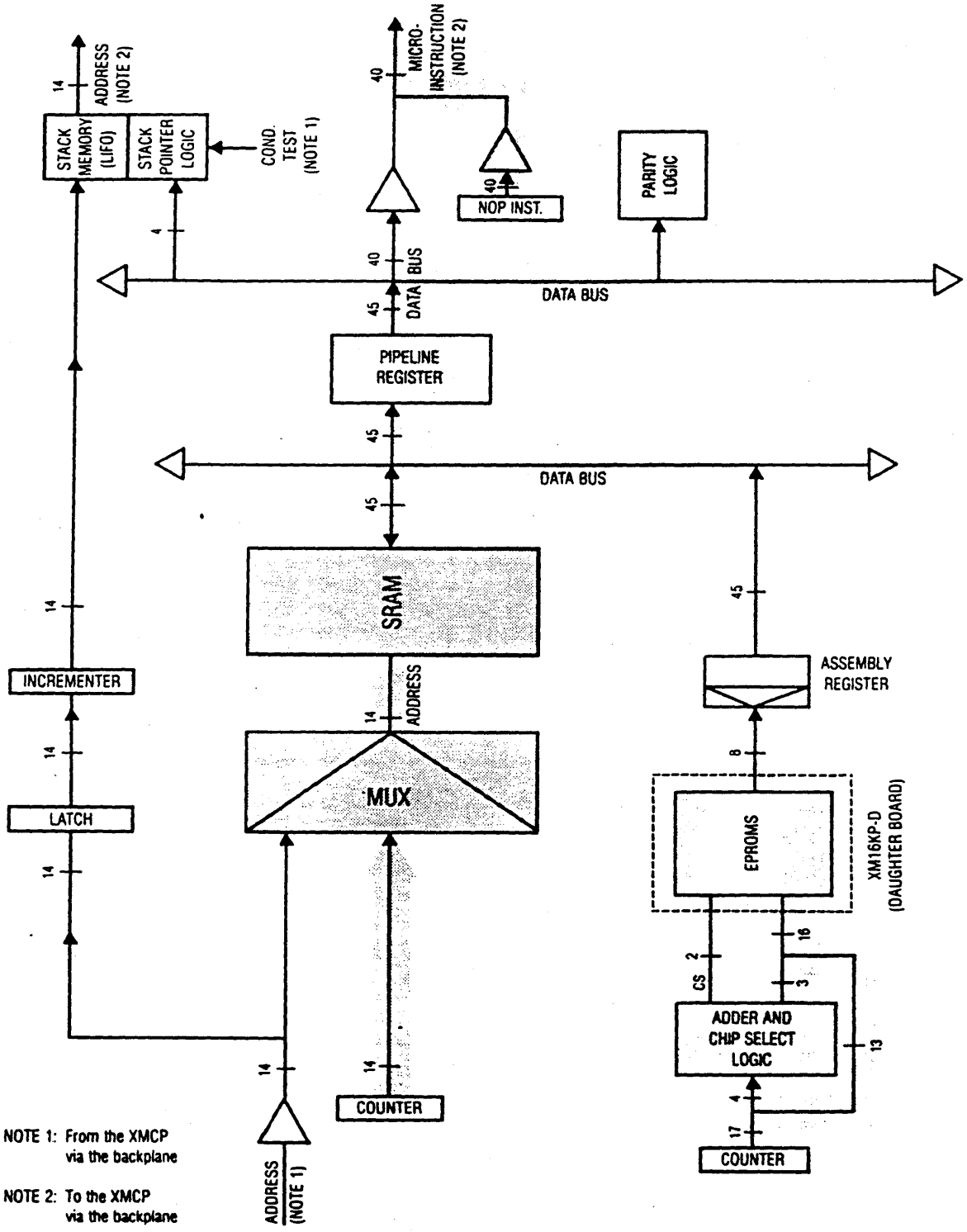


Figure 4.5 EPROM Load Mode of Operation

Immediately following a successful completion of the dry run, the board is automatically switched into the ONLINE mode. This means that the path is opened for the incoming XMCP address to the SRAM. Also, the buffers enabling the pipeline register output onto the XMCP microinstruction bus are turned on, while the "NOP" buffers become disabled. The green ON-LED (DS6) goes on, indicating that XMCP has already begun executing the microcode. This completes the automatic "bootstrap" sequence which occurs upon power up if the ON/OFF switch is ON. If it is OFF, what happens during power up depends on the position of the other toggle switches.

After the power up phase, the only function of this switch is to select between the two basic modes of operation: on and off. The off mode must be entered in order to load/check the microcode or access the SRAM from the external interface. The mode changes are synchronized with the system clocks to ensure smooth transition and prevent the XMCP from executing indeterminate operations. The "NOP" microinstruction, always forced upon the XMCP when the XM16KP(-D) is off, consists of two parts: SYS RST & JMP 0000; the "ALU" portion tells the CPU to send a reset signal to all boards in the system, while the "next address portion" holds the output of the XMCP address sequencer at zero for as long as the NOP is applied. This ensures that the XMCP will begin executing from address 0000 once the board is put on.

The power up sequence described above may be affected by an occurrence of a parity error either during the loading or the dry run. Refer to section 4.3.2 for details.

EPROM ENABLE/DISABLE Switch (SW3, Toggle)

Like all other manual controls on the XM16KP(-D) board, this switch is active only if the ON/OFF switch is in the OFF position. Its function is to enable the EPROM interface logic (which controls loading of the microcode from the daughter board EPROMs) into the SRAM on the main board. The yellow EPROM ENBLD LED (DS9) indicates the enabled state of that logic. When it is on, the load can be initiated either automatically upon power up or by manually activating the RESET pushbutton. In both cases, as always, the load is immediately followed by a dry run. This is intended as an additional check of the code's integrity, as well as conclusive proof of proper operation of the pipe register before the board is switched to the on mode. To provide positive visual feedback that the load and dry run operations have occurred and been completed, the DS9 LED blinks for their duration. Unlike the on power up sequence described in section 4.3.1, after the dry run is completed the board stays in the off mode (as long as SW2 is OFF).

RESET Switch (SW1, Pushbutton)

This switch initiates one of several events or sequences, depending upon the mode determined by the settings of SW2 and SW3 mode select switches. The effect of SW1 is tabulated in Figure 4.6, which also shows what happens during a power up in all different modes.

4.3.2 Error Detection

Parity of the microcode is always monitored during all operations performed by the XM16KP(-D) board. This minimizes the probability of fatal system level errors caused by erratic or indeterminate XMCP operation. Parity is checked during code loading, dry run, and on operation. The parity errors detected by the board's logic fall into two categories:

Load errors:
These occur during loading of the microcode into SRAM and are caused by an attempt to load data containing incorrect parity. Each time a 45-bit microcode word (assembled from data bytes from the daughter board's EPROMs) is about to be written into the SRAM, its parity is checked. If it is incorrect, the write operation is inhibited and the loading mechanism is immediately halted. Red LOAD ERROR LED (DS7) lights up to indicate this condition. The control logic locks up and will remain in this state until reset (see Figure 4.6 for all possible resets). The board, off during load, cannot be put on until the error condition is cleared.

SRAM errors:
These occur during read operation from the SRAM. This type of error, indicated by red SRAM ERROR LED (DS8), can occur either during dry run or on operation. In either case, it indicates that the data in the SRAM is invalid for one of two reasons:

- o the SRAM is in its post-power up state and has never been initialized with good data, or
- o the microcode stored in the SRAM (which must have been good at the time of the load, since otherwise it would not have been possible to load it) is corrupted due to soft or hard memory or circuitry errors.

Once this type of error is detected during normal on operation, the board is immediately switched to off mode (i.e. a "NOP" is forced upon the XMCP microinstruction bus). This switchover is not necessary if the SRAM error occurs during dry run because in that case the board is already in the off mode. In either case, the logic locks up (as it does for load errors) and remains in this state until reset (see Figure 4.6 for all possible resets).

It is important to note that:

1) the parity errors detected during SRAM write cycles inhibit the actual write operation (see item 1 above), and

2) every time the load operation completes, the entire contents of the SRAM (16K of 45-bit words) has been filled with data (see section 4.3.1). This implies that following the first successfully completed load operation after the power up, the memory should never contain data with bad parity. If it does (which can be detected by dry run or during on operation), it most likely signals a hardware failure, because the "soft" error rate of the SRAM memory chips used in the design is extremely low.

Mode Switch Settings		Effect of the RESET Pushbutton	Effect of the Power Up
ONLINE SW2	EPROM EN SW3		
ON	X	None Note: The board remains on with all controls defeated as long as SW2 is ON	1. Reset logic, set off mode 2. LOAD EPROMs into SRAM 3. Dry run SRAM 4. Switch over to on mode
OFF	OFF	1. Reset logic 2. Dry run SRAM and stay off	1. Reset logic and and stay off
OFF	ON	1. Reset logic 2. Load EPROMS into SRAM 3. Dry run SRAM and stay off	1. Reset logic 2. Load EPROMS into SRAM 3. Dry run SRAM and stay off

Figure 4.6 RESET Switch Functions and Power Up Booting

4.3.3 Daughter Board

The daughter board contains two 27512-type EPROMs, each containing 64K bytes of data. The address space assignment is as follows: EPROM #1 - from 0000H to FFFFH, EPROM #2 - from 10000H to 1FFFFH. Since the capacity of the main board's SRAM is 16K words and each word consists of 6 bytes, 96K out of 128K bytes in the EPROMs are transferred every time a load is performed.

The starting and ending EPROM load addresses are fixed, and equal to OOOH (EPROM #1) and 17FFFH (EPROM #2), respectively. The 18OOOH through 1FFFFH portion of the second EPROM is never used.

It should be pointed out that every time a load occurs, the entire SRAM is filled with data from the EPROMs (96K bytes), regardless of the actual size of the object code. The "unused" portions of the EPROMs must therefore be filled with any parity-correct data, e.g. their unprogrammed, or erased, state (all bits high - FFH). In cases when the microcode fits into only one EPROM, the other does not have to be installed; the circuitry sees a missing EPROM the same way it sees an unprogrammed one. It also sees a missing daughter board the same way it sees two unprogrammed EPROMs.

Note: Removal of the daughter board under power is not recommended unless necessary; bending and flexing of the XM16KP should be carefully avoided, so as not to move the backplane connector pins.

4.4 OPERATOR'S REFERENCE

This section is intended as a quick reference for the operator of the XM16KP(-D) board. Manual operation of the board is summarized to facilitate its use without detailed understanding of the mechanism behind the functions.

4.4.1 Online Operation

To put the XM16KP(-D) board into its normal, fully automatic on mode, the following steps have to be taken, depending on whether it is being done under power or with the controller cardcage powered down:

With controller card cage initially powered down:

1. Insert EPROM(s) containing proper microcode into the sockets on the daughter board.
2. Insert the daughter board into its nest in the main board.
3. Set the ON toggle switch (SW2) to ON; although it is not mandatory, it is a good practice to set all other switches to OFF;
4. Power up the controller card cage.

Note: Removal of the daughter board under power is not recommended unless necessary; bending and flexing of the XM16KP should be carefully avoided, so as not to move the backplane connector pins.

The microcode will be loaded and checked automatically upon power up and once this is completed 46 ms later, the XM16KP(-D) will come on, thereby causing the microcode execution to commence. The on status is indicated by a green LED (DS6) on. This board behavior will always repeat upon power up if only SW2 is ON.

With controller card cage under power:

1. Set all switches on XM16KP to OFF.
2. Insert the XM16KP card into the card cage (if it's not already there). All LEDs should be off.
3. Insert EPROM(s) containing proper microcode into the sockets on the daughter board.
4. Insert the daughter board into its nest in the main board.
5. Set the EPROM ENABLE/DISABLE switch (SW3) to ON. (Yellow EPROMENBLD LED (DS9) comes on.)
6. Depress the RESET switch (SW1). DS9 LED goes off for 46 ms and comes back on again, indicating that microcode has been successfully loaded from the EPROMs into the main board's SRAM, and then checked for proper parity. The board is now ready to be switched on.

7. Although not mandatory, it is a good practice to turn the SW3 OFF. (DS9 LED goes off.)
8. Set the ON switch ON. The green DS6 LED comes on, indicating that the XM16KP(-D) is on, and the XMCP commenced execution of the microcode (always from location zero).

Note: Removal of the daughter board under power is not recommended unless necessary; bending and flexing of the XM16KP should be carefully avoided, so as not to move the backplane connector pins.

Note that if a power up occurs at some point after the completion of the above steps, the entire bootstrap process will occur automatically as described in item 1 above (because the SW2 is ON).

See section 4.3.2 for information regarding the error conditions.

4.4.2 Offline Operation

Section 4.1 describes how to execute all steps required to place the XM16KP(-D) on, which is its normal operating mode within the system. However, individual functions like loading the microcode, checking the parity of the main board's SRAM contents (i.e. dry run), and resetting the control circuitry, can be performed separately in the offline mode (i.e. with SW2 OFF) by activating the appropriate switches. All possible manual operations are summarized in Figure 4.6.

4.4.3 Error Conditions

Errors may occur during each of the above procedures. These would be indicated by the appearance of one of two red LEDs (DS7 and DS8). The board's circuitry then "locks-up" in the offline mode and cannot be put on until the error condition is cleared. Careful repetition of all steps is recommended.

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SECTION 5 OPERATORS CONTROL PANEL MULTIWIRE (OCPM)

5.1 DESCRIPTION

The OCPM (in conjunction with the OCP keyboard) contains all the operational control functions and system status indicators for the mass storage subsystem.

The OCPM provides the linkage via the OCPM keyboard to interrupt the XMCP board and execute these functions. The OCPM also receives information from the system operating microcode and displays this information via status registers and indicators.

The OCPM contains an 8085 microprocessor (and its own microcode) to handle the interface between keyboard functions and the OCPM board. A function is entered via the keyboard which will interrupt the system operating microcode (XMCP). Once the system operating microcode has been interrupted, the information is latched into the XMCP board and will be acknowledged during idle time. The system operating microcode will perform the function during idle time, then acknowledge the OCPM that it was completed via the CT bus. The OCPM may be interrupted either from the "A" side or "B" side control unit. The control unit that interrupted the OCPM first will be acknowledged prior to honoring any other request. The OCPM also contains all the displays and status indicators used in indicating the state of the system configuration and operating status. Status RAMS on the OCPM board contain the state (i.e. cache, write thru, bypass, etc.) of each drive. The state of the drives may be changed during online operation without interruption to system operation. The OCPM board controls an alphanumeric display board used for displaying information about system status, diagnostic information, system error messages, and messages requiring operator response.

5.2 BLOCK DIAGRAM DESCRIPTION

Commands are received via the instruction bus from either the "A" side or "B" side of the controller. Refer to the lower left hand corner of Figure 5.1, OCPM Block Diagram, for an illustration of the A and B sides. In order for the OCPM to process a command from a control unit, the OCPM must first be selected by that control unit. If the selection was successful, the OCPM will then present status via the CT bus indicating the OCPM is available. If the OCPM is available, further command processing may take place. If the OCPM is not available, this indicates the OCPM is currently processing a command from the other control unit. If the OCPM was not available to the control unit, the same controller will retry the selection process at a later time.

Operator intervention will take place via the keyboard and the keyboard interface. The keyboard interface will then interrupt the OCPM 8085 microprocessor board and the 8085 microprocessor board will determine what the command was and display the message on the alphanumeric display. Messages that require operator intervention may now be entered via the keyboard. After responding to messages via the keyboard, the 8085 microprocessor board will interrupt (via channel "A" or channel "B" CT bus) the system operating microcode. The system operating microcode will then execute the command on the lowest priority basis. A typical example of this OCPM 8085 microprocessor interrupt process would be the performance of an in line diagnostic routine (ILD).

Status and error register information selected by the thumbwheel switches via the CT bus will be displayed on the OCPM board. Other miscellaneous information such as status RAM registers, XMCP address compare/sync logic, reset logic, switches and indicators are also contained on the OCPM board.

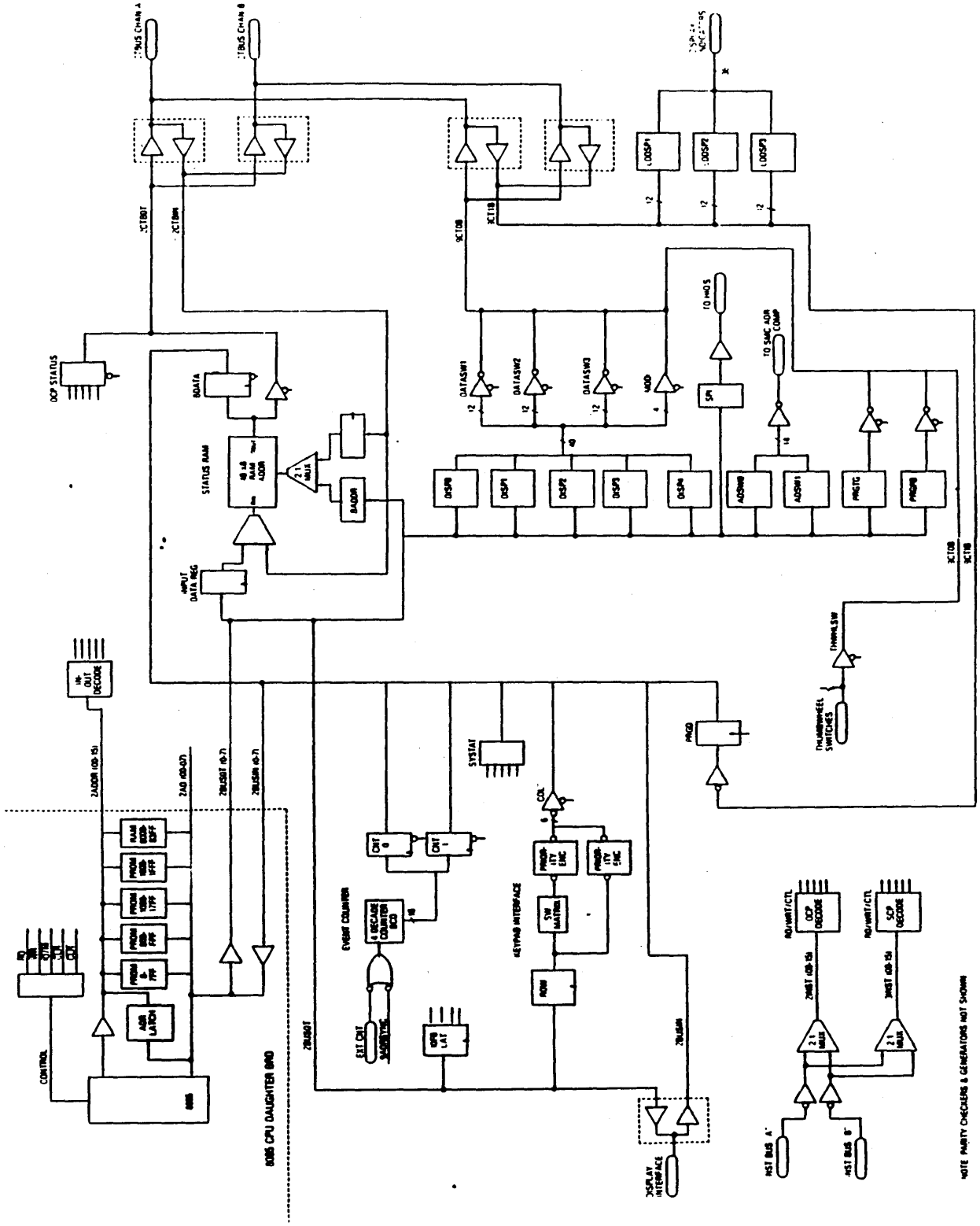
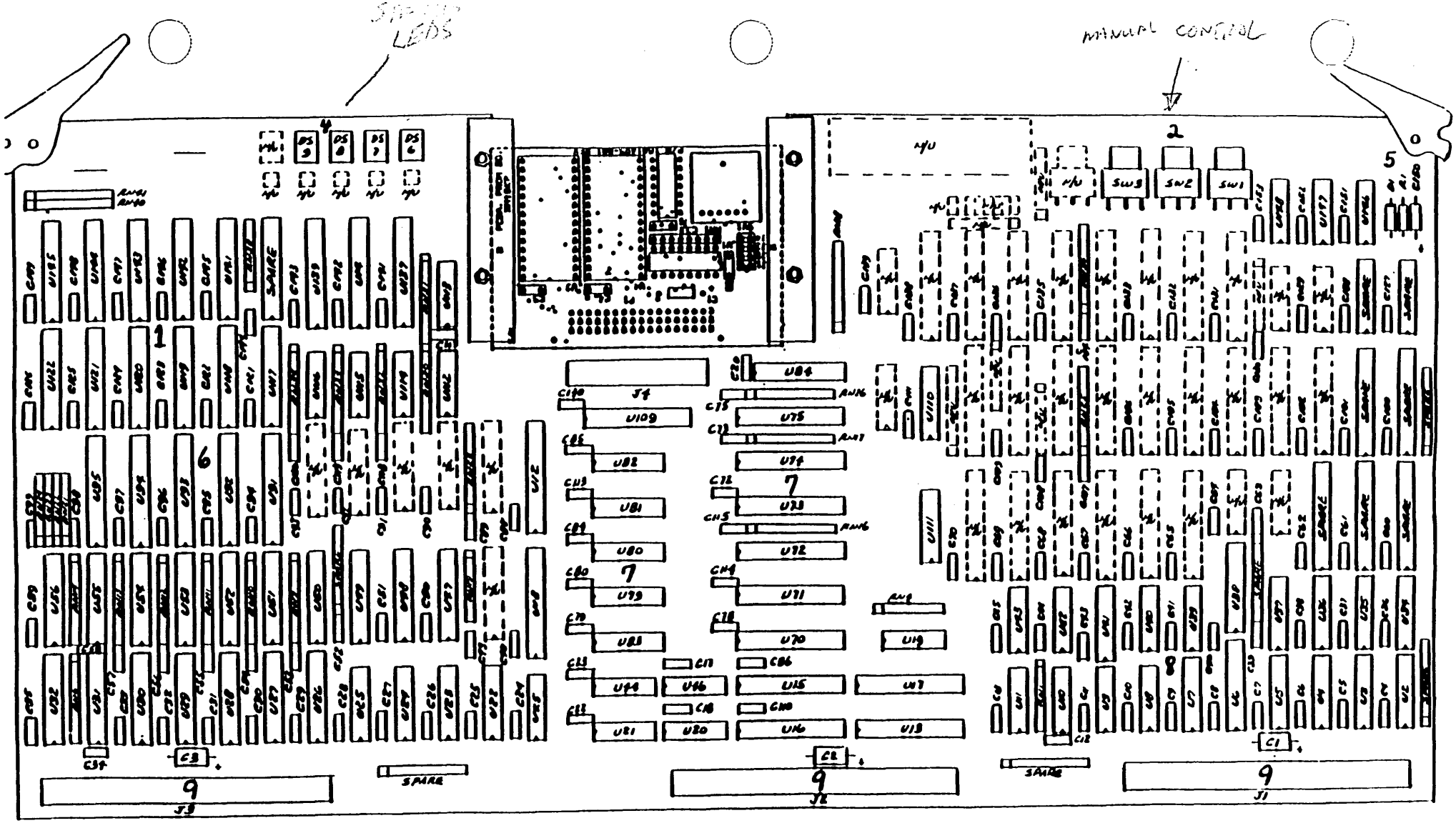


Figure 5.1 OCPM Block Diagram



XM16KP Component Layout

1 - Microprogram memory (SRAM)
2 - Manual control switches
3 - Daughter Board (XM16KP-D)
4 - Status LEDs
5 - Power up circuitry
6 - Pipeline register
7 - Control logic
8 - Stack logic
9 - Backplane connector

Figure 6-15
XM16KP Component Layout

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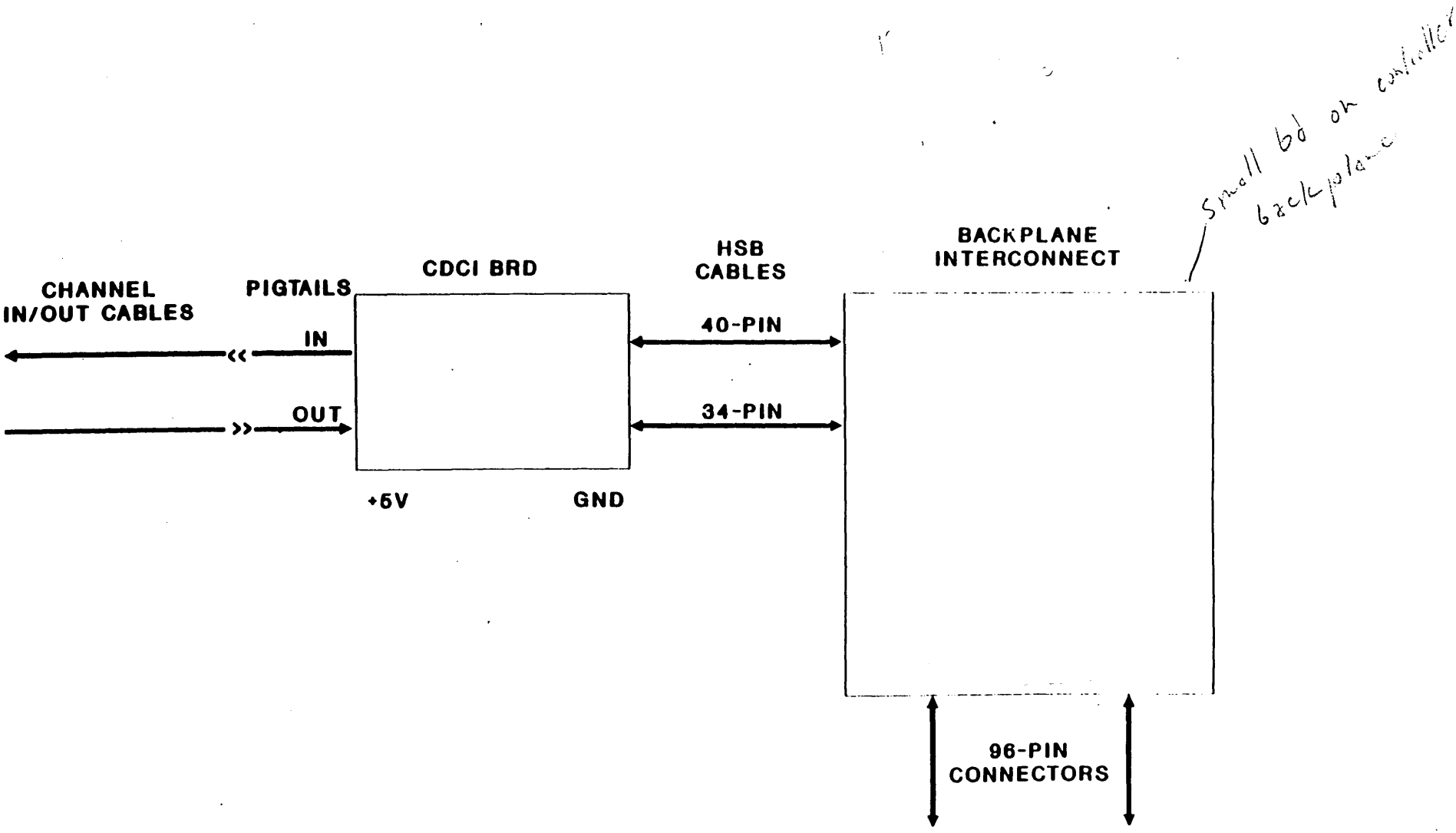
CHANNEL
IN/OUT CABLES
PIGTAILS
IN
OUT
CDCI BRD
+5V
GND
HSB
CABLES
40-PIN
34-PIN
BACKPLANE
INTERCONNECT
96-PIN
CONNECTORS

FROM CHANNEL

ACTIVE - Indicates PPU is ready to send or receive data.

INACTIVE - Indicates PPU has disconnected the channel and is not ready to send or receive.

FULL - Indicates PPU is placing valid data on the data lines.

EMPTY - Indicates PPU has received the data sent.

FUNCTION - Indicates that the valid data is to be interpreted as a command.

MASTER CLEAR - Indicates the PPU has been reset and the interface board should be reset also.

10 MHZ CLOCK - Is the timing signal used by the CDCI board to sync the data and other signals it wants to send to the PPU.

1 MHZ CLOCK - Not used.

TO CHANNEL

FULL - Indicates CDCI board is placing valid data on interface.

EMPTY - Indicates CDCI received data from PPU.

INACTIVE - Sent to PPU in response to some functions.

CYBER CHANNEL I/O CABLES

CDC OUT

PIN	SIGNAL	DIRECTION
C	BIT 2	→
F	BIT 5	→
K	BIT 8	→
N	BIT 11	→
S	FULL OUT	→
V	MASTER CLEAR	→
B	BIT 1	→
E	BIT 4	→
J	BIT 7	→
M	BIT 10	→
R	INACTIVE OUT	→
U	FUNCTION OUT	→
A	BIT 0	→
D	BIT 3	→
H	BIT 6	→
L	BIT 9	→
P	ACTIVE OUT	→
T	EMPTY OUT	→
W	PARITY OUT	→

CDC IN

PIN	SIGNAL	DIRECTION
C	BIT 2	←
F	BIT 5	←
K	BIT 8	←
N	BIT 11	←
S	FULL	←
V	1 MHZ CLK	→
B	BIT 1	←
E	BIT 4	←
J	BIT 7	←
M	BIT 10	←
R	INACTIVE	←
U	10 MHZ CLK	→
A	BIT 0	←
D	BIT 3	←
H	BIT 6	←
L	BIT 9	←
P	ACTIVE	←
T	EMPTY	←
W	PARITY IN	←

LEGEND

→ • FROM CPU TO CTLR

← • FROM CTLR TO CPU

ITM	REVISION		

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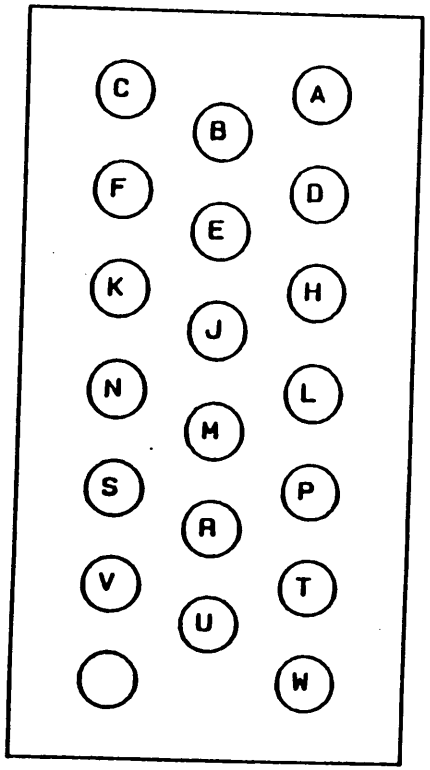
C	WHITE/RED
F	WHITE/GREEN
K	WHITE/GRAY
N	WHITE/BLACK/BROWN
S	WHITE/BLACK/YELLOW
V	WHITE/BLACK/VIOLET
B	WHITE/BROWN
E	WHITE/YELLOW
J	WHITE/VIOLET
M	WHITE/BLACK/BLACK
R	WHITE/BLACK/ORANGE
U	WHITE/BLACK/BLUE
A	WHITE/BLACK
D	WHITE/ORANGE
H	WHITE/BLUE
L	WHITE/WHITE
P	WHITE/BLACK/RED
T	WHITE/BLACK/GREEN
W	WHITE/BLACK/GRAY



ECO 2588
SH 108

ITEM	QTY.	MFR.	PART NUMBER

Protronyx

DRAWN	DATE	DRAWING NO. 25001150	REV.
CHECKED		AMP. CDC OUT CABLE	A
APPROVED		DO NOT SCALE DRAWING	

LTR	DESCRIPTION OF REVISION	APP.	DATE

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connector to CDCI cable.

50-PIN CONNECTOR-END VIEW (vs Wire Insertion End)

2	1
4	3
6	5
8	7
10	9
12	11
14	13
16	15
18	17
20	19
22	21
24	23
26	25
28	27
30	29
32	31
34	33
36	35
38	37
40	39
42	41
44	43
46	45
48	47
50	49

SHIELD	SIGNAL	COAX COLOR CODE
1	2	White/Black
3	4	White/Brown
5	6	White/Red
7	8	White/Orange
9	10	White/Yellow
11	12	White/Green
13	14	White/Blue
15	16	White/Violet
17	18	White/Gray
19	20	White/White
21	22	White/Black/Black
23	24	White/Black/Brown
33	34	White/Black/Red
35	36	White/Black/Orange
29	30	White/Black/Yellow
31	32	White/Black/Green
37	38	White/Black/Blue
39	40	White/Black/Violet
25	26	White/Black/Gray

NOTE: Test to insure there is no continuity between each shield and signal pair; i.e., 1 & 2, 3 & 4, etc.

ECO 2588
SH 109

SHEET 4 OF 4

ITEM	QTY.	MFR.	PART NUMBER

Protronyx

DRAWN	DATE	DRAWING NO. 25001150	REV. A
CHECKED		AMP. CDC OUT CABLE	
APPROVED		DO NOT SCALE DRAWING	

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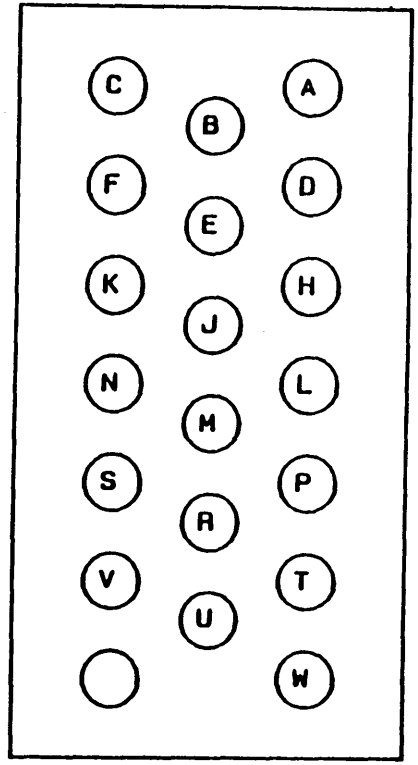
C	WHITE/RED
F	WHITE/GREEN
K	WHITE/GRAY
N	WHITE/BLACK/BROWN
S	WHITE/BLACK/YELLOW
V	WHITE/BLACK/VIOLET
B	WHITE/BROWN
E	WHITE/YELLOW
J	WHITE/VIOLET
M	WHITE/BLACK/BLACK
R	WHITE/BLACK/ORANGE
U	WHITE/BLACK/BLUE
A	WHITE/BLACK
D	WHITE/ORANGE
H	WHITE/BLUE
L	WHITE/WHITE
P	WHITE/BLACK/RED
T	WHITE/BLACK/GREEN
W	WHITE/BLACK/GRAY



ECO 2588
SH 113

ITEM	QTY.	MFR.	PART NUMBER

SHEET 3 OF 4

Protronyx

DRAWN	DATE	DRAWING NO. 25001100 AMP. CDC IN CABLE	REV. A
CHECKED			
APPROVED		DO NOT SCALE DRAWING	

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note: CDC pigtails in/out are not the same.

50-PIN
CONNECTOR-END VIEW
(vs Wire Insertion End)

2	1
4	3
6	5
8	7
10	9
12	11
14	13
16	15
18	17
20	19
22	21
24	23
26	25
28	27
30	29
32	31
34	33
36	35
38	37
40	39
42	41
44	43
46	45
48	47
50	49

SHIELD	SIGNAL	COAX COLOR CODE
1	2	White/Black
3	4	White/Brown
5	6	White/Red
7	8	White/Orange
9	10	White/Yellow
11	12	White/Green
13	14	White/Blue
15	16	White/Violet
17	18	White/Gray
19	20	White/White
21	22	White/Black/Black
23	24	White/Black/Brown
25	26	White/Black/Red
29	30	White/Black/Orange
33	34	White/Black/Yellow
31	32	White/Black/Green
37	38	White/Black/Blue
35	36	White/Black/Violet
27	28	White/Black/Gray

NOTE: Test to insure there is no continuity between each shield and signal pair; i.e., 1 & 2, 3 & 4, etc.

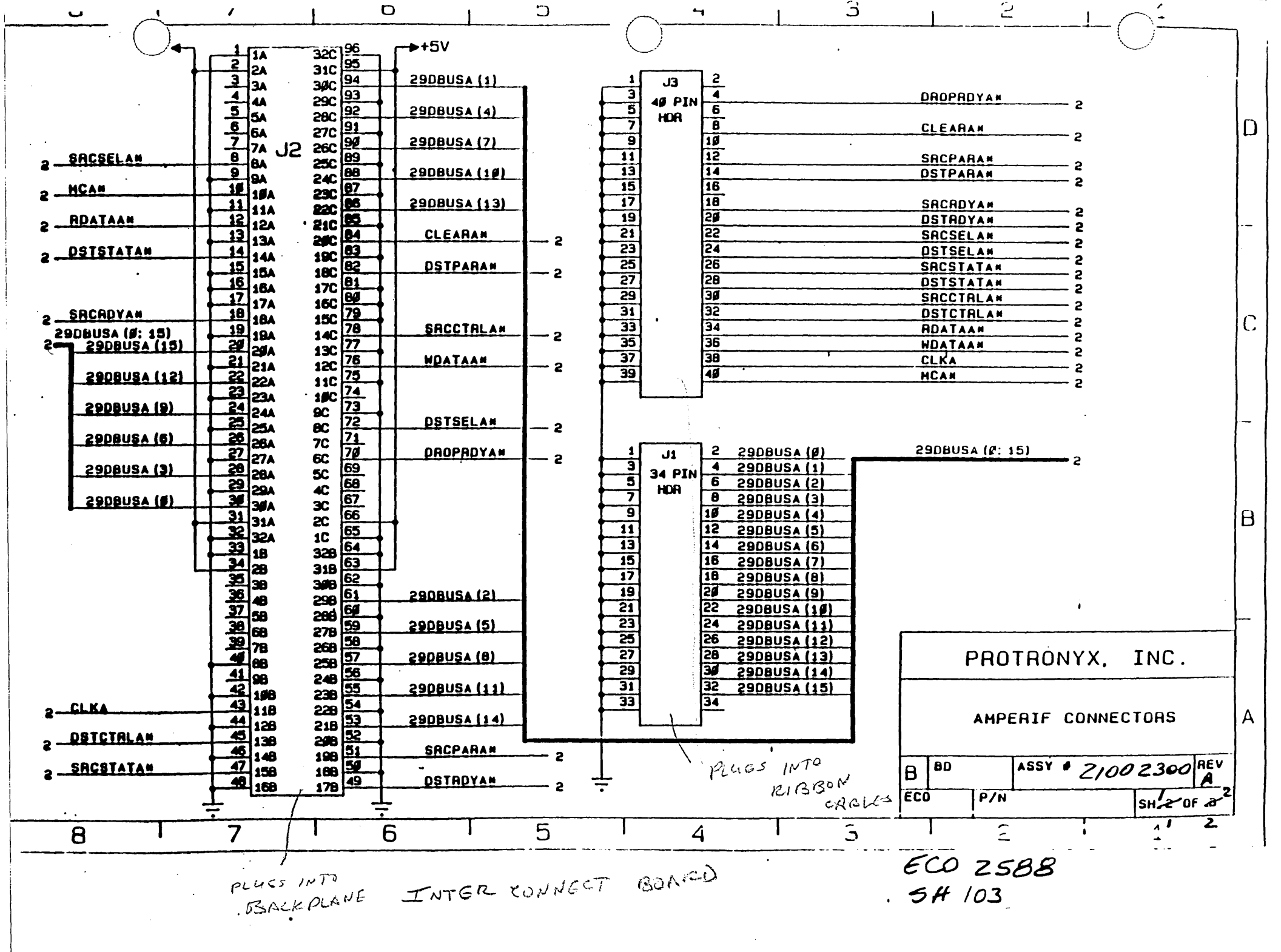
ITEM	QTY.	MFR.	PART NUMBER

ECO 2588
SH 114

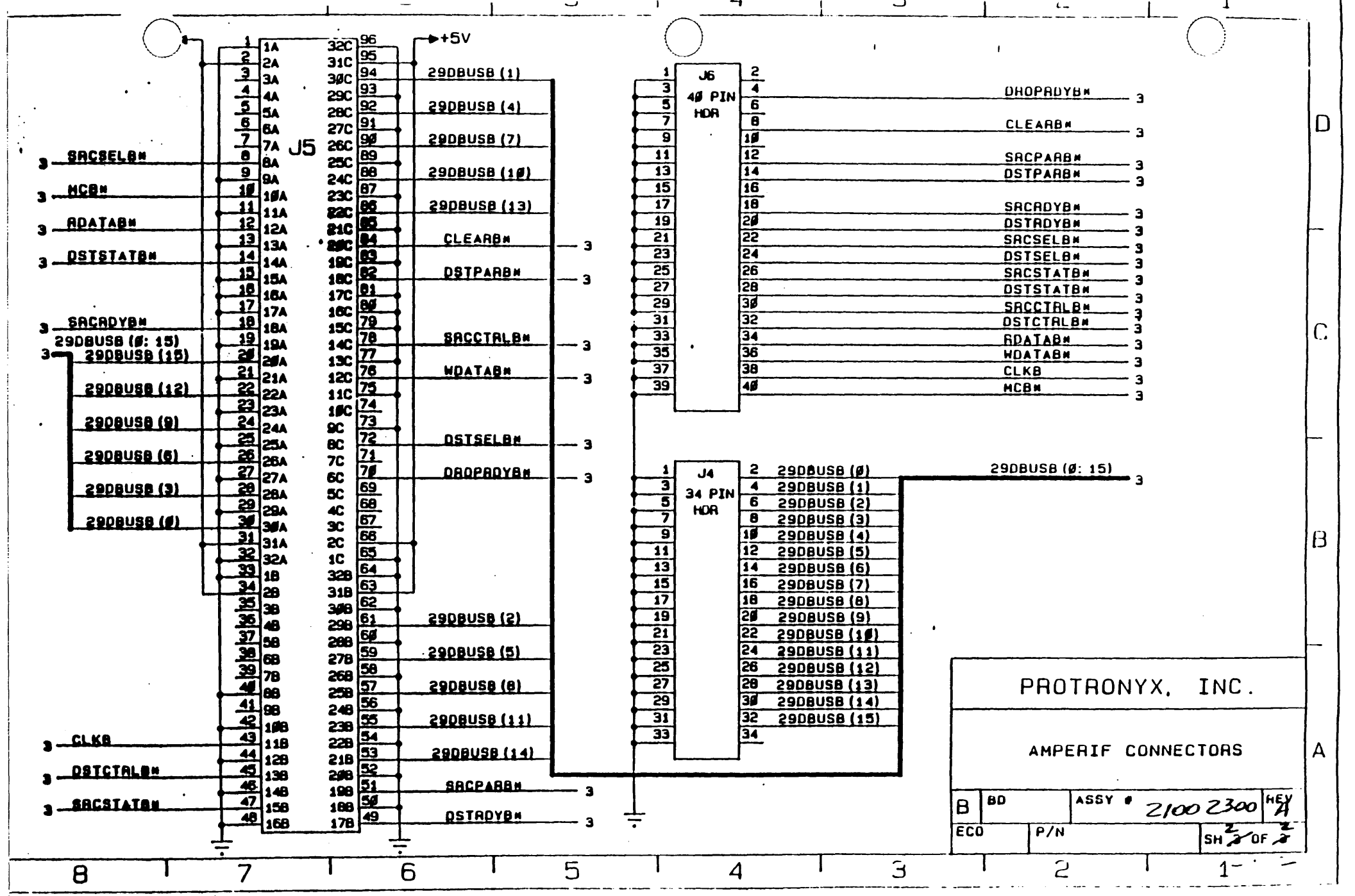
SHEET 4 OF 4

Protronyx

DRAWN	DATE	DRAWING NO. 25001100	REV. A
CHECKED		AMP. CDC IN CABLE	
APPROVED		DO NOT SCALE DRAWING	

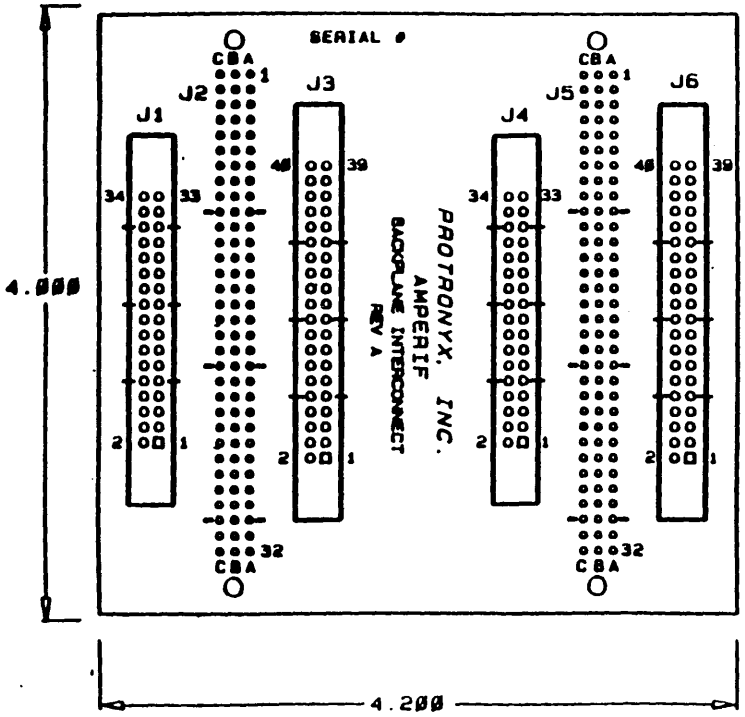


ECO 2588
SH 103



2nd half of Interconnect board

ECO 2588
SH 104



20002300

AMPERIF
BACKPLANE INTERCONNECT BOARD
MANUFACTURING INFORMATION

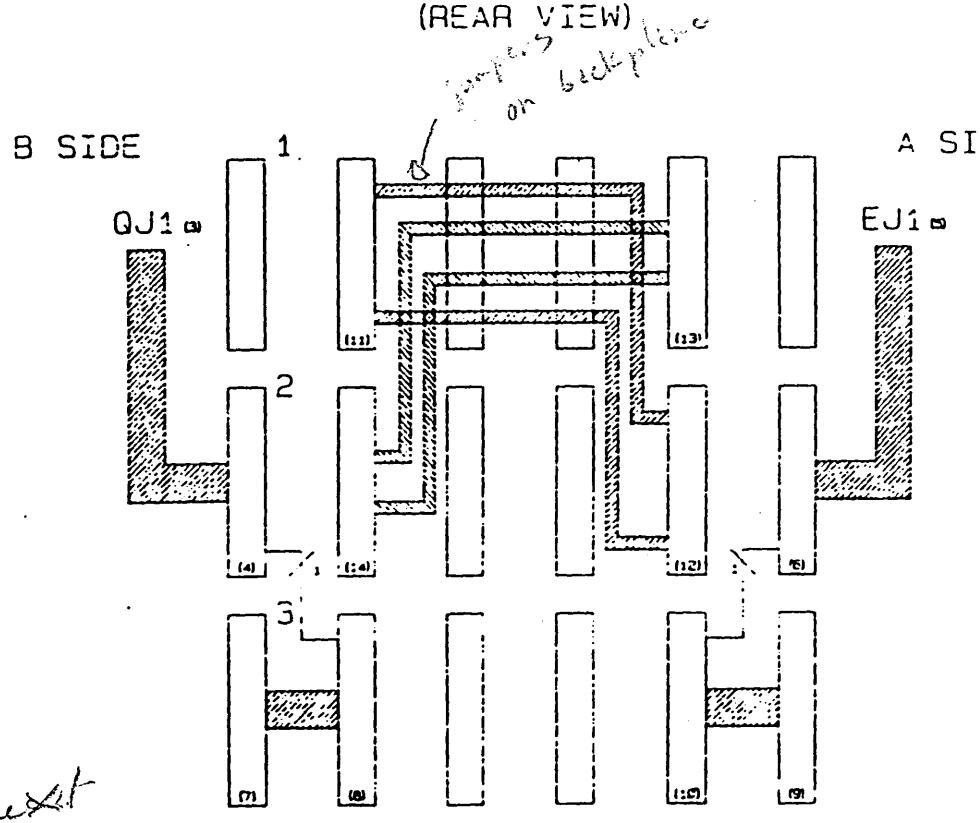
TWO-SIDED BOARD
THICKNESS = .093
SILKSCREEN ON BOTH COMPONENT
AND CIRCUIT SIDE
SILKSCREEN MUST BE WHITE
COMPONENTS MOUNTED ON BOTH
SIDES OF THE BOARD
EXACT DIMENSIONS ARE 3.9 X 4.2
HOLE COUNT: 344
4 HOLES ARE .125
340 HOLES ARE .035
ALL HOLES ARE PLATED THRU
SOLDERMASK BOTH SIDES OF BD

ECO 2588
SH 105

INTERCONNECT BOARD
LAYOUT

MIDDLE MOTHERBOARD SLOTS

(REAR VIEW)



- INDICATE WIREWRAP CONNECTIONS
- COLUMNS L AND K ARE NOT REFERENCED IN THIS DOCUMENT
- NUMBERS WITHIN PARENTHESES INDICATE A SHEET REFERENCE

see next 8 pages for

PROTACNYX, INC.			
AMPERIF MOTHERBOARD WIRING SLOT DIAGRAM			
B	BD	ASSY #	REV
ECO	P/N	2 OF 14	

AMPERIF MOTHERBOARD WIRING

QJ1	NJ2	MJ3	U-BUS
A26	A14		EFREQB
A28	A17		SETEIB
A29	A18		RSTEIB
A30	B14		DENCHTB/DENCHT
B3	B3		CLK1HIB/CLK1
B4	B4		RSTODID/RSTODIDB
B5	B5		UMPRSTB
B6	B6		SIDFLGB
B7	B7		EFINTB
B8	B8		URSPTOB
B9	B9		SPITRMB/EISENTB
B10	B10		UBPAR1B/UBPARIB
B11	B11		SETODRB
B12	B12		HIOLD/2HAIOLD
B13	B13		SETAUTO/SETAUTB
B15	B15		FILAC23B
B17	B17		CLK2HIB/CLK2
B18	B18		SPILCH1
B19	B19		SPILCH2
B20	B20		SPILCH3
B21	B21		SPILCH4
B22	B22		SPIEF1
B23	B23		SPIEF2
B24	B24		SPIEF3
B25	B25		SPIEF4
C25	A19		EFAVLB
C26	A20		USYSCRB
C28	A21	C10	SYSRST/SYSRSTB
C29	A22		SPILCHN/SPILCHA
C30	A23		SMEINER/ERSTATUSB

connection th

Signal name

EJ1	HJ2	JJ3	U-BUS
A26	A14		EFREQA/EFREQB
A28	A17		SETEIA/SETEIB
A29	A18		RSTEIA/RSTEIB
A30	B14		DENCHTA/DENCHT
B3	B3		CLK1HIA/CLK1
B4	B4		RSTODIA/RSTODIDB
B5	B5		UMPRSTA/UMPRSTB
B6	B6		SIDFLGA/SIDFLGB
B7	B7		EFINTA/EFINTB
B8	B8		URSPTOA/URSPTOB
B9	B9		SPITRMA/EISENTB
B10	B10		UBPAR1A/UBPARIB
B11	B11		SETODRA/SETODRB
B12	B12		HIOLDA/2HAIOLD
B13	B13		SETAUTA/SETAUTB
B15	B15		FILA23A/FILAC23B
B17	B17		CLK2HIA/CLK2
B18	B18		SPILC1A/SPILCH1
B19	B19		SPILC2A/SPILCH2
B20	B20		SPILC3A/SPILCH3
B21	B21		SPILC4A/SPILCH4
B22	B22		SPIEF1A/SPIEF1
B23	B23		SPIEF2A/SPIEF2
B24	B24		SPIEF3A/SPIEF3
B25	B25		SPIEF4A/SPIEF4
C25	A19		EFAVLA/EFAVLB
C26	A20		USYSCRA/USYSCRB
C28	A21	C10	SYSRSTA/SYSRSTB
C29	A22		SPILCHA
C30	A23		SMEINEA/ERSTATUSB

NOTE: The U-BUS names contain the version of name for the motherboard and the version on the PC board to which they connect. I.E. "EFREQA" is the correct name for the signal at EJ1-A26. However, its connection at HJ2-A14 (to the UBI board) is named "EFREQB" on the board logics.

MJ3	NJ3	29DBUS & CONTROL
A8	A8	SRCSEL*
A9	A9	GND
A10	A10	MC*
A11	A11	GND
A12	A12	RDATA*
A13	A13	GND
A14	A14	DSTSTAT*
A15	A15	GND
A17	A17	GND
A18	A18	SRCRDY*
A19	A19	GND
A20	A20	29DBUS(15)
A21	A21	GND
A22	A22	29DBUS(12)
A23	A23	GND
A24	A24	29DBUS(9)
A25	A25	GND
A26	A26	29DBUS(6)
A27	A27	GND
A28	A28	29DBUS(3)
A29	A29	GND
A30	A30	29DBUS(0)
B8	B8	GND
B10	B10	GND
B11	B11	CLK
B12	B12	GND
B13	B13	DSTCTRL*
B14	B14	GND
B15	B15	SRCSTAT*
B17	B17	DSTRDY*
B18	B18	GND
B19	B19	SRCPAR*
B20	B20	GND
B21	B21	29DBUS(14)
B22	B22	GND
B23	B23	29DBUS(11)
B24	B24	GND
B25	B25	29DBUS(8)
B26	B26	GND
B27	B27	29DBUS(5)
B28	B28	GND
B29	B29	29DBUS(2)
B30	B30	GND
C8	C8	DSTSEL*

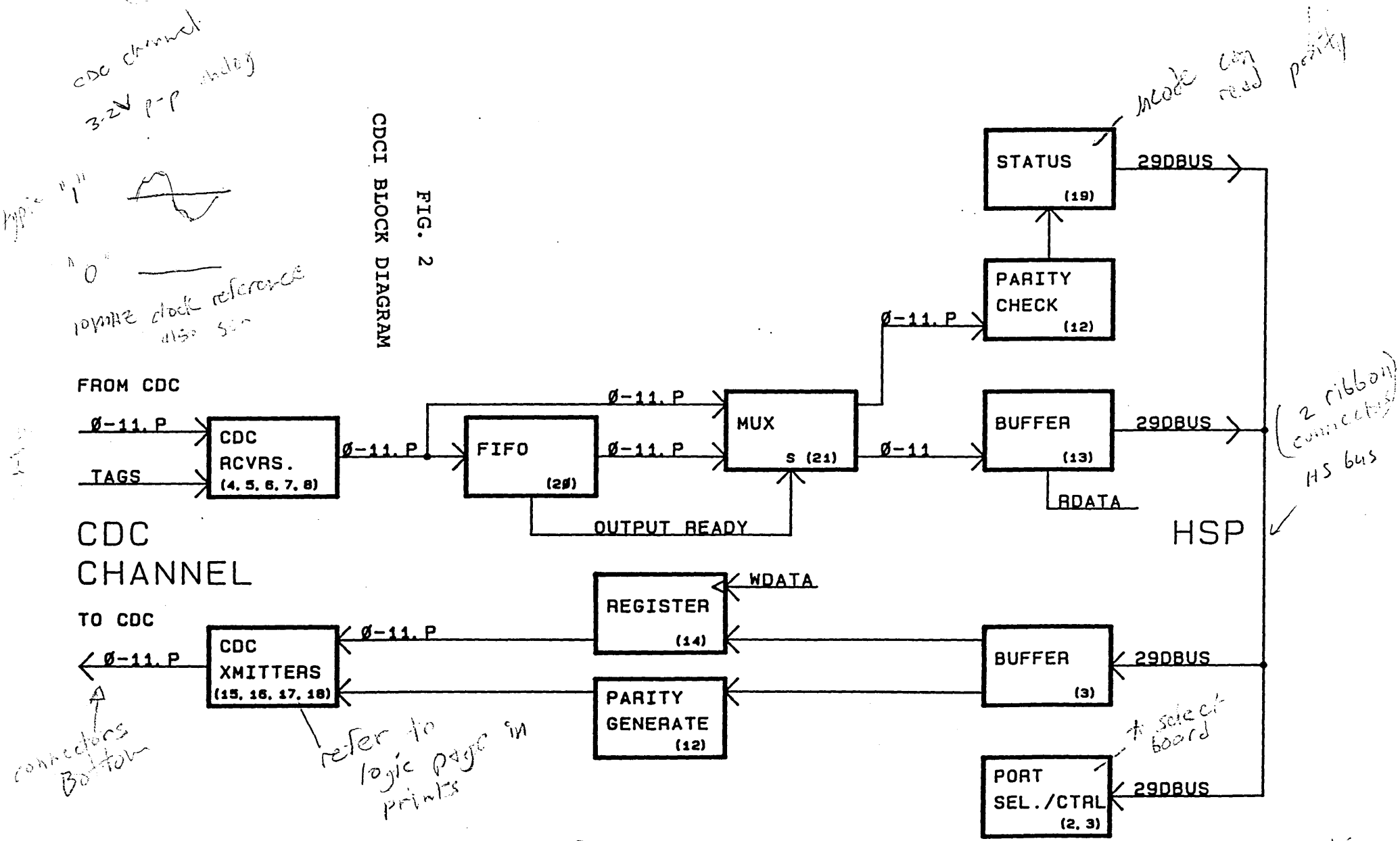
MJ3	NJ3	29DBUS & CONTROL
C9	C9	GND
C11	C11	GND
C12	C12	WDATA*
C13	C13	GND
C14	C14	SRCCTRL*
C15	C15	GND
C17	C17	GND
C18	C18	DSTPAR*
C19	C19	GND
C21	C21	GND
C22	C22	29DBUS(13)
C23	C23	GND
C24	C24	29DBUS(10)
C25	C25	GND
C26	C26	29DBUS(7)
C27	C27	GND
C28	C28	29DBUS(4)
C29	C29	GND
C30	C30	29DBUS(1)

HJ3	JJ3	29DBUS & CONTROL
A8	A8	SRCSEL*
A9	A9	GND
A10	A10	MC*
A11	A11	GND
A12	A12	RDATA*
A13	A13	GND
A14	A14	DSTSTAT*
A15	A15	GND
A17	A17	GND
A18	A18	SRCRDY*
A19	A19	GND
A20	A20	29DBUS(15)
A21	A21	GND
A22	A22	29DBUS(12)
A23	A23	GND
A24	A24	29DBUS(9)
A25	A25	GND
A26	A26	29DBUS(6)
A27	A27	GND
A28	A28	29DBUS(3)
A29	A29	GND
A30	A30	29DBUS(0)
B8	B8	GND
B10	B10	GND
B11	B11	CLK
B12	B12	GND
B13	B13	DSTCTRL*
B14	B14	GND
B15	B15	SRCSTAT*
B17	B17	DSTRDY*
B18	B18	GND
B19	B19	SRCPAR*
B20	B20	GND
B21	B21	29DBUS(14)
B22	B22	GND
B23	B23	29DBUS(11)
B24	B24	GND
B25	B25	29DBUS(8)
B26	B26	GND
B27	B27	29DBUS(5)
B28	B28	GND
B29	B29	29DBUS(2)
B30	B30	GND
C8	C8	DSTSEL*

HJ3	JJ3	29DBUS & CONTROL
C9	C9	GND
C11	C11	GND
C12	C12	WDATA*
C13	C13	GND
C14	C14	SRCCTRL*
C15	C15	GND
C17	C17	GND
C18	C18	DSTPAR*
C19	C19	GND
C21	C21	GND
C22	C22	29DBUS(13)
C23	C23	GND
C24	C24	29DBUS(10)
C25	C25	GND
C26	C26	29DBUS(7)
C27	C27	GND
C28	C28	29DBUS(4)
C29.	C29	GND
C30	C30	29DBUS(1)

JJ2	MJ1	STATUS BUFFER PORT IN/PORT OUT
B3	B3	REMOTER/TREMOTE
B4	B4	PORTD(11)/TPORT(11)
B5	B5	PORTD(10)/TPORT(10)
B6	B6	GND
B7	B7	PORTD(9)/TPORT(9)
B8	B8	PORTD(8)/TPORT(8)
B9	B9	GND
B10	B10	PORTD(7)/TPORT(7)
B11	B11	PORTD(6)/TPORT(6)
B12	B12	GND
B13	B13	PORTD(5)/TPORT(5)
B14	B14	PORTD(4)/TPORT(4)
B15	B15	GND
B17	B17	PORTD(2)/TPORT(2)
B18	B18	GND
B19	B19	PORTD(1)/TPORT(1)
B20	B20	PORTD(0)/TPORT(0)
B21	B21	GND
B22	B22	PORTPA(2)/TPA(2)
B23	B23	PORTPA(1)/TPA(1)
B24	B24	GND
B25	B25	PORTPA(0)/TPA(0)
B26	B26	PAISTB*/PAOSTB*
B27	B27	GND
B28	B28	PDISTB*/PDOSTB*
B29	B29	PORTACKI*/PORTACKO*
B30	B30	PORTD(3)/TPORT(3)

MJ1	MJ2	STATUS BUFFER PORT IN/PORT OUT
B3	B3	TREMOTE/REMOTER
B4	B4	TPORT(11)/PORTD(11)
B5	B5	TPORT(10)/PORTD(10)
B6	B6	GND
B7	B7	TPORT(9)/PORTD(9)
B8	B8	TPORT(8)/PORTD(8)
B9	B9	GND
B10	B10	TPORT(7)/PORTD(7)
B11	B11	TPORT(6)/PORTD(6)
B12	B12	GND
B13	B13	TPORT(5)/PORTD(5)
B14	B14	TPORT(4)/PORTD(4)
B15	B15	GND
B17	B17	TPORT(2)/PORTD(2)
B18	B18	GND
B19	B19	TPORT(1)/PORTD(1)
B20	B20	TPORT(0)/PORTD(0)
B21	B21	GND
B22	B22	TPA(2)/PORTPA(2)
B23	B23	TPA(1)/PORTPA(1)
B24	B24	GND
B25	B25	TPA(0)/PORTPA(0)
B26	B26	PAOSTB*/PAISTB*
B27	B27	GND
B28	B28	PDOSTB*/PDISTB*
B29	B29	PORTACKO*/PORTACKI*
B30	B30	TPORT(3)/PORTD(3)


CDCI BLOCK DIAGRAM
FIG. 2
FROM CDC
Ø-11, P
TAGS
CDC RCVRS. (4, 5, 6, 7, 8)
Ø-11, P
FIFO (2Ø)
Ø-11, P
Ø-11, P
MUX S (21)
Ø-11
Ø-11, P
PARITY CHECK (12)
STATUS (19)
29DBUS
BUFFER (13)
29DBUS
RDATA
OUTPUT READY
CDC CHANNEL
HSP
TO CDC
Ø-11, P
CDC XMITTERS (15, 16, 17, 18)
Ø-11, P
REGISTER (14)
WDATA
PARITY GENERATE (12)
BUFFER (3)
29DBUS
PORT SEL./CTRL (2, 3)
29DBUS

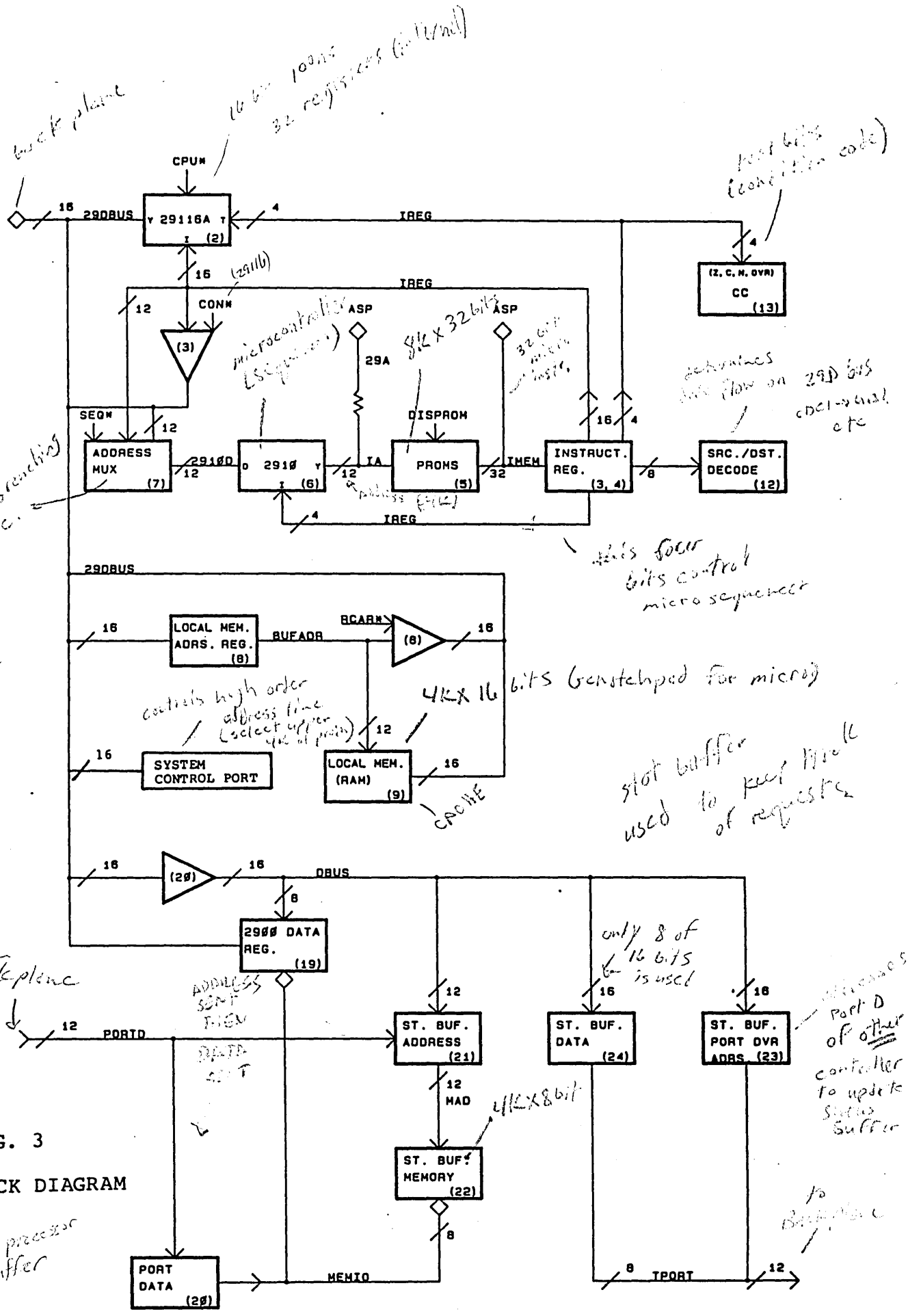


FIG. 3

HSP BLOCK DIAGRAM

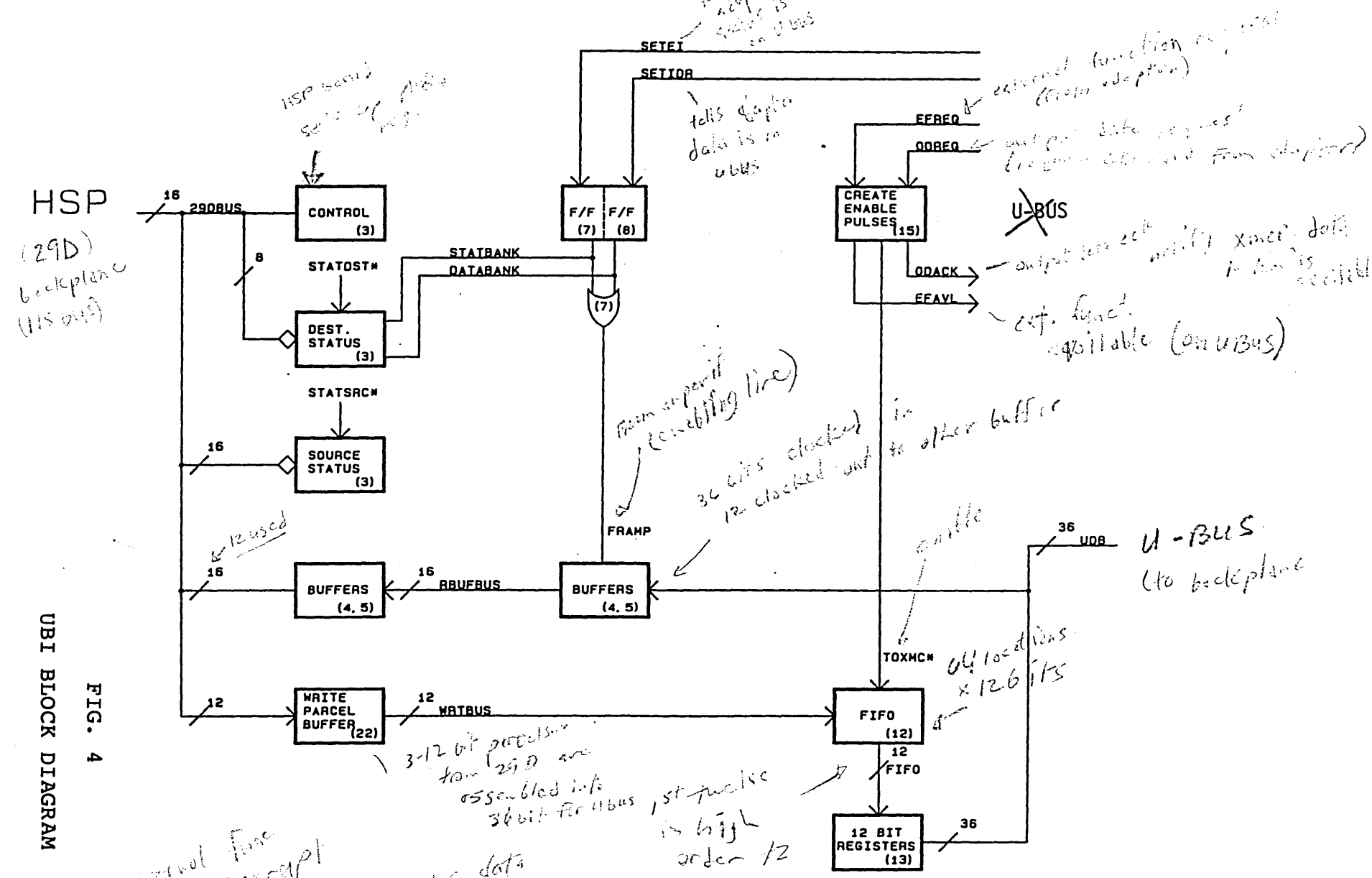
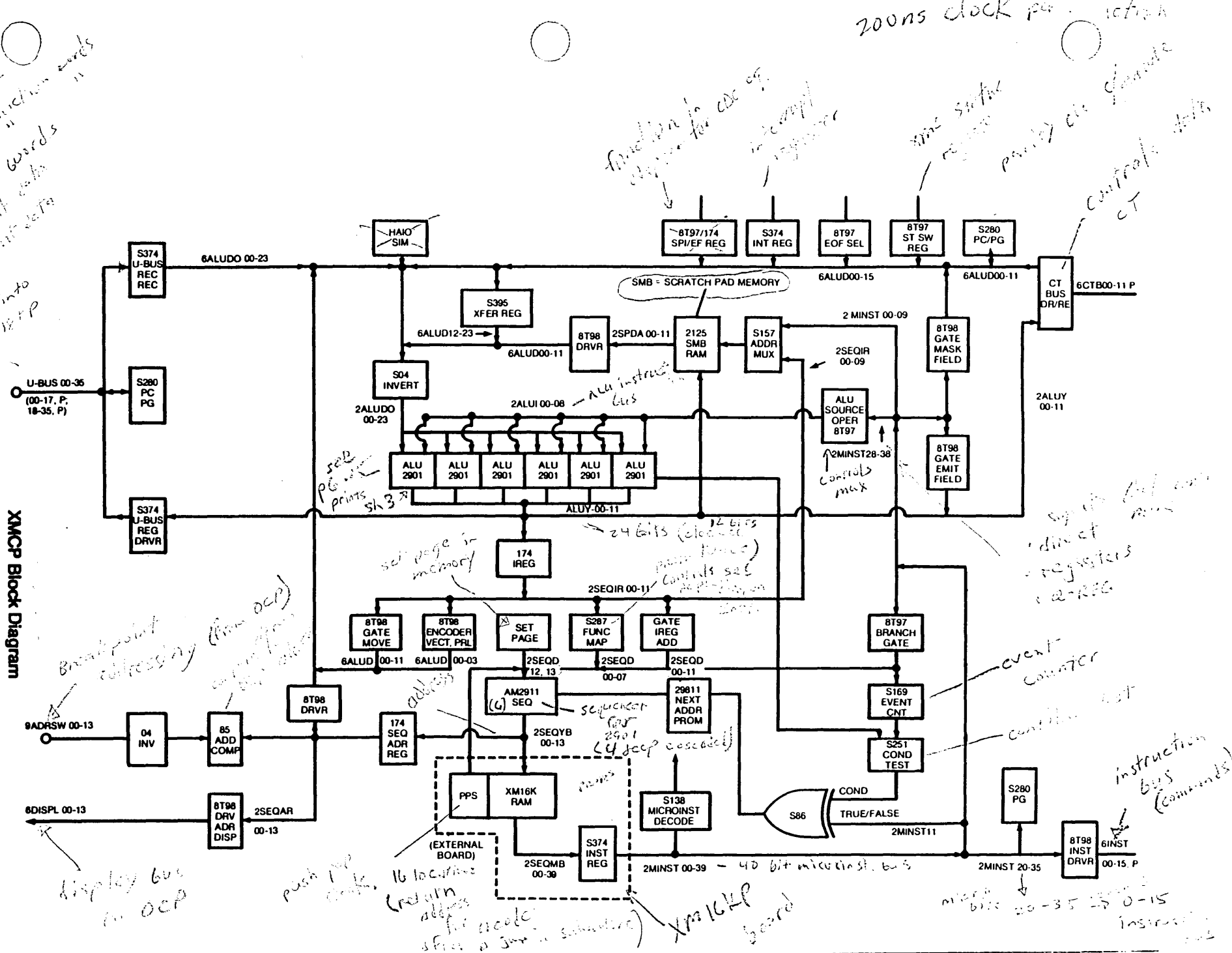
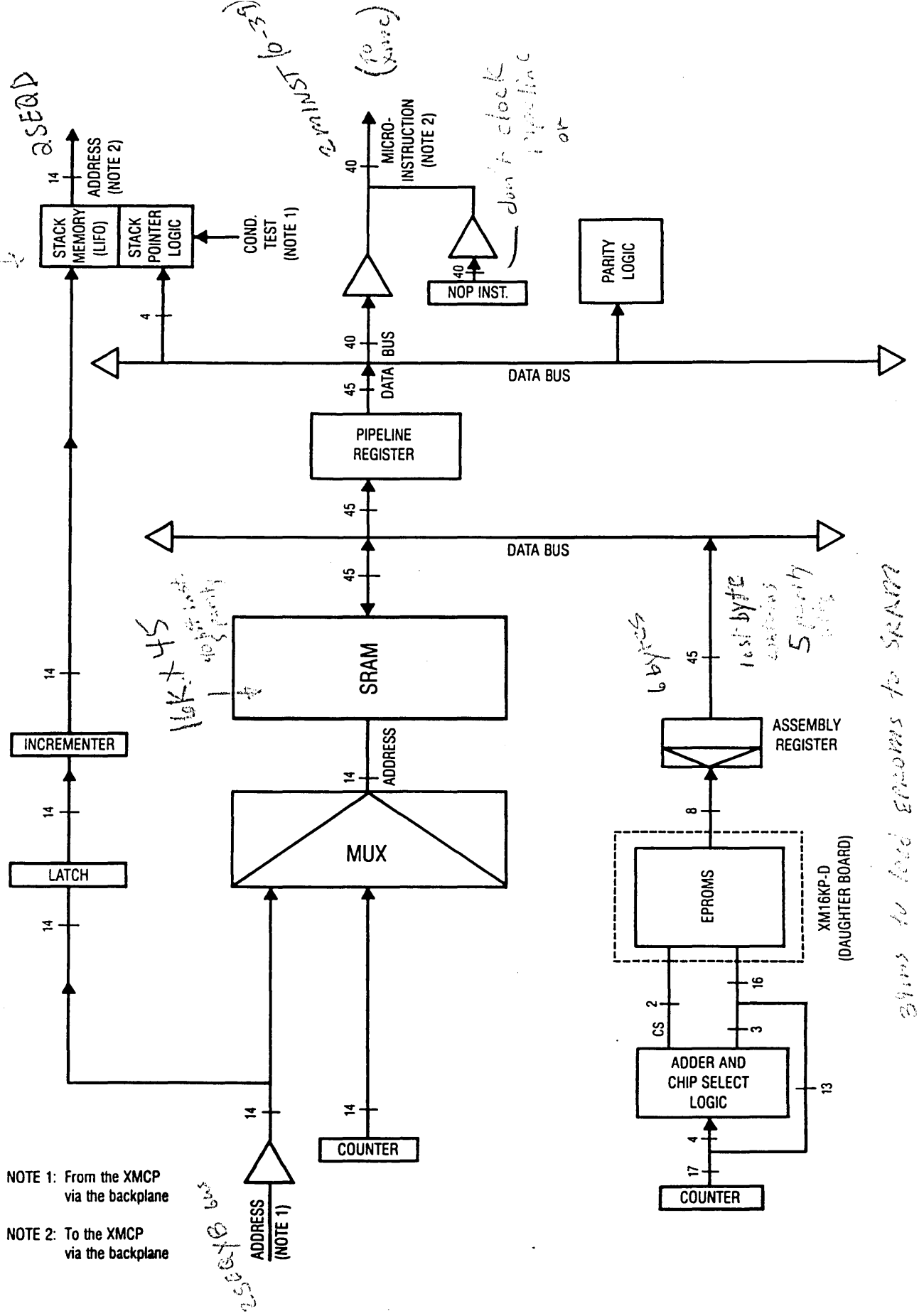


FIG. 4

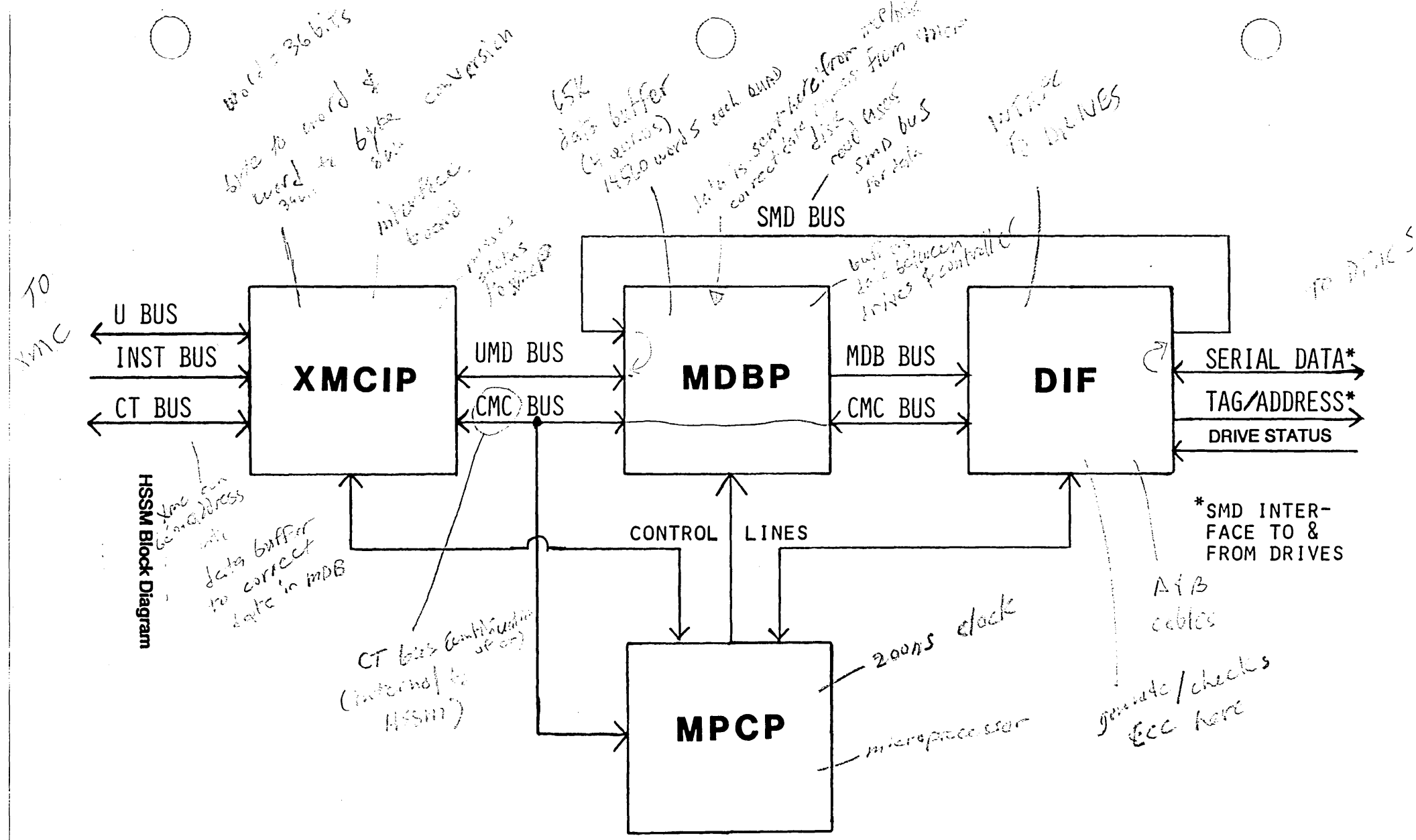
UBI BLOCK DIAGRAM


XMCP Block Diagram
S374 U-BUS REC REC
6ALUDO 00-23
HAIO SIM
8T97/174 SPI/EF REG
S374 INT REG
8T97 EOF SEL
8T97 ST SW REG
S280 PC/PG
6ALUD00-15
6ALUD00-11
CT BUS DR/RE
6CTB00-11 P
SMB = SCRATCH PAD MEMORY
S395 XFER REG
6ALUD12-23
8T98 DRVR
2SPDA 00-11
2125 SMB RAM
S157 ADDR MUX
2 MINST 00-09
2SEQIR 00-09
8T98 GATE MASK FIELD
U-BUS 00-35
(00-17, P; 18-35, P)
S280 PC PG
S04 INVERT
2ALUDO 00-23
2ALUI 00-08
ALU SOURCE OPER 8T97
2MINST28-38
2ALUY 00-11
8T98 GATE EMIT FIELD
ALU 2901
ALU 2901
ALU 2901
ALU 2901
ALU 2901
ALU 2901
S374 U-BUS REG DRVR
ALUY-00-11
24 bits
174 IREG
2SEQIR 00-11
8T98 GATE MOVE
8T98 ENCODER VECT. PRL
SET PAGE
S287 FUNC MAP
GATE IREG ADD
6ALUD 00-11
6ALUD 00-03
2SEQD 12, 13
2SEQD 00-07
2SEQD 00-11
8T97 BRANCH GATE
AM2911 (4) SEQ
29811 NEXT ADDR PROM
S169 EVENT CNT
9ADRSW 00-13
04 INV
85 ADD COMP
8T98 DRVR
174 SEQ ADR REG
2SEQYB 00-13
S251 COND TEST
PPS
XM16K RAM
S138 MICROINST DECODE
COND
S86
TRUE/FALSE
2MINST11
S280 PG
6DISPL 00-13
8T98 DRV ADR DISP
2SEQAR 00-13
(EXTERNAL BOARD)
2SEQMB 00-39
S374 INST REG
2MINST 00-39
2MINST 20-35
8T98 INST DRVR
6INST 00-15, P

4.

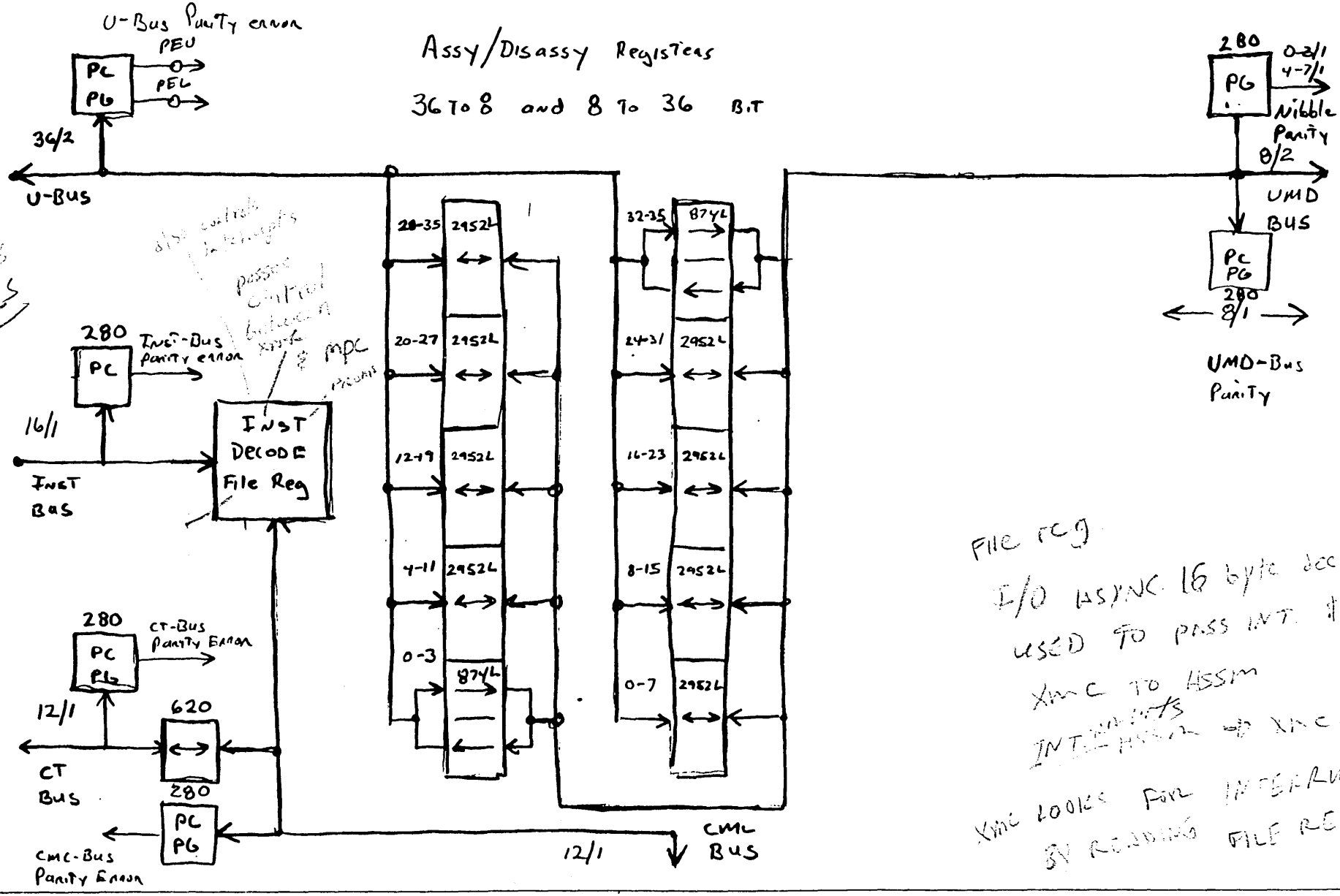


XM16KP(-D) - Block Diagram



HSSM BLOCK DIAGRAM

XMCIP



FILE REG

I/O ASYNC 16 byte deep RAM

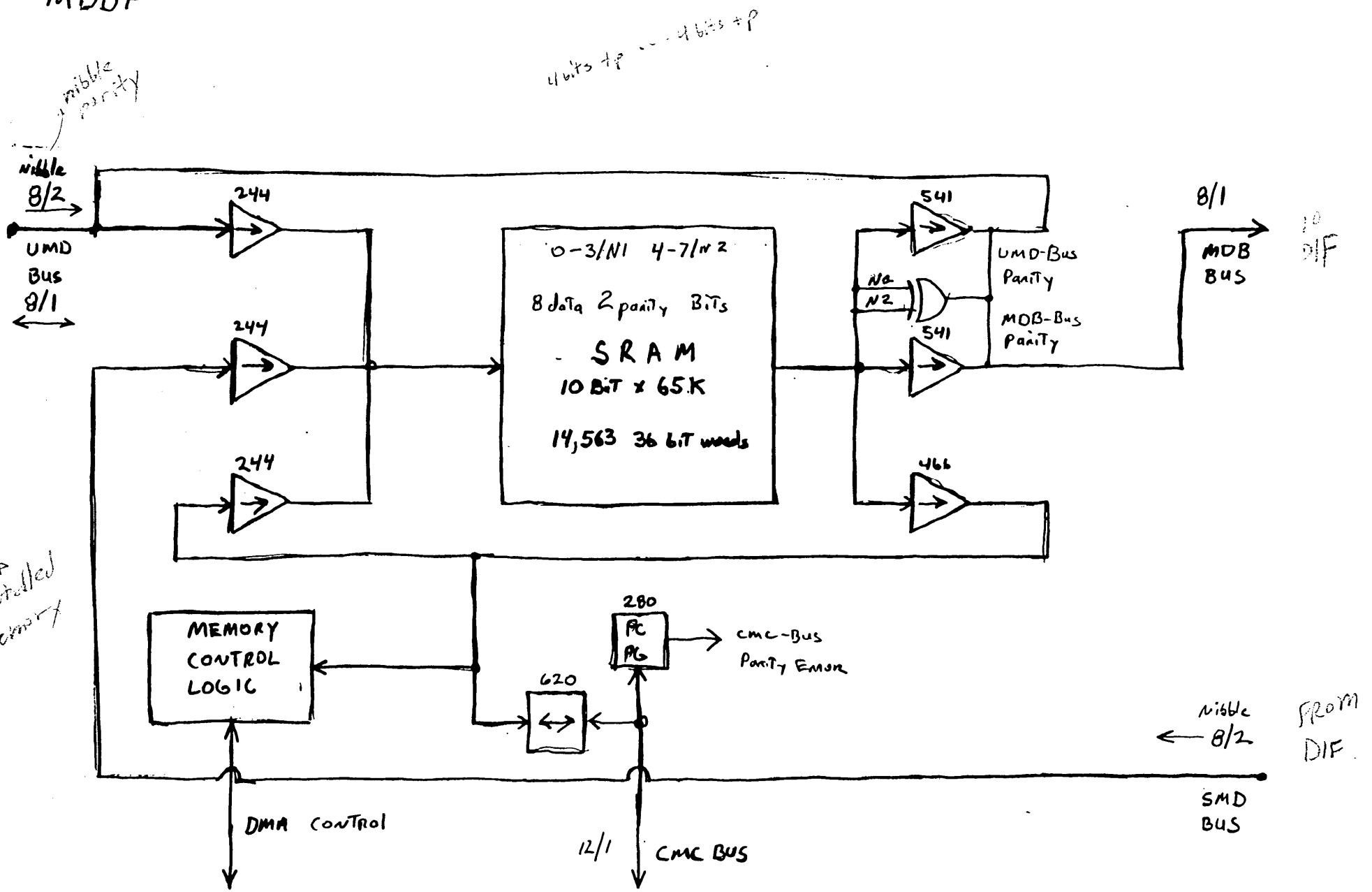
USED TO PASS INT. & CONT

XMC TO ASSM

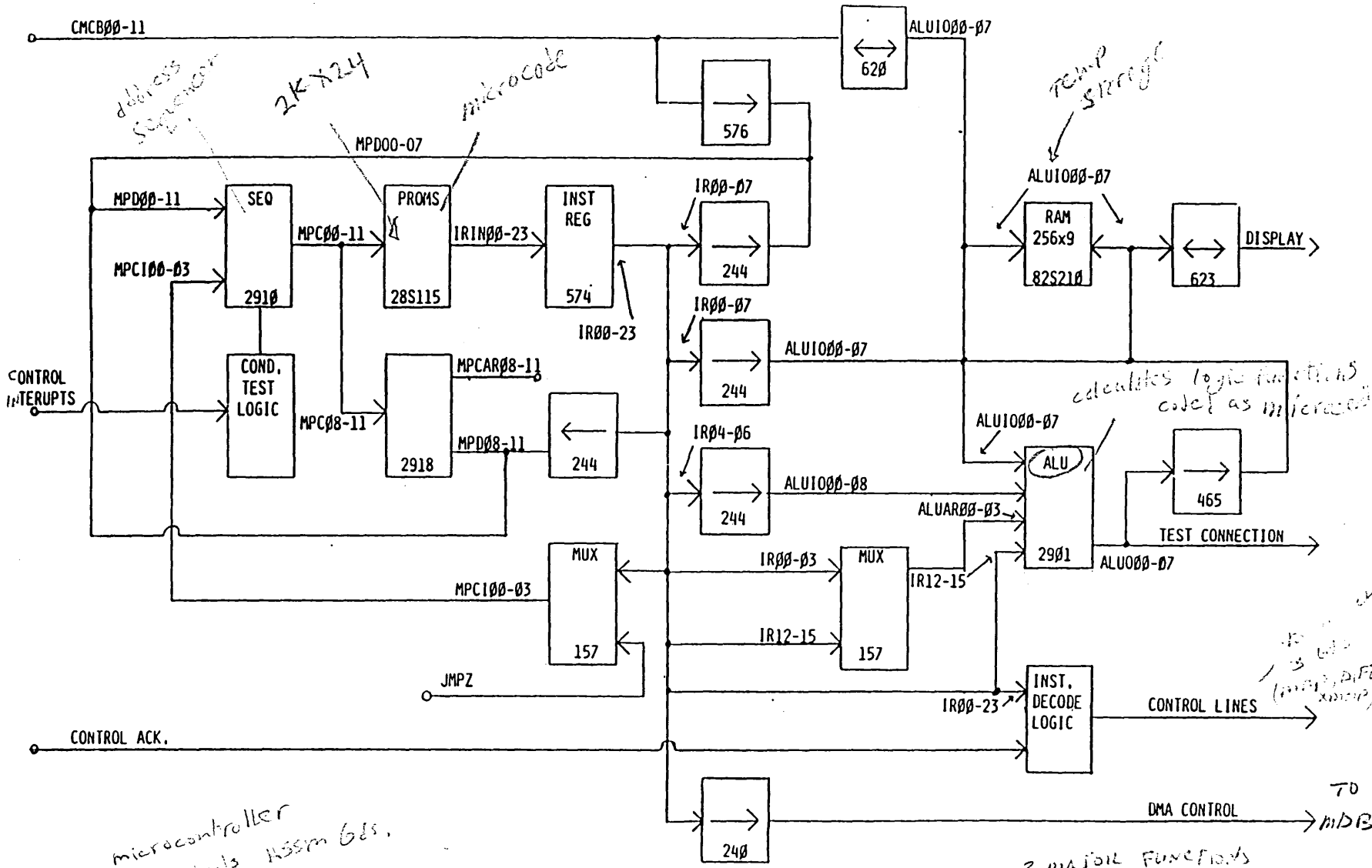
INTERRUPTS

XMC LOOKS FOR INTERRUPTS BY READING FILE REG.

MDBP


nibble parity
nibble 8/2
UMD Bus 8/1
244
244
244
0-3/N1 4-7/N2
8 data 2 parity Bits
SRAM
10 BIT x 65K
14,563 36 bit words
541
541
466
Na
N2
UMD-Bus Parity
MDB-Bus Parity
8/1
MDB BUS
DMA controlled memory
MEMORY CONTROL LOGIC
280
PC
PG
CMC-Bus Parity Error
620
nibble 8/2
FROM DIF
SMD BUS
DMA CONTROL
12/1
CMC BUS

8



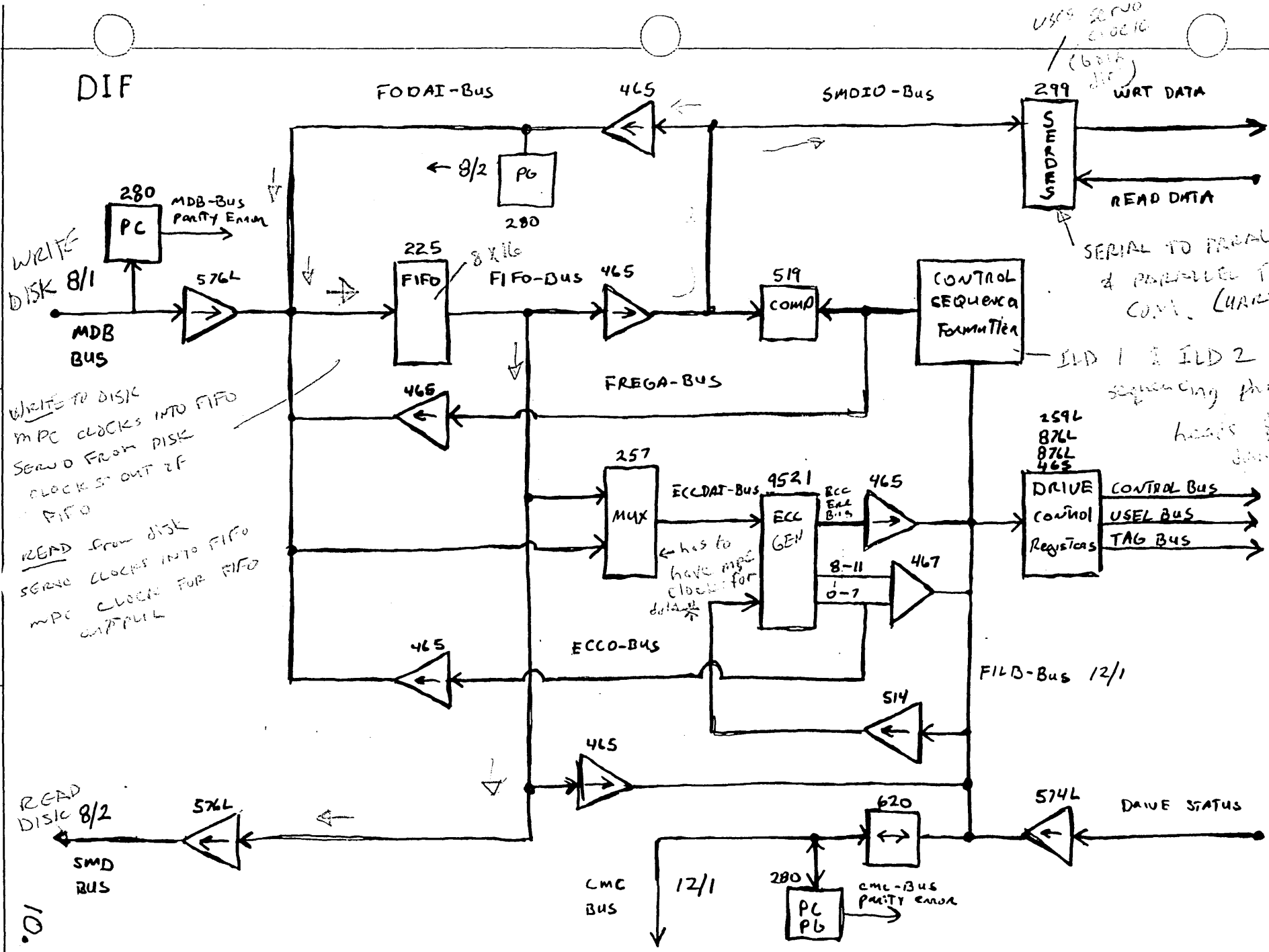
MPCP Block Diagram

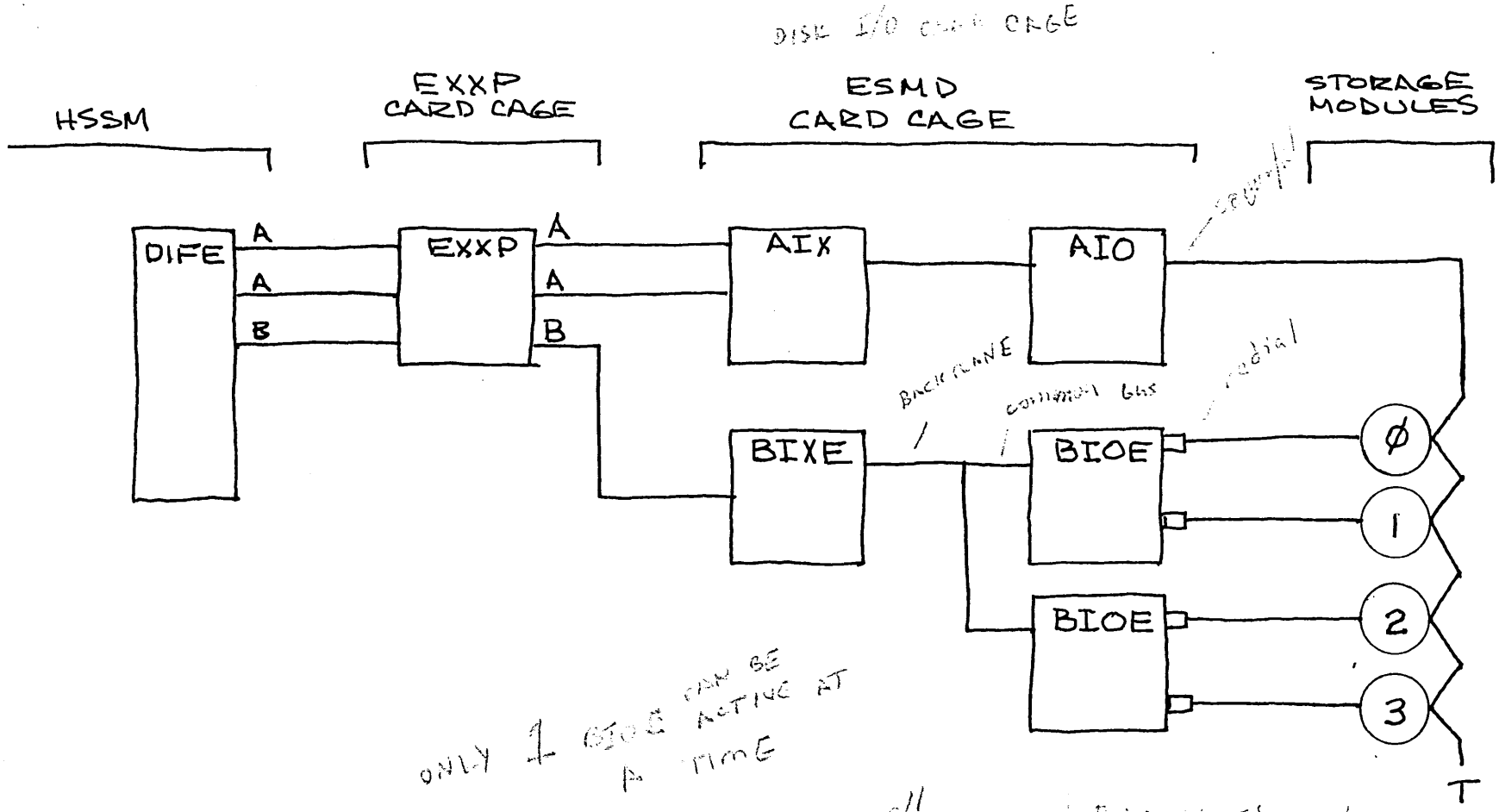
MPC BLOCK DIAGRAM

(HSSM controller)

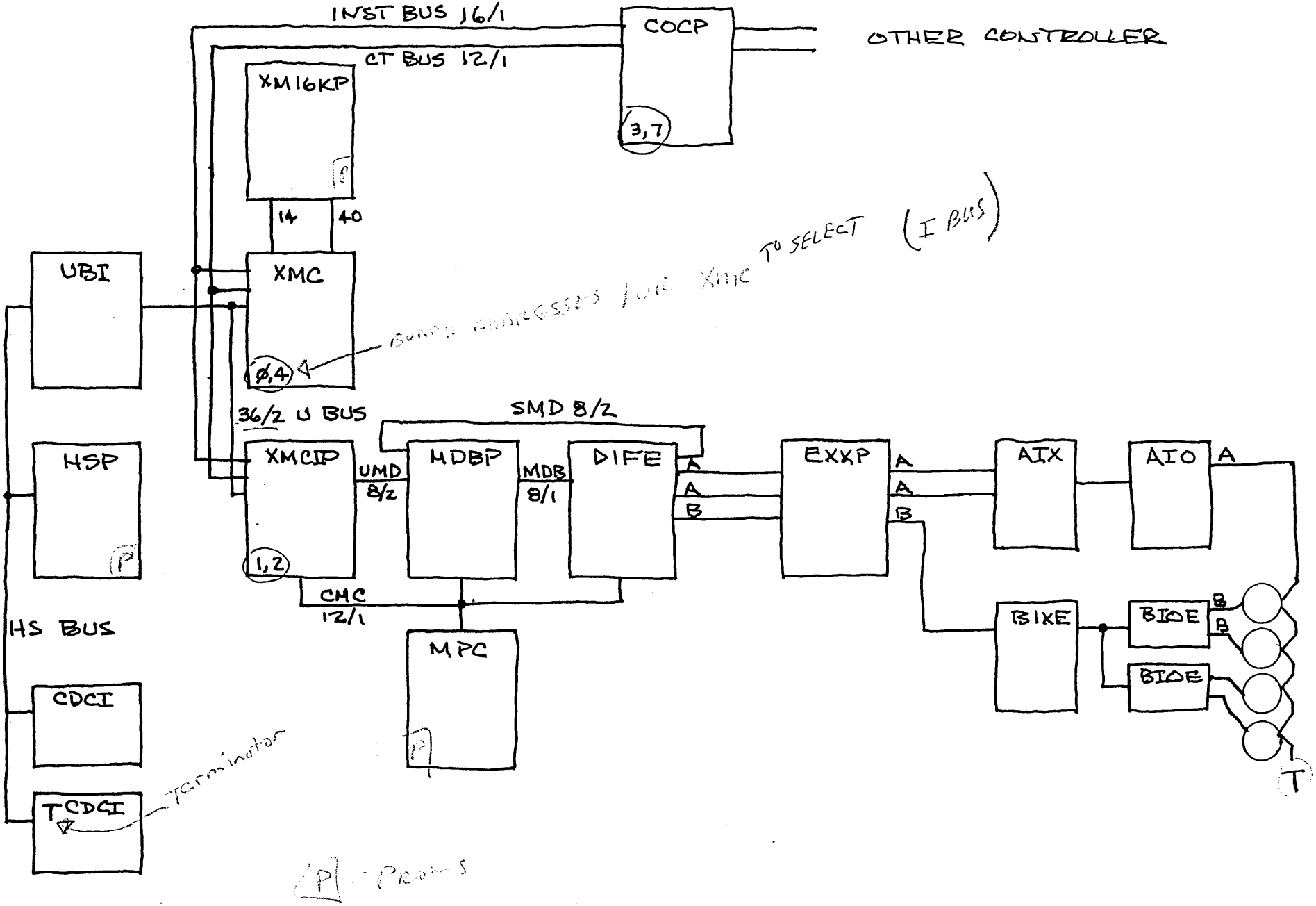
microcontroller controls HSSM bds.

3 MAJOR FUNCTIONS
1. sets DMA
2. monitors status of bds


DIF
FODAI-Bus
465
SMDIO-Bus
299
SERDES
WRT DATA
READ DATA
SERIAL TO PARALLEL & PARALLEL TO SERIAL CONV. (UART?)
280
PC
MDB-Bus Parity Error
WRITE DISK 8/1
MDB BUS
574L
225
FIFO
8 X 16
FIFO-Bus
465
519
COMP
CONTROL SEQUENCE FORMATTER
ILD 1 & ILD 2 sequencing through
FREGA-BUS
WRITE TO DISK
mPC CLOCKS INTO FIFO
SERVO FROM DISK
CLOCKS OUT OF FIFO
READ from disk
SERVO CLOCKS INTO FIFO
mPC CLOCK FOR FIFO CONTROL
257
MUX
ECCDAT-Bus
9521
ECC GEN
has to have mpc clock for data
ECC Err Bits
465
8-11
0-7
467
259L
876L
876L
465
DRIVE control Registers
CONTROL Bus
USEL Bus
TAG Bus
ECCO-BUS
FILD-Bus 12/1
514
READ DISK 8/2
574L
SMD BUS
620
574L
DRIVE STATUS
CMC BUS
12/1
280
PC Pb
cmc-Bus parity error
.01
PRIMARY 2 ECC GENERATORS


DISK I/O CARD CAGE
HSSM
EXXP CARD CAGE
ESMD CARD CAGE
STORAGE MODULES
DIFE
A
A
B
EXXP
A
A
B
AIX
AIO
BACKPLANE
common bus
radial
BIXE
BIOE
BIOE
ϕ
1
2
3
T
ONLY 1 BIOE CAN BE ACTIVE AT A TIME
1 BIOE can cause all drives to hang up if it has a problem
Drive addresses sent to A bus program drive responds on B cable.
disk port arbitration in each drive.

11



NATIONAL
42-381 50 SHEETS 5 SQUARE
42-382 100 SHEETS 5 SQUARE
42-389 200 SHEETS 5 SQUARE

6.9.3 Interface Specifications

Unit Selection

The drive must be selected before it will respond to any commands from the controller. This is the case because the tag and bus bit receivers, as well as certain transmitters, are not enabled until the drive is selected.

In both single and dual channel units, the select sequence is initiated by a Unit Select Tag signal from the controller. However, the sequence performed is different depending upon whether a single or dual channel is being considered. Since only one controller can communicate with the drive at a time, dual channel logic must solve the problem of priority when more than one controller wants to select the drive at the same time.

Signal	Meaning
	Function: Controller Selecting Drive
Unit Select Tag	This signal gates Unit Select Lines into logical number compare circuit. Unit is selected within 600 nanoseconds internal time lapse. Drive will not process commands until selected. A priority select status is indicated when the Unit Select Tag is accompanied by a Bus Bit 9 active. The drive is unconditionally selected and reserved by the channel issuing this command provided that both channels are enabled and a priority select condition does not exist on the other channel. Priority select is not used by the controller microcode. In dual-channel units, selection also causes the device to be reserved to the selecting channel. The reserve condition is cancelled by one of the following: 1. executing a Release command 2. the completion of the current operation provided the Release Timer Select switch on the card in slot A07 is set to RTM executing a priority select from the other channel
Unit Select Lines	A binary code is placed on these four lines to select a drive. The binary code must match the logical address of the drive defined by the position of four Unit Select switches on the card in slot B04/C04 of the logic chassis. Drives can be numbered 0 through 15.
Unit Selected	This line indicates that a drive has responded to the Unit Select Lines and the Unit Select Tag. This line must be active before the drive will respond to any command from the controller.
Open Cable Detector	A voltage is supplied by the controller to override the bias voltage at drive receiver. If the cable is disconnected or if controller power is lost, unit selection and controller commands are inhibited.

Signal	Meaning
	Function: Drive Indicates Operational Status
Unit Ready	This status line indicates that the drive is ready to accept commands and that no fault condition exists within the drive.
Index	This signal is derived from the servo tracks. It occurs once per revolution of the disk and its leading edge is the leading edge of sector zero.
Sector	This signal is derived from the servo tracks and is used to indicate the beginning of each sector on the track. The number of sector signals that occur for each revolution of the disk is switch selectable on the card at location B04/C04 in the logic chassis.
Busy	This signal is generated when a controller attempts to select or reserve a drive that has already been selected and/or reserved by the other controller. This signal is sent to the controller attempting the selection.
Write Protected	When this line is high, it indicates that the drive write circuits are disabled. The write protect mode is enabled by the WRITE PROTECT pushbutton switch on the operator panel, or by certain fault conditions. Attempting to write while the write protect mode is active results in a fault condition.
On Cylinder	This status line indicates that the heads are positioned at a usable cylinder and that no Seek Error exists. On Cylinder is negated on the trailing edge of the Set Cylinder command or on the leading edge of Rezero. On Cylinder status is cleared by any seek instruction including a no motion seek.
	Function: Controller Sends Commands to Drive
Bits 0 - 10 (Bus Lines)	These ten lines carry data to the drive. The meaning of the data is a function of the active tag line.
Tag 1 (Cylinder Select)	This tag line gates the data on the bus out lines to the drive Cylinder Address register. The bus bits have the significance listed below.

RPS - rotational position sensing not used by AMPENIF

Bus Out Bit	Cyl Address Value
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512

Signal	Meaning
Tag 2 (Head Select)	This tag line gates the data on the bus lines to the drive Head Address register and strobes the highest order bit (2^{10}) into the Cylinder Address register. The bus bits have the significance listed below. Note that the bus bit functions are discussed for both the movable and fixed head select operations.

Bus Out Bit	Head Address Value
0	1
1	2
2	4
3	8
4	16
5	not used
6	not used
7	CYL 1024

Tag 3 (Control Select) This signal, when active, allows the bus lines to control operations in a selected drive. The operation performed is dependent upon which of the bus lines is active. The significance of the bus bits is as follows:

Bus Bit	Name Performed	Function Performed
0	Write Gate	With Address Mark Enable (Bus 5) negated, Write Gate enables the write circuitry to transfer the serialized information on the Write Data line to the recording medium. If Address Mark Enable is asserted during Write Gate, the drive records an address mark. While the Write Gate is asserted, the drive faults related to write operations may be detected and signaled via the Fault line on the control ("A") cable. Other than Address Mark Enable, all other combinations of control functions asserted with Write Gate result in undefined action.

Bus Bit	Name Performed	Function Performed
1	Read Gate	With Address Mark Enable negated, Read Gate enables the read circuitry to transfer the serialized information on the Read Data line from the recording medium. If Address Mark Enable is asserted during Read Gate, the drive searches for a previously recorded address mark. All other combinations of control functions asserted with Read Gate result in undefined action.
2	Servo Offset Plus	Not used.
3	Servo Offset Minus	Not used.
4	Fault Clear	This signal clears the Fault status provided no condition remains that activates Fault. Rezero, Release, or both may also be asserted. All other combinations of control functions asserted with Fault Reset result in undefined action.
5	Address Mark Enable	Address Mark Enable writes an address mark when concurrent with Write Gate, or initiates an address mark search when concurrent with Read Gate. The following conditions must also be asserted: Write Gate or Read Gate. All other combinations of control functions asserted with Address Mark Enable result in undefined action.
6	RTZ (Rezero)	This command first causes the head to retract, and then causes the drive to move the positioner to cylinder zero, track zero. It also resets the Head Address register and Seek Error latch. Rezero may be used with Fault Clear or Release; all other combinations of control functions asserted with Rezero result in undefined action.
7	Data Strobe Early	Not used.
8	Data Strobe Late	Not used.
9	Release (Dual Channel Option Only)	Clears device reserved status on the selected interface. (Refer to Unit Selection discussion.) The drive is released by the controller if the controller asserts Control Select and Bus 9 while the drive is selected. The drive remains reserved until Select Enable is negated. Fault Reset, Rezero, or both can also be asserted. All other combinations of control functions asserted with Unit Release result in undefined action.
Tag 4 (Read Current Sector)		This tag gates the current value of the drive's sector counter to the input lines. While Tag 4 is active, all drive statuses except Seek End and Selected are disabled.

Signal	Meaning
	Function: Drive Response to Controller Command
On Cylinder	Described previously
Seek End	This signal indicates either an On Cylinder status or Seek Error status resulting from a seek operation that has terminated.
Fault	When asserted, this line indicates that a fault condition (for example, Read/Write unsafe) has occurred within the drive. The Fault condition disables the Read and Write operations within the drive. This condition also causes negation of Unit Ready (On Cylinder and Seek End remain unaffected). The Fault signal is reset either by a Fault Reset command, or optionally by operator intervention at the drive, provided no condition remains that activates Fault.
Seek Error	When asserted, this status line indicates that the drive failed to complete an initial head load, Set Cylinder, or Rezero command. Seek Error also results when an invalid cylinder address is received by the drive. The Seek Error status may be negated either by a Rezero command from the controller or optionally by operator intervention at the drive.
Address Mark Found	This line indicates drive detection of a previously recorded address mark when Read Gate and Address Mark Enable are both asserted.
	Functions: Read, Write, and Clock
Read Data	This line carries serial data (recovered from disk) synchronized with Read Clock during the assertion of Read Gate. This data is transmitted in NRZ form to the controller.
Read Clock	This signal is developed within the drive. It defines the beginning of a data cell during a Read operation and is used by the controller to strobe Read Data.
Write Data	This line transmits NRZ data from the controller to the drive during Write Gate assertion. The serial write data is strobed with the Write Clock.
Write Clock	This signal is used by the drive to strobe the Write Data line while recording; it defines the beginning of a data cell during a Write operation. Write Clock is generated in the control unit by regenerating the drive's Servo Clock signal.. The Write Clock signal precedes and is transmitted continuously during the assertion of Write Gate.
Servo Clock	This signal is developed within the drives and provides the control unit with a reference clock that synchronizes Write Data to the rotational position of the recording surface during a write operation. The Servo Clock is valid only when Unit Read is asserted.

6.2.4 Arithmetic Logical Unit (ALU) Functions

This section explains the operation and use of the XMCP.

6.2.4.1 2901 Overview

The Am2901 ALU contains the shifting, decoding and multiplexing circuitry which is used by the XMC to perform arithmetic and logic operations. This 4-bit, bit-slice microprocessor contains an internal RAM 16 words deep by 4 bits wide. A cascading technique is used to connect 6 ALUs in order to formulate a 24-bit microprocessor which contains an internal RAM 16 words deep by 24 bits wide.

Since the CPU transmits data in 36-bit-wide segments, the 24-bit microprocessor must transmit data to/from the CPU in only two segments: bits 0 through 23 are transmitted first and then bits 24 through 36 are transmitted. The ALUs are located directly on the XMC board.

The ALU is controlled by a nine-bit microinstruction word which is organized into three groups of three bits each. Each group of three bits selects the ALU source, the ALU function, or the ALU destination registers. With its high speed ALU and 16 working registers, the 2901 is capable of performing 3 arithmetic (ADD, SUBR, and SUBS) and 5 logic (OR, AND, MASK, EXOR, and EXNOR) operations on data being transmitted through the ALU.

Figure 6-6 shows an illustration of the 2901 Microprocessor Block Diagram. A detailed description of the components which comprise the 2901 ALU is provided in the following sections.

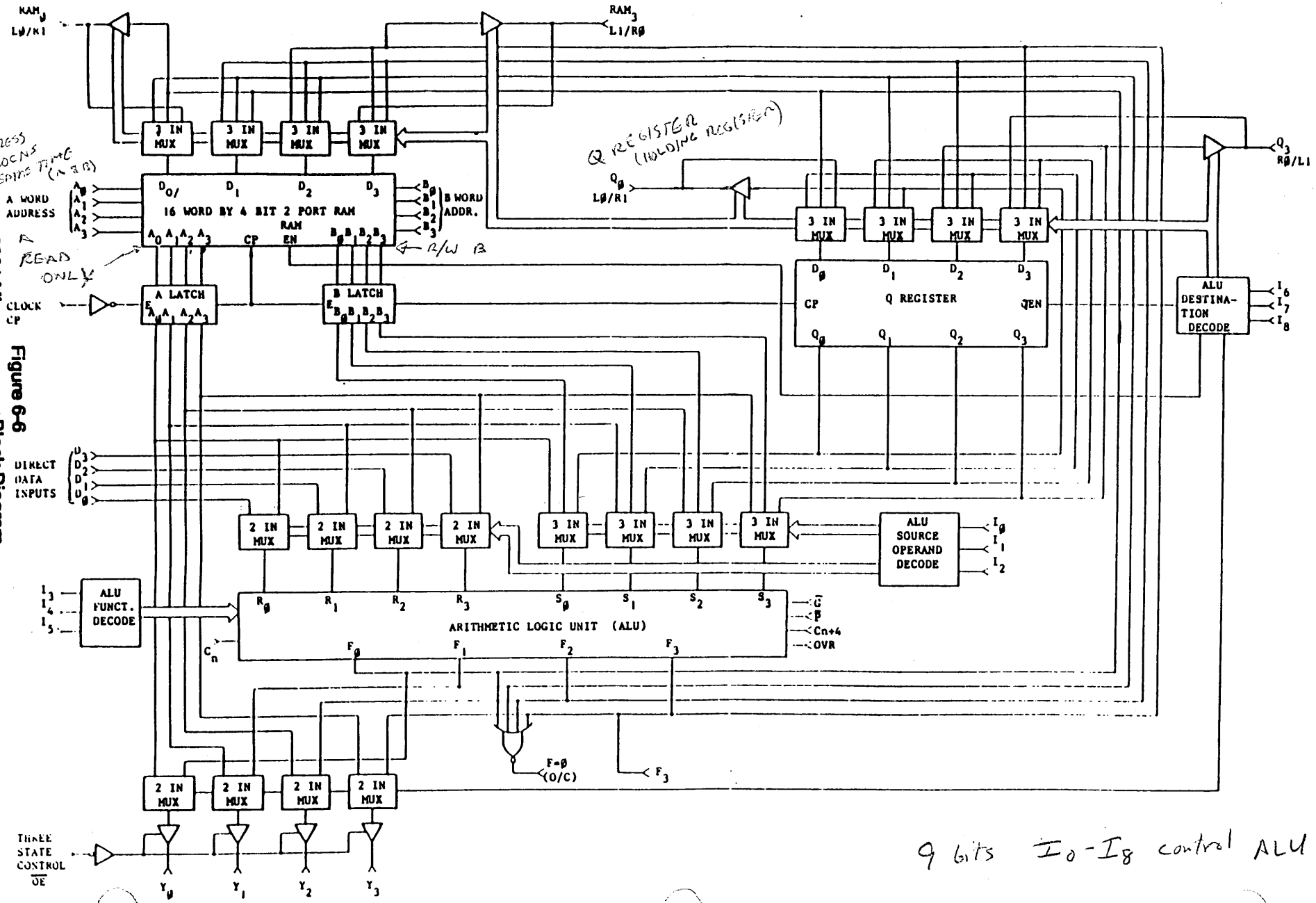


Figure 6-6 2901 Microprocessor Block Diagram

R0 - R15 Registers

In the microcode, the RAM that is located inside the ALU is addressed as R0-R15. These 16 working registers hold values for the ALU functions and are located on a RAM 24-bits-wide by 16-words-deep. (There are 4 bits per RAM and 6 parallel RAMs.)

A and B Ports. The RAM contains two ports, A and B. The A port is addressed by lines A0-A3 and the B port is addressed by lines B0-B3. Figure 6-7 provides a diagram of the A and B ports.

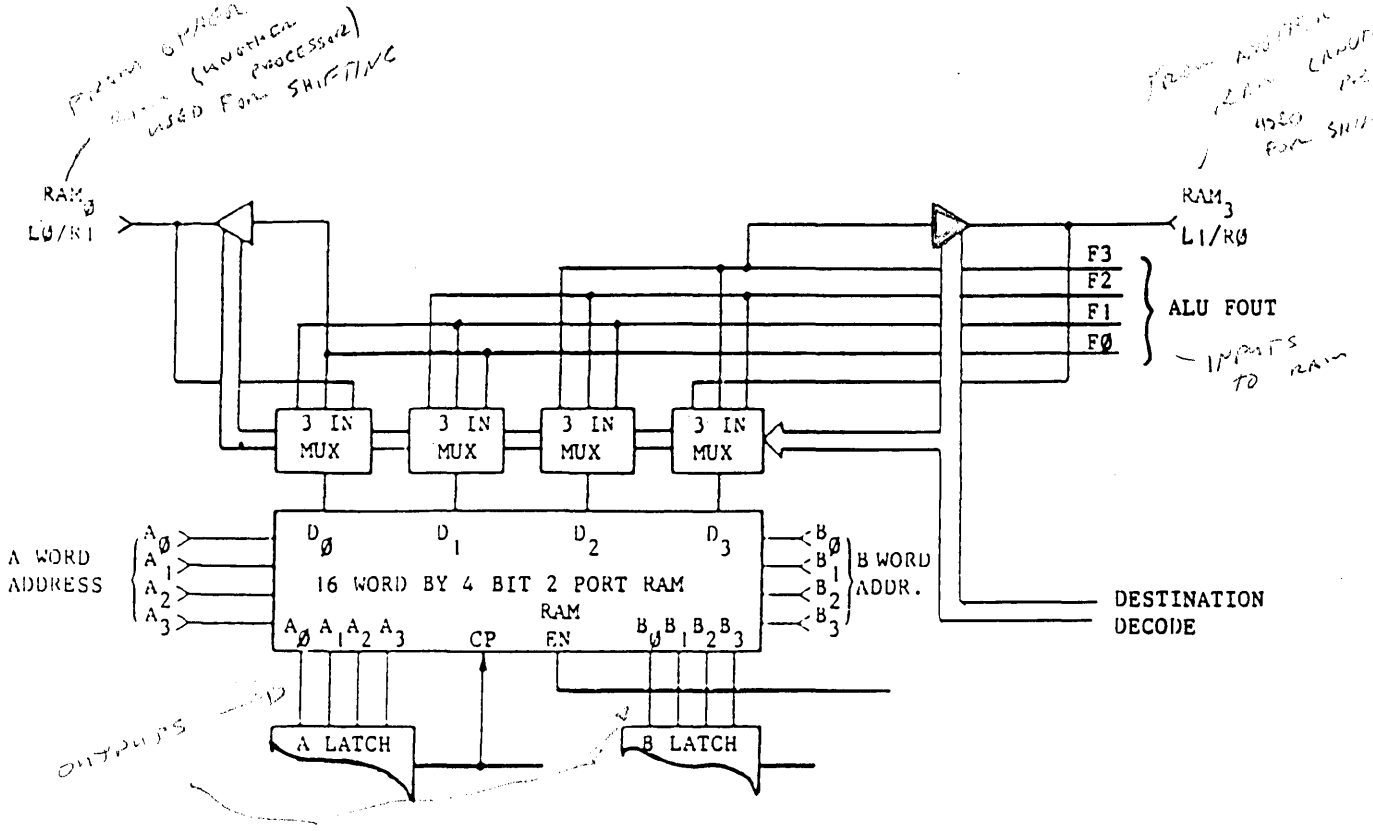


Figure 6-7
A & B Ports

Port A is a **read only port** and is controlled by the four-bit A address field input. Data in any of the 16 words of the RAM can be read from the A port.

Port B is a **read/write port.** Data in any one of the 16 words of the RAM, as defined by the B address field input, can be simultaneously read from the B port of the RAM. In addition, the three-input multiplexer scheme allows data to be shifted up (left) one bit position, down (right) one bit position, or not shifted at all.

The 3 to 1 multiplexer allows for 3 data inputs to the RAM. The center path is straight from the ALU FOUT Lines, F3 to D3, F2 to D2. The two outside paths are used for shifting left and right, F2 from ALU out feeds D1, D2, and D3. Shifting is controlled by the ALU destination decode to enable the correct multiplexer path.

A and B Latches. If both addresses on the A and B address lines are identical, the same memory location data is presented to the A and B output latches, as shown in Figure 6-8.

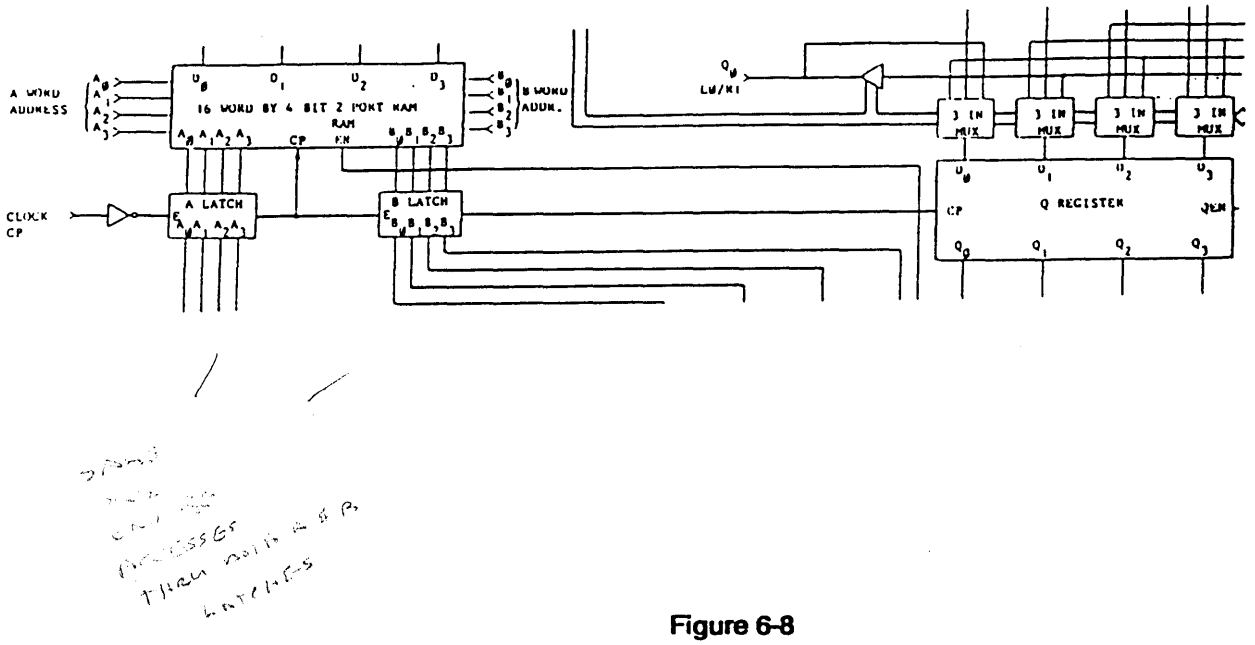


Figure 6-8
A and B Output Latches

New data can only be written to the RAM with write enable to the address specified on the B lines. Both ports have separate 4-bit output latches. These latches hold the RAM data while the clock input is LOW to ensure that new data is written into the RAM without interference.

Clock Input. The clock input to the 2901 controls the RAM, the Q register and the A and B latches, as shown in Figure 6-8 above. When enabled, data is clocked into the Q register on the LOW to HIGH transition clock. When the clock input is LOW, the latches are closed and the last data entered is held in the A or B latch. When the clock input is HIGH, the A and B latches are opened and data is passed to the RAM outputs.

R and S Ports. One word from an address specified by the A lines, and one word from an address on the B lines can be simultaneously presented to the R and S ports of the ALU for an ALU operation. All information coming out of the A port can be fed to the R and S ports of the ALU, while information coming in and out of the B ports can be fed only to the S port of the ALU. Refer to Figure 6-9 for an illustration of the R and S ports.

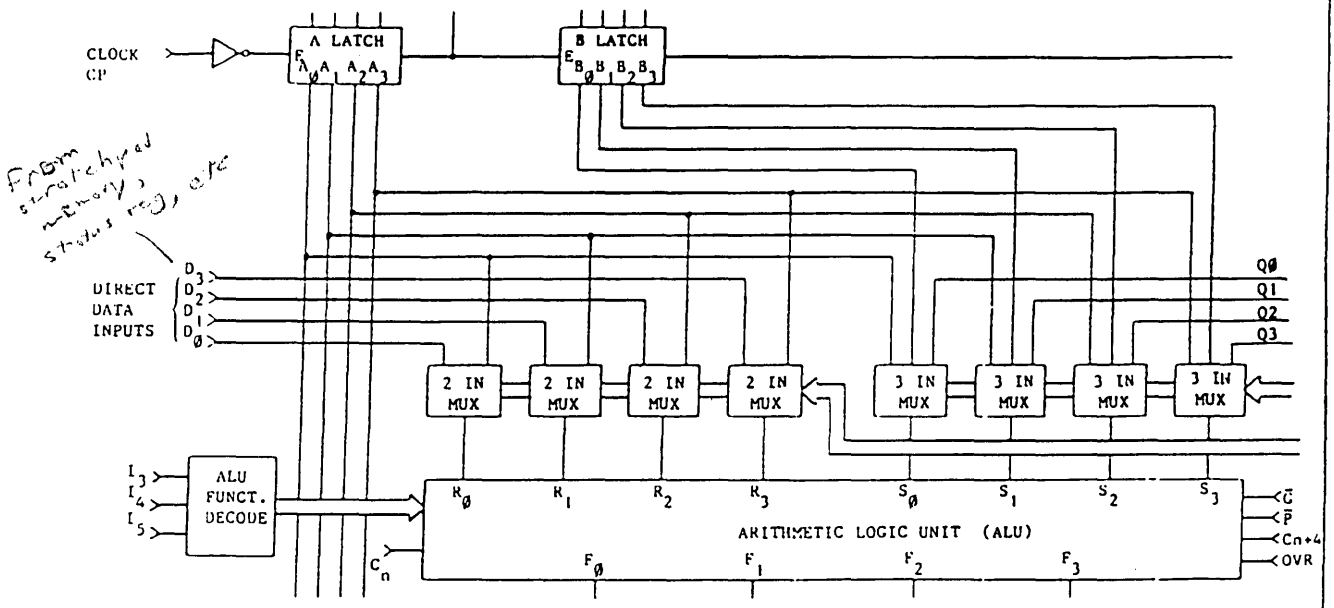


Figure 6-9
R and S Ports

The R input field is driven by a 2-input multiplexer and the S input field is driven by a 3-input multiplexer. Both multiplexers have an inhibit capability which prohibits data from being passed (equivalent to "zero" source operand).

The multiplexer feeding the R port of the ALU has two input sources:

1. direct data input which is four bits wide (D0-D3) coming into the ALU from the host system (i.e., status registers, SMB RAM, etc.), and
2. outputs of the A latch.

The multiplexer feeding the S port of the ALU has three input sources:

1. outputs of the A latch,
2. outputs of the B latch, and
3. outputs of the Q Register.

Q Register

The Q Register is a separate 4-bit field used primarily as a holding or temporary register. This register is driven from a 3-input multiplexer, which feeds data from the ALU output lines or the Q output lines. If data is fed from the Q outputs, the input multiplexers can be selected to allow shifting, under control of the ALU Destination Decode. Figure 6-10 below illustrates the Q Register input and output lines.

In no shift mode, the multiplexer enters the ALU data into the Q register. In shift-up or shift-down mode, the multiplexer selects the Q register data and shifts data up or down accordingly. The Q shifter has two ports and is controlled from I6, I7, and I8 microinstruction inputs (ALU Destination Code); its operation is similar to the RAM shifter described in the previous section.

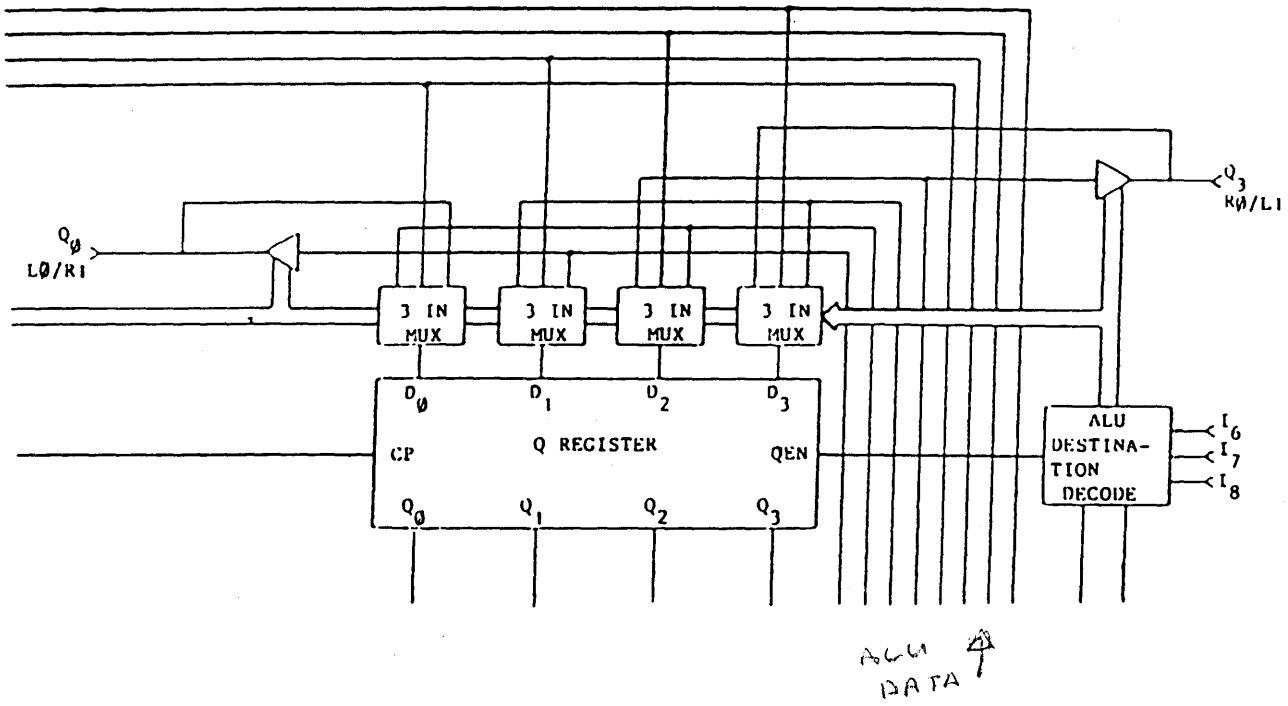


Figure 6-10
Q Register

Source Operand Decode

The Source Operand Decode defines the source of the R and S inputs into the ALU per the table in Figure 6-11. This 3-bit microinstruction word provides the ALU with the source of the R and S inputs required to perform an ALU operation. The input multiplexers also have an inhibit feature which is equal to a zero source.

	MICROCODE				ALU SOURCE OPERANDS	
MNEMONIC	I2	I1	I0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 6-11
ALU Source Operand Control

Function Decode

The ALU can perform three arithmetic (ADD, SUBR, SUBS) and five logic (OR, AND, MASK, EXOR, EXNOR) functions as defined in Figure 6-12 below. This 3-bit microinstruction word indicates to the ALU the type of function which will be performed on the data received.

	Microcode					
Mnemonic	I5	I4	I3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R+S
SUBR	L	L	H	1	S Minus R	S - R
SUBS	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R∨S
AND	H	L	L	4	$\underline{R}$ AND S	$\underline{R}$∧S
MASK	H	L	H	5	R AND S	R∧S
EXOR	H	H	L	6	R EX-OR S	$\underline{R \veebar S}$
EXNOR	H	H	H	7	R EX-NOR S	R⊻S

Figure 6-12
ALU Function Control

Destination Decode

The destination decode lines determine where the result of the ALU function is placed after the operation has been performed. Lines F0-F3 of the ALU are stored according to the table in Figure 6-13.

	MICROCODE				RAM FUNCTION		Q-REG. FUNCTION		Y	RAM SHIFTER		Q SHIFTER	
Mnemonic	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load	Output	RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
FAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

Figure 6-13
ALU Destination Control

Summary of Table in Figure 6-13

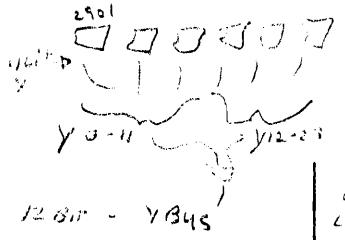
Octal Code	Mnemonic	Result
0	QREG	Load F word to Q register
1	NOP	Used for FoutL, FoutU control
2	RAMA	A latch to Y, and F word to B
3	RAMF	Load F word to B register
4	RAMQD	Load F/2 to B register, Q/2 to Q register--shift right
5	RAMD	Load F/2 to B register--shift right
6	RAMQU	Load 2F to B register, 2Q to Q register--shift left
7	RAMU	Load 2F to B register--shift left

Status Signals of the ALU

Code	Description
F=0	Indicates the result of an ALU operation was equal to zero.
F3	Is MSB out of ALU
CN	Is Carry-in
$\overline{G}$	Carry Lookahead Generator
$\overline{P}$	Carry Lookahead Generator
CN+4	Is Carry-out
OVR	Is Overflow

NOTE: Since the ALU is 24 bits wide and the ALU Y Bus is only 12 bits wide, the output enable lines control which 12 bits are output (upper or lower).

Output Enable Lower (OEL) bits 0-11
Output Enable Upper (OEU) bits 12-23

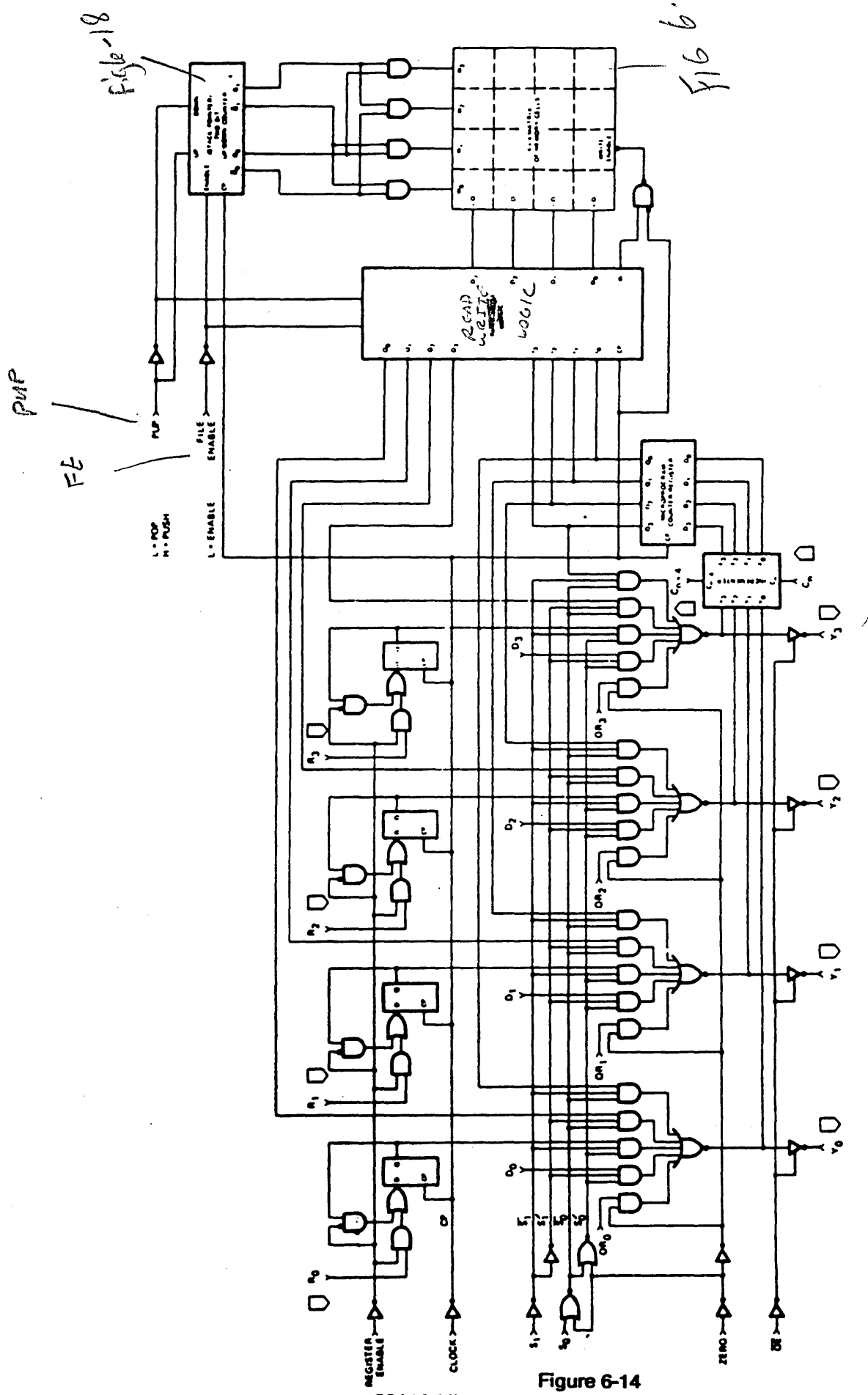


6.2.4.2 2911A Overview

The 2911A is a cascadable, 4-bit microprocessor sequencer which supplies the address location to the microprogram. Four 2911As are cascaded to create a 16-bit address controller that allows addressing of up to 12K words of microprogram. The 2911A sequencer addresses one microinstruction word per instruction cycle and is capable of addressing a 40-bit wide microinstruction word.

Since the 2911A is not deep enough to hold the circuitry for the push/pop stack, the address controller and the microprogram are located on the XM16K PROM board (see section 6.3). The sequencer addresses the PROM board using 16 address locations.

The 2911A Microprogram Sequencer Block Diagram is shown in Figure 6-14. The components of the 2911A Sequencer are described in the following sections.



Note: R_i and D_i connected together on Am2911A and OR_i removed.

Figure 6-14
2911A Microprogram Sequencer Block Diagram

S0 and S1 Inputs

Controlled by the S0 and S1 inputs, the 2911A contains a 4-input multiplexer which selects either the address register, direct inputs, microprogram counter, or the push/pop stack as shown in Figure 6-15 below.

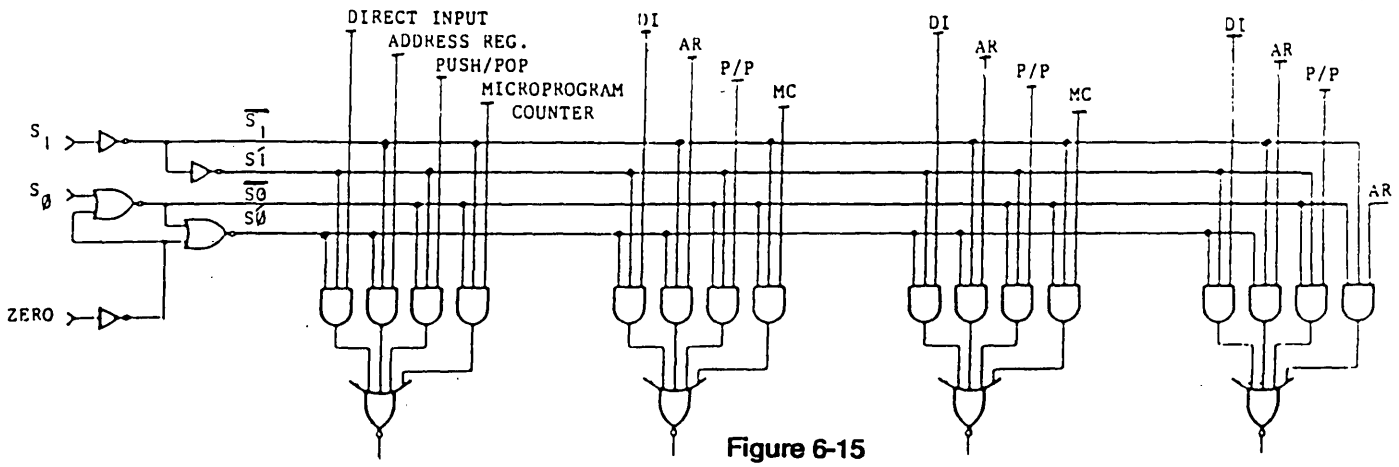


Figure 6-15
S0 and S1 Inputs

Address Register — internal to the 2911

The address register indicates the source of the next microinstruction address. The 2911A has one address register which contains a common clock enable. When an address register enable is low, new data is entered into the register on the clock LOW to HIGH transition. The address register is used to store one microprogram address which is to be returned to some time later in the execution of the microprogram. There are four flip-flops (labelled R0-R3) which make up a 16-bit wide by 1 deep address register. Figure 6-16 below provides an illustration of the address register.

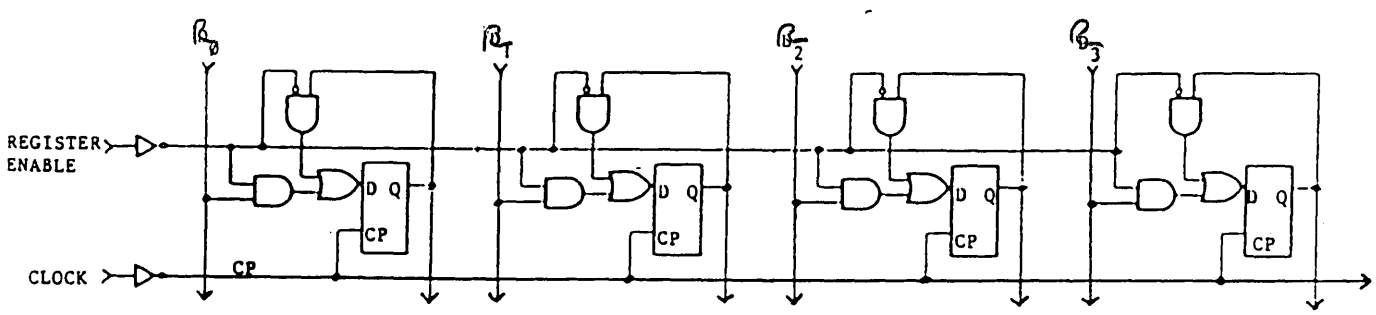


Figure 6-16
Address Registers

Direct Inputs

The direct input is a 4-bit field of inputs to the multiplexer which can be selected as the next microinstruction address, as illustrated in Figure 6-15. These inputs may also be used as inputs to the register, thus allowing an N-way branch (where N is any word in the microcode).

Microprogram Counter Register and Incrementer

The 2911A contains a microprogram counter composed of a 4-bit incrementer followed by a 4-bit register, as shown in Figure 6-17 below. The incrementer has a carry-in (Cn) and carry-out (Cn+4) to make cascading to larger words straightforward.

The outputs of the 4 input OR gates (Y0-3) feed the incrementer. By controlling the carry-in = 0 or 1, either the current address or the current address + 1 is presented to the microprogram counter to serve as the next address source. All decoding of OR gate outputs is performed on the 16-word deep external push/pop stack located on the XM16KP board. Although this is performed differently than in an internal push/pop stack, the result is the same as that which is shown in Figures 6-18 and 6-19.

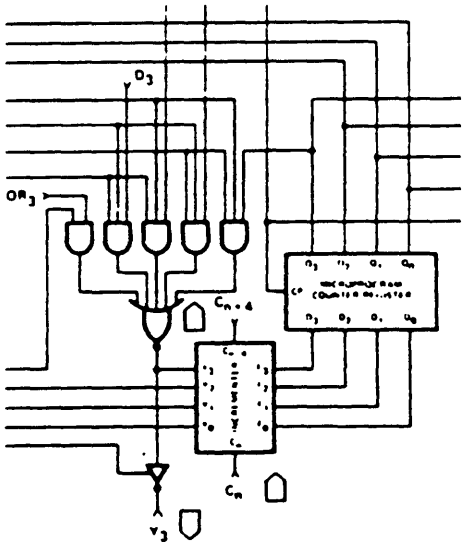


Figure 6-17
Incrementer and Microprogram Counter Register

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	µPC
1	L	H	Address register	AR
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

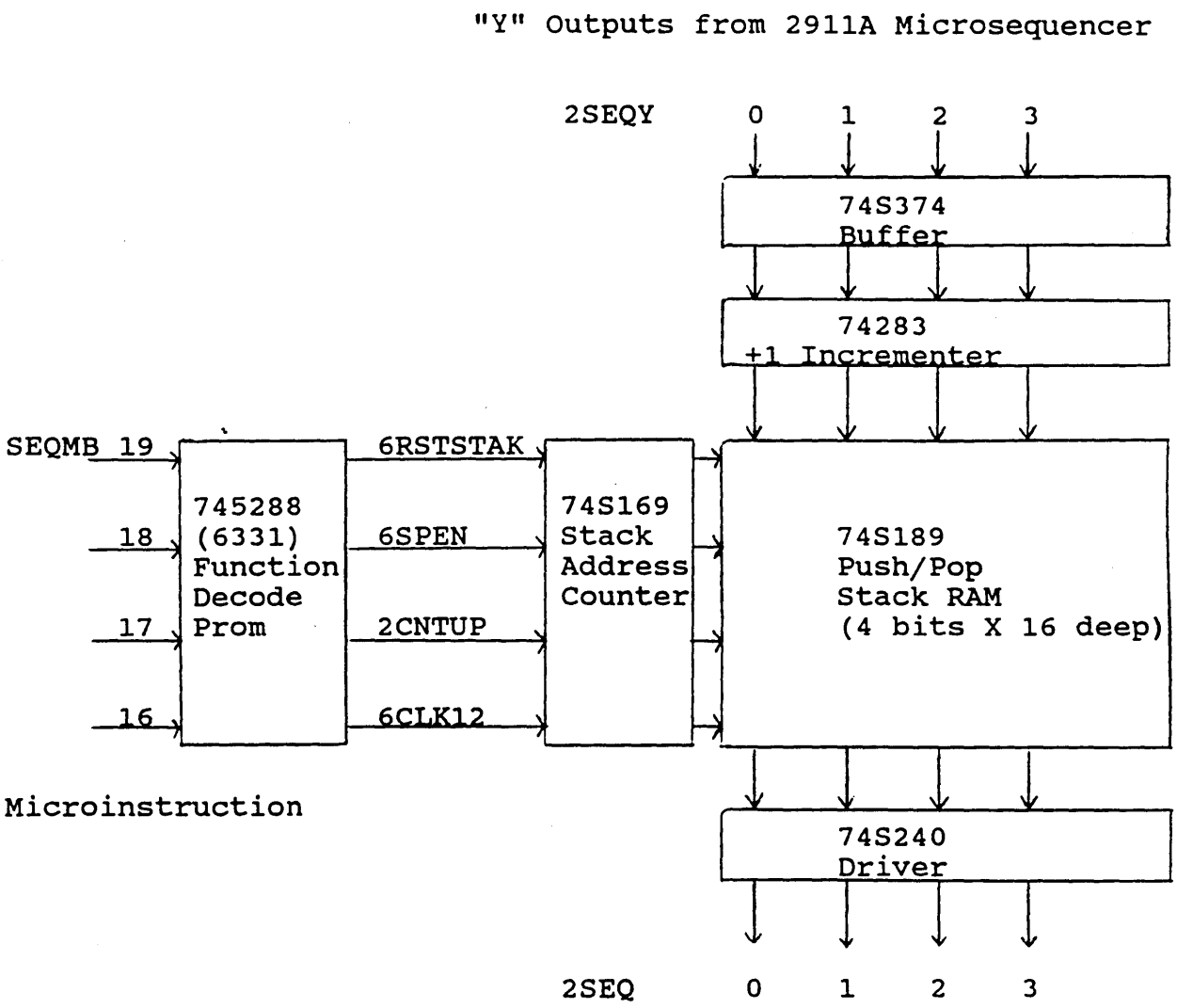
Figure 6-18

PUSH POP STACK COMMANDS — USED ONLY FOR RETURN ADDRESS — NOT REGISTERS

CYCLE	S_1, S_0, $\overline{FE}$, PUP	µPC	AR	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N N+1	0 0 0 0 –	J J+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	J –	Push µPC	Set-up Loop
N N+1	0 0 1 X –	J J+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	K –	Push µPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J Ra+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	Ra –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J Ra+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	Ra –	Jump to Address in STK0; Push µPC	
N N+1	1 0 1 X –	J Ra+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	Ra –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	Ra Rb	Rb Rc	Rc Rd	Rd Ra	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	Ra J	Rb Ra	Rc Rb	Rd Rc	D –	Jump to Address on D; Push µPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	Ra Ra	Rb Rb	Rc Rc	Rd Rd	D –	Jump to Address on D	JMP D

X = Don't Care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH

Figure 6-19



(Actual Stack is on the XM16KP Board)

Figure 6-19A
Push/Pop Stack Block Diagram
(4-bit slice)

USED FOR RETURN ADDRESSES ONLY.

Push/Pop Stack RAM

The Push/Pop Stack is comprised of four 74S189 RAM devices mounted on the XM16KP board. They are arranged to assemble a 16-bit wide by 16-location deep Stack. (The upper 2 bits are not used.) Figure 6-20 illustrates a single 74S189 device. The Stack is used to store the Return Microsequencer Address (14 bits wide) plus one on a Push Stack command. On a Pop Stack command, the return microsequencer address plus one will be retrieved.

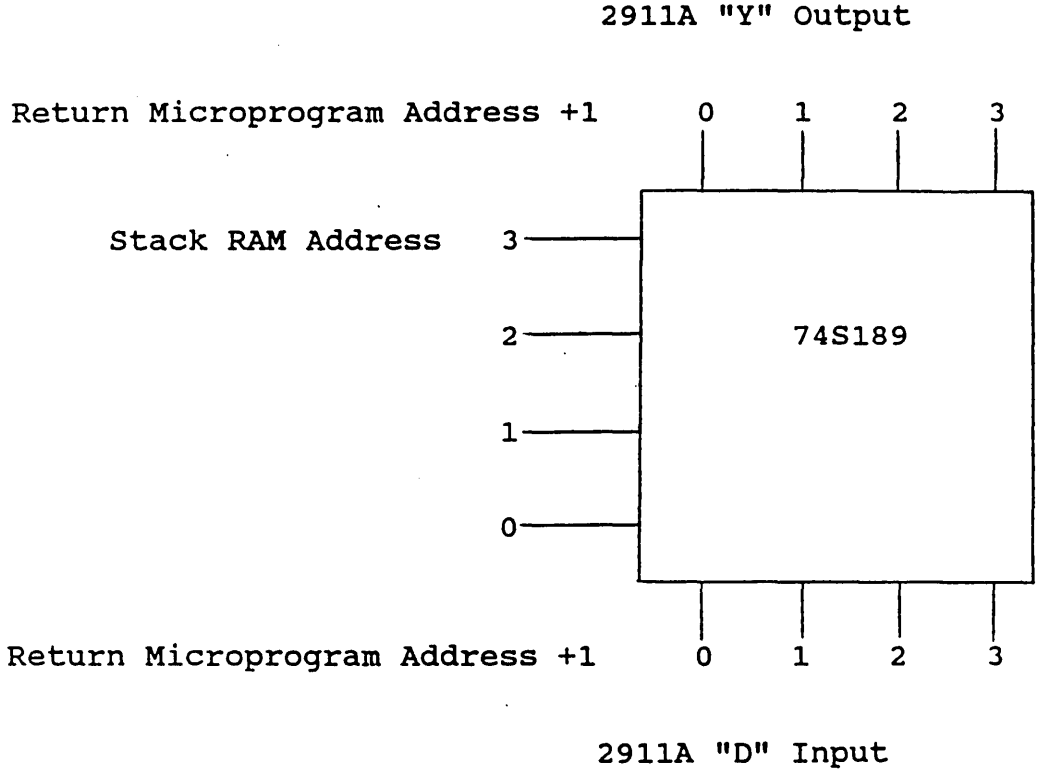


Figure 6-20
Push/Pop Stack RAM

Push/Pop Stack Controller

The Push/Pop Stack Controller, illustrated in Figure 6-21, controls the operation of the Stack RAM. A Push Stack command on microinstruction bits 19-16 causes a 74S288 (6331) function decode PROM to generate an increment sequence to the 74S169 Stack RAM Address Counter, which increments the RAM memory. At this time, the Microinstruction Program Address plus one is stored into that memory location.

On a Pop Stack command, the function decode PROM will decode a decrement command to the Stack RAM Address Counter, causing the Microinstruction Program Address plus one to be retrieved.

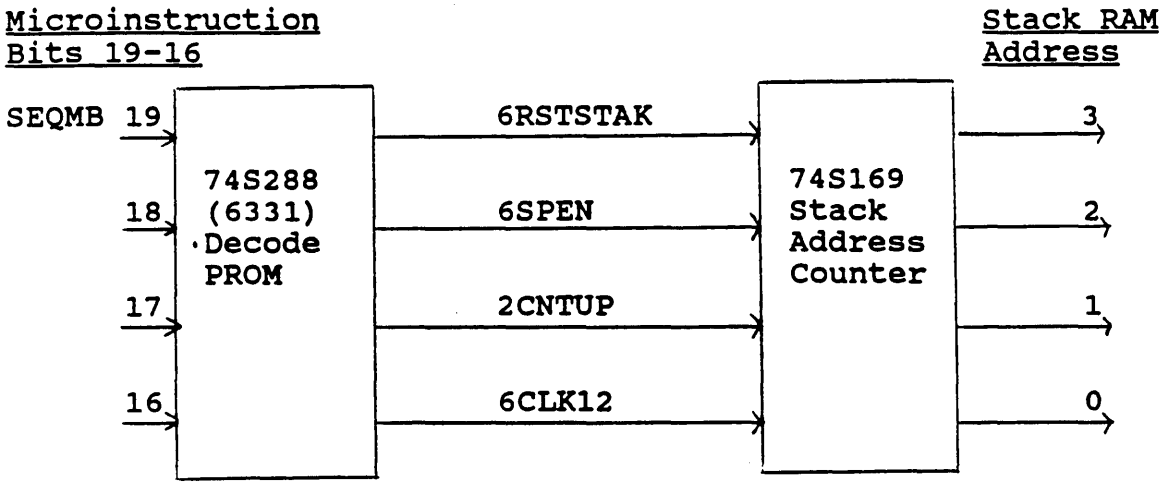


Figure 6-21
Push/Pop Stack Controller

Push/Pop Stack Incrementer

The Push/Pop Stack Incrementer is a 74283, as shown in Figure 6-21A. It is used to increment the Return Microsequencer Program Address by one. This Address is then stored in the 74S189 Stack RAM on a Push Stack command.

On a Pop Stack command, the Return Microsequencer Program Address is retrieved. The increment by one counter allows the Microprogram to return from a subroutine to the correct Microprogram Address. Four of these devices are used to assemble a complete incrementer.

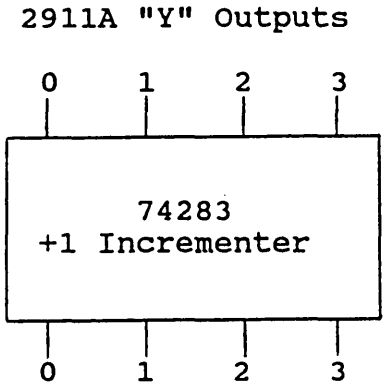


Figure 6-21A
Push/Pop Stack Incrementer

Y Outputs

The 2911A features three-state Y outputs which provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control PROM. Figure 6-22 shows the location of the Y outputs.

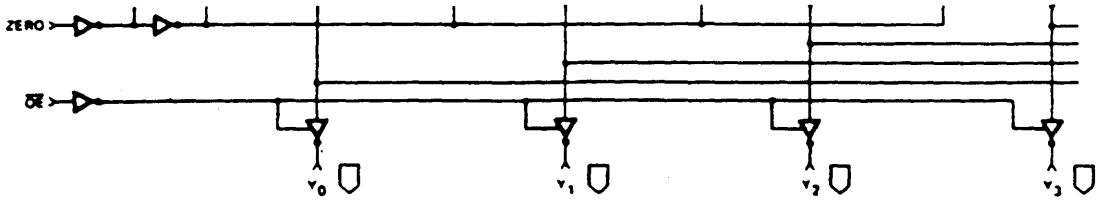


Figure 6-22
Y Outputs

Zero Input

The ZERO input is used to force the four outputs to a binary zero state, as shown in Figure 6-22. When ZERO input is LOW all outputs are LOW regardless of any other inputs. Each Y output bit also has a separate OR input so that conditional logic can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

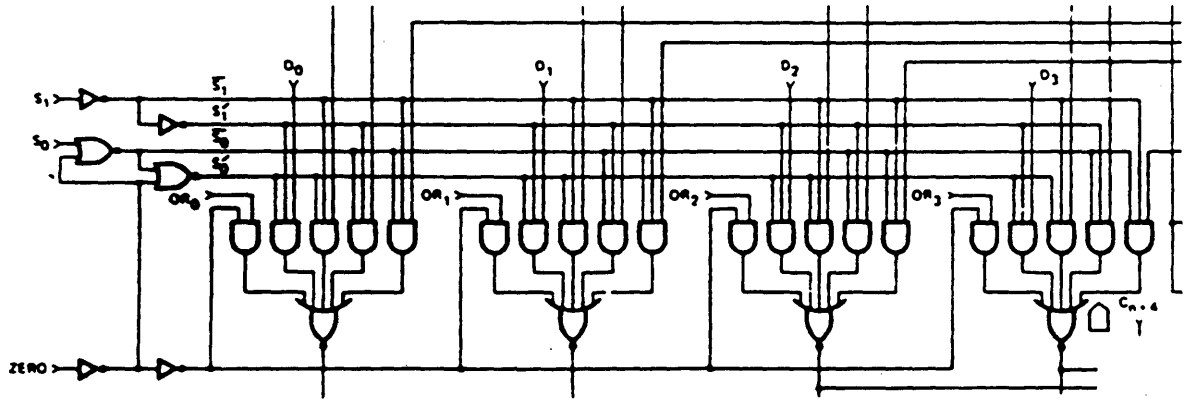


Figure 6-23
Zero Input

6.2.5 Internal and External Operations

The XMC and the microcode work in conjunction with each other and are considered the "brain" of the controller. The XMC is the board which controls all the other boards in the controller and the microcode is the software which drives the hardware. In effect, the microcode tells the hardware which operations are to be performed via the XMC circuit board.

The microcode consists of a 40-bit-wide microinstruction word. Depending upon the data in the microcode, the microinstruction word sets up the hardware to perform a particular operation; instructs the controller as to which part of the operation is to be performed first; and based on that result, indicates what needs to be done next. Figure 6-24 provides a breakdown of the 40-bit microinstruction word which is read by the XMC.

The microinstruction word is divided into two 20-bit-wide sections for easier manipulation of data. Bit 39 determines whether an operation is to be performed internally (within the ALU/XMC) or externally (on specific logic boards). If bit 39 is not active, bits 20-38 control the internal operations within the ALU/XMC. If bit 39 is active, bits 20-38 control the external logic boards which are to be accessed by the XMC. When bit 39 is active, bits 20-35 are also referred to as Instruction Bus Bits 0-15. Bits 00-19 define the next instruction in the microprogram which is to be executed.

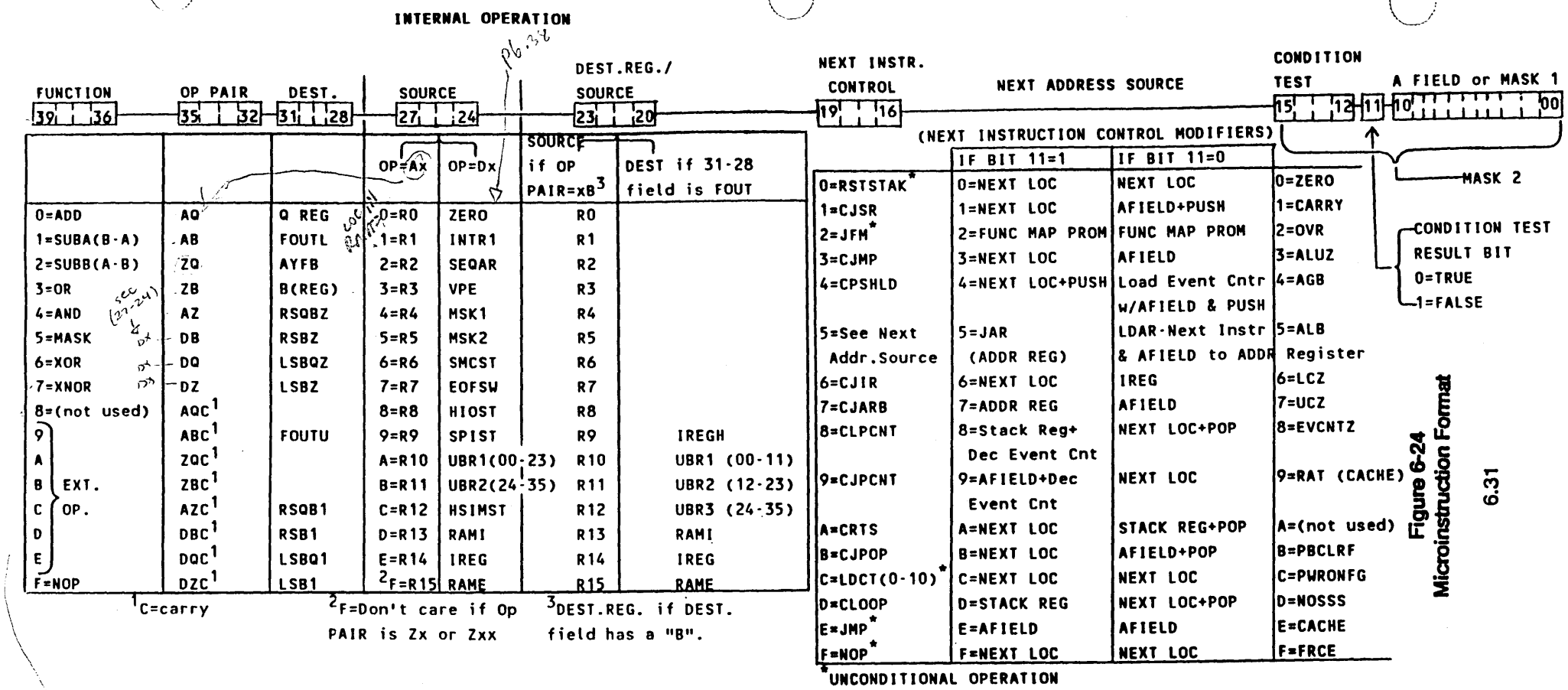
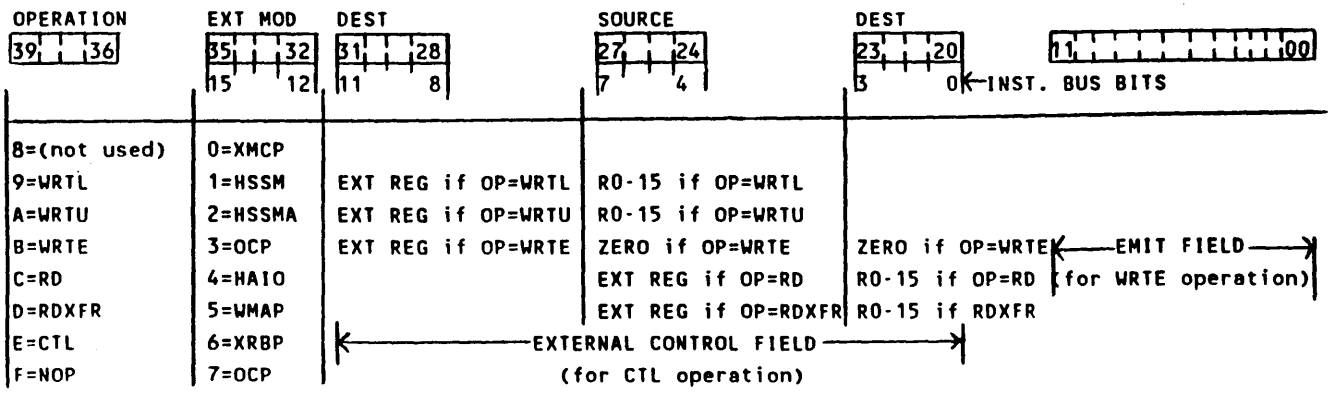
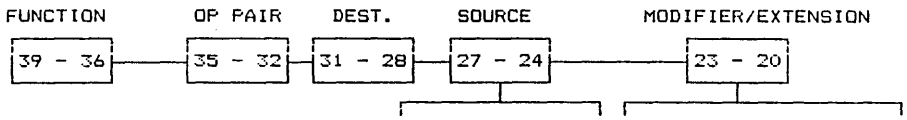

INTERNAL OPERATION
FUNCTION
OP PAIR
DEST.
SOURCE
DEST.REG./ SOURCE
NEXT INSTR. CONTROL
NEXT ADDRESS SOURCE
CONDITION TEST
A FIELD or MASK 1
39 36 35 32 31 28 27 24 23 20 19 16 15 12 11 10 00
(NEXT INSTRUCTION CONTROL MODIFIERS)
OP=Ax
OP=Dx
SOURCE if OP PAIR=xB3
DEST if 31-28 field is FOUT
IF BIT 11=1
IF BIT 11=0
MASK 2
CONDITION TEST RESULT BIT 0=TRUE 1=FALSE
0=ADD AQ 0=R0 ZERO R0
1=SUBA(B-A) AB FOUTL 1=R1 INTR1 R1
2=SUBB(A-B) ZQ AYFB 2=R2 SEQAR R2
3=OR ZB B(REG) 3=R3 VPE R3
4=AND AZ RSQBZ 4=R4 MSK1 R4
5=MASK DB RSBZ 5=R5 MSK2 R5
6=XOR DQ LSBQZ 6=R6 SMCST R6
7=XNOR DZ LSBZ 7=R7 EOFSW R7
8=(not used) AQC1 8=R8 HIOST R8
9 ABC1 FOUTU 9=R9 SPIST R9 IREGH
A ZQC1 A=R10 UBR1(00-23) R10 UBR1 (00-11)
B EXT. ZBC1 B=R11 UBR2(24-35) R11 UBR2 (12-23)
C OP. AZC1 RSQB1 C=R12 HSIMST R12 UBR3 (24-35)
D DBC1 RSB1 D=R13 RAMI R13 RAMI
E DQC1 LSBQ1 E=R14 IREG R14 IREG
F=NOP DZC1 LSB1 2F=R15 RAME R15 RAME
0=RSTSTAK* 0=NEXT LOC NEXT LOC 0=ZERO
1=CJSR 1=NEXT LOC AFIELD+PUSH 1=CARRY
2=JFM* 2=FUNC MAP PROM FUNC MAP PROM 2=OVR
3=CJMP 3=NEXT LOC AFIELD 3=ALUZ
4=CPSHLD 4=NEXT LOC+PUSH Load Event Cntr w/AFIELD & PUSH 4=AGB
5=See Next Addr.Source 5=JAR (ADDR REG) LDAR-Next Instr & AFIELD to ADDR Register 5=ALB
6=CJIR 6=NEXT LOC IREG 6=LCZ
7=CJARB 7=ADDR REG AFIELD 7=UCZ
8=CLPCNT 8=Stack Reg+ Dec Event Cnt NEXT LOC+POP 8=EVCNTZ
9=CJPCNT 9=AFIELD+Dec Event Cnt NEXT LOC 9=RAT (CACHE)
A=CRTS A=NEXT LOC STACK REG+POP A=(not used)
B=CJPOP B=NEXT LOC AFIELD+POP B=PBCLRF
C=LDCT(0-10)* C=NEXT LOC NEXT LOC C=PWRONFG
D=CLOOP D=STACK REG NEXT LOC+POP D=NOSSS
E=JMP* E=AFIELD AFIELD E=CACHE
F=NOP* F=NEXT LOC NEXT LOC F=FRCE
1C=carry
2F=Don't care if Op PAIR is Zx or Zxx
3DEST.REG. if DEST. field has a "B".
*UNCONDITIONAL OPERATION

Figure 6-24 Microinstruction Format


EXTERNAL OPERATION
OPERATION
EXT MOD
DEST
SOURCE
DEST
INST. BUS BITS
39 36 35 32 31 28 27 24 23 20 11 00
15 12 11 8 7 4 3 0
8=(not used) 0=XMCP
9=WRTL 1=HSSM EXT REG if OP=WRTL R0-15 if OP=WRTL
A=WRTU 2=HSSMA EXT REG if OP=WRTU R0-15 if OP=WRTU
B=WRTE 3=OCP EXT REG if OP=WRTE ZERO if OP=WRTE ZERO if OP=WRTE EMIT FIELD (for WRTE operation)
C=RD 4=HAIO EXT REG if OP=RD R0-15 if OP=RD
D=RDXFR 5=WMAP EXT REG if OP=RDXFR R0-15 if RDXFR
E=CTL 6=XRBP EXTERNAL CONTROL FIELD (for CTL operation)
F=NOP 7=OCP

INTERNAL OPERATIONS:



			OP=Ax	OP = Dx	SOURCE OR DEST IF OP PAIR = xB	DEST IF 31 - 28 IS FOUT
0=ADD	AQ	Q REG	0=R0	ZERO	R0	
1=SUBA(B-A)	AB	FOUTL	1=R1	INTR1	R1	
2=SUBB(A-B)	ZQ	AYFB	2=R2	SEQAR	R2	
3=OR	ZB	B(REG)	3=R3	VPE	R3	
4=AND	AZ	RSQBZ	4=R4	MSK1	R4	
5=MASK	DB	RSBZ	5=R5	MSK2	R5	
6=XOR	DQ	LSQBZ	6=R6	SMCST	R6	
7=XNOR	DZ	LSBZ	7=R7	EOFSW	R7	
8=(NOT USED)	AQC(C=CARRY)		8=R8	HIOST	R8	
9	ABC "	FOUTU	9=R9	SPIST	R9	IREGH
A EXT.	ZQC "		A=R10	UBR1(00-23)	R10	UBR1(00-11)
B	ZBC "		B=R11	UBR2(24-35)	R11	UBR2(12-23)
C OP.	AZC "	RSQB1	C=R12	HSIMST	R12	UBR3(24-35)
D	DBC "	RSB1	D=R13	RAMI	R13	RAMI
E	DQC "	LSQB1	E=R14	IREG	R14	IREG
F=NOP	DZC "	LSB1	F=R15*	RAME	R15	RAME

* F=DON'T CARE IF OP PAIR IS Zx OR Zxx

FUNCTION DECODE (BITS 36 - 39):

MNEMONIC	MICROCODE I2	I1	I0	OCTAL CODE	ALU FUNCTION	SYMBOL
ADD	L	L	L	0	R PLUS S	R + S
SUBA(B-A)	L	L	H	1	S MINUS R	S - R
SUBB(A-B)	L	H	L	2	R MINUS S	R - S
OR	L	H	H	3	R OR S	R v S
AND	H	L	L	4	R AND S	R ^ S
MASK	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ^ S
XOR	H	H	L	6	R EX-OR S	R ⊻ S
XNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

OP PAIR (BITS 32 - 35):

HEX CODE	MNEMONIC	DESCRIPTION
0	AQ	IF LINE A IS DEFINED AS ONE OF THE PAIRS, USE BITS 24 - 27 TO DETERMINE THE ADDRESS OF THE A REGISTER (BITS 24-27 THEN CORRESPOND TO ADDRESS LINES A0 - A3 OF THE ALU)
1	AB	IF LINE B IS SPECIFIED AS AN OP PAIR, USE BITS 20 - 23 TO DETERMINE THE ADDRESS OF THE B REGISTER (BITS 20-23 CORRESPOND TO ADDRESS LINES B0 - B3 OF THE ALU)
2	ZQ	OP PAIR IS 0 AND Q REGISTER
3	ZB	OP PAIR IS 0 AND B REGISTER
4	AZ	OP PAIR IS A (SPECIFIED BY BITS 24-27) AND 0
5	DB	IF D IS SPECIFIED AS ONE OF THE OP PAIRS USE BITS 24-27 TO DETERMINE WHICH EXTERNAL REGISTERS WILL UNLOAD THE D INPUTS
6	DQ	DIRECT INPUT AS SPECIFIED BY BITS 24-27 & Q REG
7	DZ	DIRECT INPUT AS SPECIFIED BY BITS 24-27 AND 0
8 - F		THESE OP PAIRS ARE IDENTICAL TO 0 - 7 WITH THE ADDITION OF A CARRY WHICH IS EQUAL TO 1. IF BIT 35 IS A 1 (HIGH) IT WILL SET 2 ALUCN.

DESTINATION DECODE (BITS 28 - 31):

HEX CODE	MNEMONIC	DESCRIPTION
0	Q REG	
1	FOUTL	ENABLE LOWER 12 BITS ONTO ALU Y LINES. THE DESTINATION IS DEFINED WITH BITS 20-23
2	AYFB	ACCOMPLISHES 2 FUNCTIONS: 1) LOADS THE CONTENTS OF THE Rx AS ADDRESSED BY THE A FIELD (A0-A3) TO THE ALU Y BUS AND 2) LOADS THE ALU F BUS TO THE Rx AS SPECIFIED BY B FIELD (B0-B3). Rx = R0-R15
3	B REG	WRITES TO Rx AS ADDRESSED BY THE B FIELD BITS 20-23
4	RSQBZ	RIGHT SHIFT THE F WORD WITH A 0 AND STORE IT IN B AND Q REGISTERS 1) F/2 -> B WITH Q0 2) Q/2 -> Q WITH A "0" INTO Q23

HEX CODE	MNEMONIC	DESCRIPTION
5	RSBZ	RIGHT SHIFT F WORD WITH A 0, BUT ONLY LOAD TO B (NOT Q) REGISTER
6	LSBQZ	LEFT SHIFT THE F WORD WITH 0 AND LOAD TO B & Q REGS 1) 2F -> B WITH A "0" 2) 2Q -> Q WITH B23
7	LSBZ	LEFT SHIFT F WORD WITH 0, ONLY LOAD TO B REG
8		NOT DEFINED
9	FOUTU	LOAD UPPER ALU BITS 12-23 TO THE Y BUS AND WRITE TO AN EXTERNAL REGISTER SPECIFIED BY BITS 20-23
A		NOT DEFINED
B		NOT DEFINED
C	RSQB1	RIGHT SHIFT WITH A 1 LOAD TO Q AND B REGISTERS 1) F/2 -> B WITH Qo 2) Q/2 -> WITH A "1" INTO Q23
D	RSB1	RIGHT SHIFT WITH A 1 LOAD TO B REGISTER
E	LSBQ1	LEFT SHIFT WITH A 1 LOAD TO Q AND B REGISTERS 1) 2F -> B WITH A "1" INTO Bo 2) 2Q -> Q WITH B23
F	LSB1	LEFT SHIFT WITH A 1 LOAD TO B REGISTER

SOURCE DECODE (BITS 24 - 27):

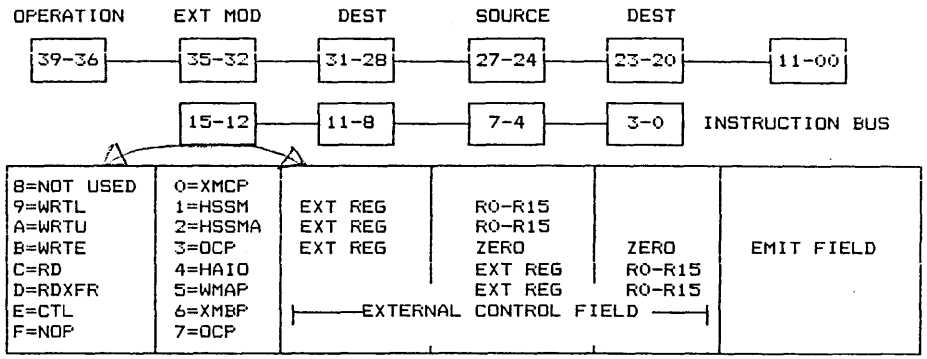
HEX CODE	MNEMONIC	DESCRIPTION
0	ZERO	
1	INTR1	INTERRUPT REGISTER, PAGE 19 EL1 EL2
2	SEQAR	SEQUENCE ADDRESS REGISTER, PAGE 10 BD3 BD2
3	VPE	VECTOR PRIORITY ENCODER, PAGE 6 DF4 DH4
4	MSK1	MASK 1 FIELD 2MINST 00-10, PAGE 14 BF1 BF2
5	MSK2	MASK 2 FIELD 2MINST 00-15, PAGE 14 BF1 BF2 BF3
6	SMCST	XMC STATUS REGISTER, PAGE 19 AF5 AD4
7	EOFSW	OPTION JUMPER REGISTER, PAGE 18 BB5 EM3
8	HIOST	HAIO STATUS REGISTER, PAGE 18 BH2 BH3
9	SPIST	SPI STATUS REGISTER, PAGE 19 BH4
A	UBR1	U BUS REGISTER BITS 00-23, PAGE 1
B	UBR2	U BUS REGISTER BITS 24-35, PAGE 1
C	HSIMST	PAGE 23 BH5
D	RAMI	SMB RAM (SCRATCHPAD RAM) AS ADDRESSED BY THE I REGISTER, PAGE 6 & PAGE 30 DH5 DK5
E	IREG	I REGISTER THRU THE MOVE GATE, PAGE 6 DD4 DF2
F	RAME	SMB RAM AS ADDRESSED BY THE ~~EMIT~~ A FIELD 2MINST 00-09, PAGE 30

MODIFIER/EXTENSION DECODE (BITS 20 - 23):

BITS 20-23 FURTHER DEFINE THE DESTINATION (BITS 28-31) OR THE SOURCE (BITS 24-27) INPUT FIELDS. IF THE DESTINATION FIELD IS FOUT OR B, BITS 20-23 SHOW THE OUTPUT OF THE RESULT. IF THE SOURCE FIELD IS B, BITS 20-23 FURTHER DEFINE THE REGISTER PER THE TABLE BELOW.

HEX CODE	MNEMONIC	DESCRIPTION
9	IREGH	IREG BITS 12 & 13, PAGE 10A FH3
A	UBR1	U BUS REGISTER BITS 00-11, PAGE 4
B	UBR2	U BUS REGISTER BITS 12-23, PAGE 4
C	UBR3	U BUS REGISTER BITS 24-35, PAGE 4
D	RAMI	SMB RAM AS ADDRESSED BY THE IREG, PAGE 30
E	IREG	, PAGE 6 DK5 DH5
F	RAME	SMB RAM AS ADDRESSED BY THE EMIT FIELD, PAGE 30

EXTERNAL OPERATIONS:



OPERATION (BITS 36 - 39):

HEX CODE	MNEMONIC	DESCRIPTION
8	ROTATE	NOT USED
9	WRTL	WRITE THE ALU Y BUS (BITS 0-11) TO AN EXTERNAL REGISTER SPECIFIED BY INSTRUCTION BUS BITS 0-15
A	WRTU	WRITE THE ALU Y BUS (BITS 12-23) TO AN EXTERNAL REGISTER SPECIFIED BY INSTRUCTION BUS BITS 0-15
B	WRTE	WRITE THE EMIT FIELD CONTENTS (BITS 0-11) TO AN EXTERNAL REGISTER SPECIFIED BY INSTRUCTION BUS BITS 0-15
C	RD	READ INTO THE ALU D BUS (BITS 0-11) FROM AN EXT. REGISTER SPECIFIED BY INSTRUCTION BUS BITS 0-15
D	RDXFER	TRANSFER BITS 0-11 ON THE ALU D BUS TO BITS 12-23 ON THE ALU D BUS
E	CTL	PERFORM A CONTROL OPERATION TO AN EXTERNAL BOARD (OR XMC). THE CTL DETERMINES WHICH GATES ARE ENABLED
F	NOP	

EXTERNAL MODULE (BITS 32 - 35):

BITS 32-35 (INSTRUCTION BUS BITS 12-15) DEFINE WHICH BOARD THE INSTRUCTION IS GOING TO.

DESTINATION (BITS 28 - 31):

IF THE SOURCE FIELD INDICATES R0-R15, BITS 28-31 (INSTRUCTION BUS BITS 8-11) DEFINE THE DESTINATION OF THE INFORMATION BEING SENT TO A SPECIFIC BOARD. THESE BITS INDICATE WHAT EXTERNAL REGISTER IS TO BE USED AND WHAT OPERATION IS BEING PERFORMED IN THE EXTERNAL REGISTER OF A PARTICULAR BOARD.

SOURCE (BITS 24 - 27):

BITS 24-27 (INSTRUCTION BUS BITS 4-7) INDICATE WHERE INFORMATION CAME FROM ON THE ALU. THE SOURCE DEFINES THE REGISTER WHICH THE XMC USES TO READ FROM OR WRITE TO.

DESTINATION (BITS 20 - 23):

BITS 20-23 (INSTRUCTION BUS BITS 0-3) DEFINE THE SOURCE OF THE REGISTER IF THE SOURCE FIELD (BITS 24-27) INDICATES R0-R15.

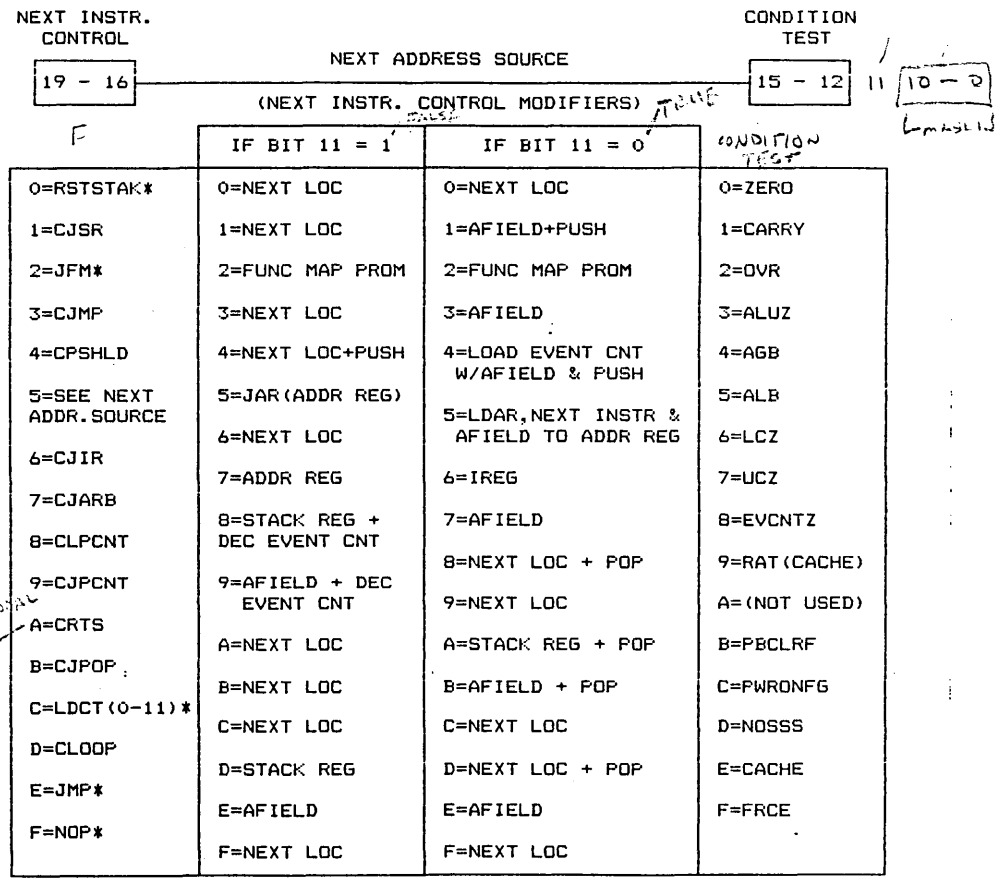
EMIT FIELD (BITS 0 - 11):

THE EMIT FIELD IS USED WHEN A WRITE EMIT (WRTE) IS INDICATED IN THE OPERATION FIELD (BITS 36-39). WHEN A WRITE EMIT OCCURS, DATA WHICH IS TO BE WRITTEN TO A BOARD IS PLACED IN THE MICROCODE IN THE WRITE EMIT FIELD. THEN THE VALUE IN THE EMIT FIELD IS WRITTEN TO THE REGISTER ON ONE OF THE EXTERNAL BOARDS.

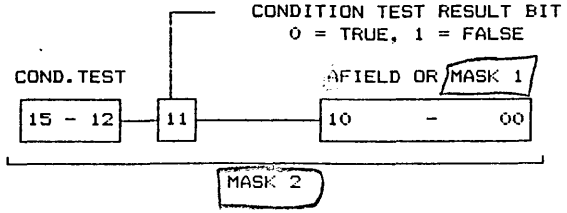
XMCP CONTROL FUNCTIONS:

MNEMONIC	DESCRIPTION	HEX REPRESENTATION
HSSMRST	RESET HSSM INTERRUPTS	0 0 8 2
SMCRST	XMC RESET	0 0 8 4
WMARST	RESET & DESELECT HIGH SPEED MEMORY	0 0 8 8
SYSRST	SYSTEM RESET	0 0 8 F
UMPRST	DESELECT CURRENT HAIO	0 0 9 0
SCHDAK	SEARCH DATA ACKNOWLEDGE	0 1 0 8
RSTODAK	RESET OUTPUT DATA ACKNOWLEDGE	0 2 0 2
RSTIDAK	RESET INPUT DATA ACKNOWLEDGE	0 2 0 4
AUTOLD	AUTOLOAD (PAD ZEROS) MODE	0 2 0 8

NEXT INSTRUCTION INDICATOR (BITS 00 - 19):



* UNCONDITIONAL OPERATION



NEXT INSTRUCTION CONTROL (BITS 16 -19):

INFORMATION ON BITS 16-19 IS DRIVEN TO THE NEXT INSTRUCTION CONTROL PROM AND CAUSES THE PROM TO OUTPUT INFORMATION TO THE SEQUENCER. THE PROM CONTROLS THE SEQUENCER.

CONDITION TEST DEFINITIONS (BITS 12 - 15):

BITS 12-15 DEFINE THE TYPE OF CONDITION BEING TESTED. THESE BITS DETERMINE THE TEST THAT MUST BE SATISFIED AS PART OF THE CONDITION TEST. ONLY 1 INPUT CAN BE ENABLED TO THE OUTPUT LINE AT ANY ONE TIME.

HEX CODE	MNEMONIC	DESCRIPTION
0	ZERO	ZERO, LOW, 0 NEVER SATISFY CONDITION
1	CARRY	IS THE CARRY OUT OF THE ALU SET ?
2	OVR	IS THE OVERFLOW STATUS FLAG ON THE ALU SET ?
3	ALUZ	IS THE ENTIRE ALU OUT LINES (0-23) ZERO ?
4	AGB	USED WITH SUBTRACT FUNCTION: A GREATER THAN B
5	ALB	USED WITH SUBTRACT FUNCTION: A LESS THAN B
6	LCZ	ARE ALU OUTPUTS 0-11 = 0 ?
7	UCZ	ARE ALU OUTPUTS 12-23 = 0 ?
8	EVCNTZ	IS THE EVENT COUNTER = 0 ?
9	RAT	IS THE SYSTEM RATQUIC(CACHE), NO JUMPER AR1 11 -> 12
A		NOT USED
B	PBCLRF	WAS THE PUSHBUTTON PUSHED ?
C	PWRONFG	IS THE POWER-UP FLAG SET ?
D	NOSSS	NO SOLID STATE STORAGE OPTION JUMPER NO JUMPER BETWEEN AR1 5 -> 6
E	CACHE	CACHE OPTION: JUMPER, NO JUMPER BETWEEN AR1 13 -> 14
F	FRCE	1, HIGH, ONE, ALWAYS SATISFY CONDITION

CONDITION TEST NEXT ADDRESS SOURCE (BIT 11):

THE CONDITION TEST BIT INDICATES IF THE CONDITION TEST IS TO BE TRUE OR FALSE. IF BIT 11 EQUALS 0, THE CONDITION IS TRUE. IF BIT 11 EQUALS 1, THE CONDITION TEST IS FALSE.

BITS (0 -10):

BITS 0-10 ARE USED TO SELECT THE NEXT ADDRESS SOURCE, OR TO PERFORM A MASKING OPERATION. THE NEXT ADDRESS SOURCE BITS 0-10 DEFINES THE ADDRESS TO JUMP TO. MASKS ARE USED TO DETERMINE AN UNKNOWN NUMBER (i.e. A KNOWN NUMBER IS PLACED IN THE MASK TO DETERMINE THE UNKNOWN NUMBER). WHEN PERFORMING A MASKING OPERATION THE NUMBER TO BE MASKED IS PLACED IN EITHER MSK1 OR MSK2, DEPENDING ON THE SIZE OF THE NUMBER. MSK1 TESTS A NUMBER UP TO 16 BITS.

INPUT/OUTPUT BUSSES:

INPUT/OUTPUT BUSSES ARE TRI-STATE, BIDIRECTIONAL BUSSES. THEY HAVE 3 VOLTAGE LEVELS; (0) LOW, (2) INACTIVE, OR (+5) HIGH. DATA IS TRANSMITTED THRU A BUS USING LOW OR HIGH. WHEN DATA IS NOT BEING TRANSMITTED THRU THE BUS, THE SIGNAL IS INACTIVE.

U BUS:

DATA IS TRANSMITTED THRU THE U BUS AS A 36 BIT WORD + 2 PARITY BITS. BITS 0-17 PLUS 1 PARITY BIT COMPRISE THE LOWER HALF OF THE 36 BIT WORD. BITS 18-36 PLUS 1 PARITY BIT COMPRISE THE UPPER HALF OF THE 36 BIT WORD. THE U BUS IS USED TO TRANSMIT 5 TYPES OF INFORMATION:

1. COMMAND FUNCTION WORDS
2. ADDRESS FUNCTION WORDS
3. STATUS WORDS
4. OUTPUT DATA
5. INPUT DATA

THE COMMAND AND ADDRESS FUNCTION WORDS ARE TRANSFERRED BETWEEN THE 2HAIO AND THE XMC. THE XMC BREAKS DOWN THE COMMAND AND ADDRESS FUNCTION WORD DATA TO DETERMINE THE TYPE OF OPERATION TO BE PERFORMED. THE XMC ALSO TRANSMITS EXTERNAL INTERRUPTS (STATUS WORDS) THRU THE U BUS TO THE 2HAIO.

CT BUS:

THE CT BUS IS THE OVERALL COMMUNICATIONS BUS. THIS BUS IS CONNECTED TO ALL BOARDS EXCEPT THE 2HAIO. THE DATA TRANSMITTED ON THE CT BUS IS 12 BITS + 1 PARITY.

INSTRUCTION BUS:

THE XMC SENDS INSTRUCTIONS TO ALL BOARDS, EXCEPT THE 2HAIO BOARD, VIA THE INSTRUCTION BUS. THE INSTRUCTION BUS IS UNIDIRECTIONAL; ITS ONLY PURPOSE IS TO SUPPLY THE BOARDS WITH INFORMATION. THE INSTRUCTIONS WHICH ARE CONTAINED IN THE BITS 20-35 OF THE EXTERNAL MICROINSTRUCTION WORD ARE DRIVEN OUT AS BITS 0-15 ON THE INSTRUCTION BUS.

CLOCK:

THE XMC HOLDS A 20 MEGAHERTZ CRYSTAL OSCILLATING CLOCK. THE MASTER CLOCK CIRCUITRY WITHIN THE XMC PROVIDES THE BOARDS WITH A CONTINUOUS SET OF CLOCKS TO ENSURE THAT ALL THE BOARDS IN THE SYSTEM ARE IN SYNC.

MACRO INSTRUCTION SET

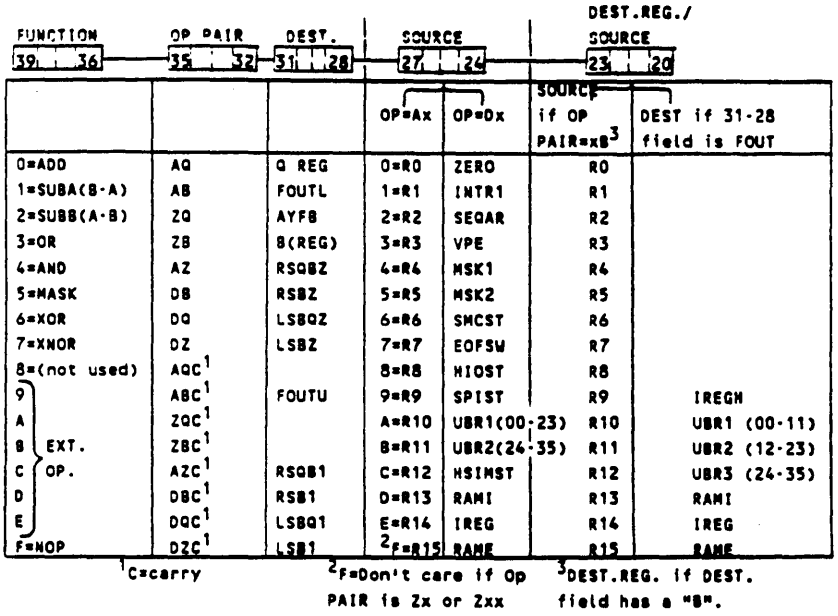
```
OLDREG      OR ZQ,FOUTL,,EXT.REG.
NOLDREG     XNOR ZQ,FOUTL,,EXT.REG.
ALDREG      OR AZ,FOUTL,R0-R15,EXT.REG.
NALDREG     XNOR AZ,FOUTL,R0-R15,EXT.REG.
OLDREGU     OR ZQ,FOUTU,,EXT.REG.
NOLDREGU    XNOR ZQ,FOUTU,,EXT.REG.
ALDREGU     OR AZ,FOUTU,R0-R15,EXT.REG.
NALDREGU *  XNOR AZ,FOUTU,R0-R15,EXT.REG.
RDREGB      OR DZ,B,EXT.REG.,R0-R15
RDREGQ   *  OR DZ,Q,EXT.REG.
INCRB       ADD ZBC,B,,R0-R15
INCRQ       ADD ZQC,Q
INCRD       ADD DZC,FOUTL,EXT.REG.,EXT.REG.
DECRB       SBA ZB,B,,R0-R15
DECRQ       SBA ZQ,Q
DECRD       SBA DZ,FOUTL,EXT.REG.,EXT.REG.
TSTRMSK     XOR DB,Q,MSK2,R0-R15 & NOP VAR
TSTQMSK     XOR DQ,Q,MSK2 & NOP VAR
TSTRBIT     AND DB,Q,MSK2,R0-R15
TSTQBIT     AND DQ,Q,MSK2
RSTRBIT     MASK DB,B,MSK2,R0-R15
SETRBIT  *  OR DB,B,MSK2,R0-R15
LSHFTZ      OR ZB,LSBZ,,R0-R15 & CLPCNT EVCNTZ
LSHFT1      OR ZB,LSB1,,R0-R15
LSHFT2      ADD AB,LSBZ,R0-R15,R0-R15 & CLPCNT EVCNTZ
LSHFTDZ     OR ZB,LSBQZ,,R0-R15 & CLPCNT EVCNTZ
LSHFTD1  *  OR ZB,LSBQ1,,R0-R15
RSHFTZ      OR ZB,RSBZ,,R0-R15 & CLPCNT EVCNTZ
RSHFTDZ  *  OR ZB,RSQBZ,,R0-R15 & CLPCNT EVCNTZ
RESETR      AND ZB,B,,R0-R15
RESETQ   *  AND ZQ,Q
CALL        ADD DZC,B,SEQAR,RX & JMP ADDRESS
BOZ         CJMP ALUZ,ADDRESS
BNZ      *  CJMP NALUZ,ADDRESS
RDMSKB      OR DZ,B,MSK2,R0-R15 & NOP VAR
RDMSKQ   *  OR DZ,Q,MSK2 & NOP VAR
RTOR        OR AZ,B,R0-R15,R0-R15
QTOR        OR ZQ,B,,R0-R15
RTOQ        OR AZ,Q,R0-R15
MOVE     *  OR DZ,FOUTL,EXT.REG.,EXT.REG.
RDRAMB      RDREGB RAME,RX & NOP VAR
RDRAMQ      RDREGQ RAME & NOP VAR
ALDRAM      ALDREG RX,RAME & NOP VAR
ALDRAMU     ALDREGU RX,RAME & NOP VAR
QLDRAM      QLDREG RAME & NOP VAR
QLDRAMU     QLDREGU RAME & NOP VAR
RESETRAM    MOVE ZERO,RAME & NOP VAR
```

```
QLDREG    OR ZQ,FOUTL,,EXT.REG.
NQLDREG   XNOR ZQ,FOUTL,,EXT.REG.
ALDREG    OR AZ,FOUTL,R0-R15,EXT.REG.
NALDREG   XNOR AZ,FOUTL,R0-R15,EXT REG.
QLDREGU   OR ZQ,FOUTU,,EXT.REG.
NQLDREGUXNOR ZQ,FOUTU,,EXT.REG.
ALDREGU   OR AZ,FOUTU,R0-R15,EXT.REG.
NALDREGUXNOR AZ,FOUTU,R0-R15,EXT.REG.
RDREGB    OR DZ,B,EXT.REG.,R0-R15
RDREGQ    OR DZ,Q,EXT.REG.
INCRB     ADD ZBC,B,,R0-R15
INCRQ     ADD ZQC,Q
INCRD     ADD DZC,FOUTL,EXT.REG.,EXT.REG.
DECRB     SBA ZB,B,,R0-R15
DECRQ     SBA ZQ,Q
DECRD     SAB DZ,FOUTL,EXT.REG.,EXT.REG.
TSTRMSK   XOR DB,Q,MSK2,R0-R15 & NOP VAR
TSTQMSK   XOR DQ,Q,MSK2 & NOP VAR
TSTRBIT   AND DB,Q,MSK2,R0-R15
TSTQBIT   AND DQ,Q,MSK2
RSTRBIT   MASK DB,B,MSK2,R0-R15
SETRBIT   OR DB,B,MSK2,R0-R15
LSHFTZ    OR ZB,LSBZ,,R0-R15 & CLPCNT EVCNTZ
LSHFT1    OR ZB,LSB1,,R0-R15
LSHFT2    ADD AB,LSBZ,R0-R15,R0-R15 & CLPCNT EVCNTZ
LSHFTDZ   OR ZB,LSBQZ,,R0-R15 & CLPCNT EVCNTZ
LSHFTD1   OR ZB,LSBQ1,,R0-R15
RSHFTZ    OR ZB,RSBZ,,R0-R15 & CLPCNT EVCNTZ
RSHFTDZ   OR ZB,RSQBZ,,R0-R15 & CLPCNT EVCNTZ
RESETR    AND ZB,B,,R0-R15
RESETQ    AND ZQ,Q
CALL      ADD DZC,B,SEQAR, RX & JMP ADDRESS
BOZ       CJMP ALUZ,ADDRESS
BNZ       CJMP NALUZ, ADDRESS
RDMSKB    OR DZ,B,MSK2,R0-R15 & NOP VAR
RDMSKQ    OR DZ,Q,MSK2 & NOP VAR
RTOR      OR AZ,B,R0-R15,R0-R15
QTOR      OR ZQ,B,,R0-R15
RTOQ      OR AZ,Q,R0-R15
MOVE      OR DZ,FOUTL,EXTREG,EXTREG
RDRAMB    RDREGB RAME,RX & NOP VAR
RDRAMQ    RDREGQ RAME & NOP VAR
ALDRAM    ALDREG RX, RAME & NOP VAR
ALDRAMU   ALDREGU RX, RAME & NOP VAR
QLDRAM    QLDREG RAME & NOP VAR
QLDRAMU   QLDREGU RAME & NOP VAR
RESETRAM MOVE ZERO,RAME & NOP VAR
```

Figure 6-24
Microinstruction Format (cont'd)

6.2.5.1 Internal Operations

This section explains how the microcode affects the internal operation of the XMC circuit board. Microinstruction (MINST) bits 20-39 define the internal arithmetic or logic operation which is to be executed by the XMC. When bit 39 is not active, these bits instruct the ALU what to do, which registers to use, and where to put the results. The following sections describe the function of bits 20-39 when bit 39 is not active.



FUNCTION 39 36	OP PAIR 35 32	DEST. 31 28	SOURCE 27 24 OP=Ax	SOURCE 27 24 OP=Dx	DEST.REG./ SOURCE 23 20 SOURCE if OP PAIR=xB[3]	DEST.REG./ SOURCE 23 20 DEST if 31-28 field is FOUT
0=ADD	AQ	Q REG	0=R0	ZERO	R0	
1=SUBA(B-A)	AB	FOUTL	1=R1	INTR1	R1	
2=SUBB(A-B)	ZQ	AYFB	2=R2	SEQAR	R2	
3=OR	ZB	B(REG)	3=R3	VPE	R3	
4=AND	AZ	RSQBZ	4=R4	MSK1	R4	
5=MASK	DB	RSBZ	5=R5	MSK2	R5	
6=XOR	DQ	LSBQZ	6=R6	SMCST	R6	
7=XNOR	DZ	LSBZ	7=R7	EOFSW	R7	
8=(not used)	AQC[1]		8=R8	HIOST	R8	
9	ABC[1]	FOUTU	9=R9	SPIST	R9	IREGH
A	ZQC[1]		A=R10	UBR1(00-23)	R10	UBR1 (00-11)
B EXT.	ZBC[1]		B=R11	UBR2(24-35)	R11	UBR2 (12-23)
C OP.	AZC[1]	RSQB1	C=R12	HSIMST	R12	UBR3 (24-35)
D	DBC[1]	RSB1	D=R13	RAMI	R13	RAMI
E	DQC[1]	LSBQ1	E=R14	IREG	R14	IREG
F=NOP	DZC[1]	LSB1	[2]F=R15	RAMF	R15	RAMF

[1]C=carry
[2]F=Don't care if Op PAIR is Zx or Zxx
[3]DEST.REG. if DEST. field has a "B".

Function Define - (2MINST Bits 36-39)

As bits 36-38 are driven through the XMC they are transmitted to function control decode lines I3, I4, and I5 (ALU Function Decode) of the ALU. The ALU performs the function decoded as shown in figure 6-25 below.

Mnemonic	Microcode 38 I5	37 I4	36 I3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R+S
SUBA(B-A)	L	L	H	1	S Minus R	S - R
SUBB(A-B)	L	H	L	2	R Minus S	R - S
OR	L	H	H	3	R OR S	R∨S
AND	H	L	L	4	R AND S	R∧S
MASK	H	L	H	5	R AND S	R∧S
XOR	H	H	L	6	R EX-OR S	R⊻S
XNOR	H	H	H	7	R EX-NOR S	R⊻S

Figure 6-25
Function Control Decode

Note that when bit 39 is active, the function decode is 8-F. This is an external operation and is discussed in Section 6.2.5.2.

OP Pair (2MINST Bits 32-35)

The XMC drives bits 32-34 to the ALU as OP Pair lines I0, I1, and I2 (ALU Source Operands Decode). If bit 35 is active, bits 32-34 also require information located on bits 20-27 to further identify the registers or the source of direct inputs. Figure 6-26 provides an illustration of how the OP Pair lines are decoded by the ALU Source Operands.

	MICROCODE				ALU SOURCE OPERANDS	
Mnemonic	34 I5	33 I4	32 I3	Hex Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
AZ	H	L	L	4	0	A
DB	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	Z
AQC	L	L	L	8	A	Q
ABC	L	L	H	9	A	B
ZQC	L	H	L	A	0	Q
ZBC	L	H	H	B	0	B
AZC	H	L	L	C	0	A
DBC	H	L	H	D	D	A
DQC	H	H	L	E	D	Q
DZC	H	H	H	F	D	Z

Figure 6-26
Source Operands Decode

Note that if bit 35 is active it provides a decode of 8-F, which sets a carry-in equal to 1 bit. An explanation of the OP pair lines is provided below.

Explanation of OP Pairs

OP PAIR LINES
I2, I1, I0

2MINST Bits 32-35

Hex Code	Mnemonic	Description
0	AQ	If line A is defined as one of the pairs, use bits 24-27 to determine the address of the A register (bits 24-27 then correspond to address lines A0-A3 of the ALU).

1	AB	If line B is specified as an OP pair, use bits 20-23 to determine the address of the B register (bits 20-23 correspond to address lines B0-B3 of the ALU).
2	ZQ	OP pair is 0 and Q register.
3	ZB	OP pair is 0 and B register.
4	AZ	OP pair is A (specified by bits 24-27) and 0.
5	DB	If D is specified as one of the OP pairs use bits 24-27 to determine which external registers will unload the D inputs.
6	DQ	Direct input as specified by bits 24-27 and Q register.
7	DZ	Direct input as specified by bits 24-27 and 0.
8-F		These OP pairs are identical to 0-7 with the addition of a carry which is equal to 1. If bit 35 is a 1 - (high) it will set 2 ALUCN. For further information refer to page 20 of the Logics Manual; see the XMC-EF6 section.

Destination Define (2MINST Bits 28-31)

The destination define uses bits 28-30 to instruct the ALU where to place the result of an arithmetic operation. These bits are driven to the XMC as I6, I7, and I8 (ALU Destination Decode) as shown in figure 6-27.

	MICROCODE				RAM FUNCTION		Q-REG FUNCTION			RAM SHIFTER		Q SHIFTER	
	30	29	28	Hex					Y				
MNEMONIC	I8	I7	I6	Code	Shift	Load	Shift	Load	Output	RAM0	RAM3	Q0	Q3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
FOUTL	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
AYFB	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
B(REG)	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RSQBZ	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F0	IN3	Q0	IN3
RSBZ	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F0	IN3	Q0	X
LSBQZ	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN0	F3	IN0	Q3
LSBZ	H	H	H	7	UP	2F → B	X	NONE	F	IN0	F3	X	Q3
--	-	-	-	8	-	-	-	-	-	-	-	-	-
FOUTU	L	L	H	9	X	NONE	X	NONE	F	X	X	X	X
--	-	-	-	A	-	-	-	-	-	-	-	-	-
--	-	-	-	B	-	-	-	-	-	-	-	-	-
RSQB1	H	L	L	C	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F0	IN3	Q0	IN3
RSB1	H	L	H	D	DOWN	F/2 → B	X	NONE	F	F0	IN3	Q0	X
LSBQ1	H	H	L	E	UP	2F → B	UP	2A → Q	F	IN0	F3	IN0	Q3
LSB1	H	H	H	F	UP	2F → B	X	NONE	F	IN0	F3	X	Q3

Figure 6-27
Destination Decode

Bit 31 is used as a flag. If bit 31 contains a 1, it defines either FOUT upper or adds a carry-in equal to 1 for all other shift operations (hex codes 4 through 7 and C through F). If bit 31 contains a 0, it defines either FOUT lower or a carry-in equal to 0. For hex codes 1 and 9, it defines FOUT lower or upper. An explanation of the destination lines is provided below.

Explanation of Destination Lines

DEST LINES I8 I7 I6 Hex Code	Mnemonic	2MINST Bit 28-31 Description
0	Q Register	
1	FOUTL	Enable lower 12 bits onto ALU Y lines. The destination is defined with bits 20-23 (e.g., Line A = UBR1 - U bus register).
2	AYFB	Accomplishes 2 functions: 1) loads the contents of the Rx as addressed by the A field (A0 - A3) to the ALU Y bus, and 2) loads the ALU F bus to the Rx as specified by B field (B0 - B3). NOTE: Rx = R0 to R15 (where x equals one of the 16 registers) 1) A = Y 2) F = B
3	B Register	Writes to Rx as addressed by the B field (bits 20-23).
4	RSQBZ	Right shift the F word with a 0 and store it in B and Q registers. 1) F/2 → B with Qo 2) Q/2 → Q with a "0" into Q23
5	RSBZ	Right shift F word with a 0, but only load to B (not Q) register.

6	LSBQZ	Left shift F word with Q and load to B and Q registers. Examples F = 5 F = 0101 LSZ F = 1010 = 10 2F -> B with a "0" 2Q -> Q with B23
7	LSBZ	Left shift F word with 0, only load to B register.
8	Not Defined	
9	FOUTU	Load the upper ALU bits, 12-23 to the Y bus and write to an external register specified by bits 20-23.
A	Not Defined	
B	Not Defined	
C	RSQB1	Right shift, load to Q and B registers. F/2 -> B with Qo Q/2 -> Q with a "1" into Q23
D	RSB1	Right shift with a one, load to B register.
E	LSBQ1	Left shift, load to Q and B registers. F/2 -> B with a "1" into B0 Q/2 -> Q with B23
F	LSB1	Left shift with a one, load to B register.

Source (2MINST Bits 24-27)

Source bits 24-27 perform different functions depending upon the information which is displayed in the OP pair (bits 32-35) field. If the OP pair specifies an A register input, the source bits serve as the pointer for address lines A0-A3. Hex codes 0-F equal R0-R15 as shown in Figure 6-23. If the OP pair specifies a D input (Direct Input lines D0-D3 of the ALU), the source bits specify the input source per the table below. Note that the page numbers listed below refer to pages in the Logics Manual.

DIRECT INPUT LINES

SOURCE OF DIRECT INPUT LINES

Hex Code	Mnemonic	Description
0	ZERO	
1	INTR1	Interrupt Register Page 19 EL1, EL2
2	SEQAR	Sequence address register page 10 BD3, BD2
3	VPE	Vector priority encoder page 6 DF4, DH4
4	MSK1	Mask 1 field 2MINST 00-10 page 14 BF1, BF2
5	MSK2	Mask 2 field 2MINST 00-15 page 14 BF1, BF2, BF3
6	SMCST	XMC Status register page 19 AF5, AD4
7	EOFSW	Option jumper register page 18 BB5, EM3
8	HIOST	HAIO status register page 18 BH2, BH3
9	SPIST	SPI status register page 19 BH4
A	UBR1	U Bus register bits 0-23 page 1
B	UBR2	U Bus register bits 24-35 page 1
C	HSIMST	Page 23 BH5
D	RAMI	SMB RAM (scratchpad ram) as addressed by the I register page 6 and page 30 DH5, DK5
E	IREG	I register through the Move Gate page 6 DD4, DF2
F	RAME	SMB RAM (scratchpad ram) as addressed by the Emit Field 2MINST 00-09 page 30 (00-10 page 30 for systems operating under a multihost environment)

If the Op pair specifies a B register input, bits 20-23 are used instead of bits 24-27. Bits 20-23 serve as a pointer for address lines B0 - B3 (0-F = R0-R15). See the following section for details.

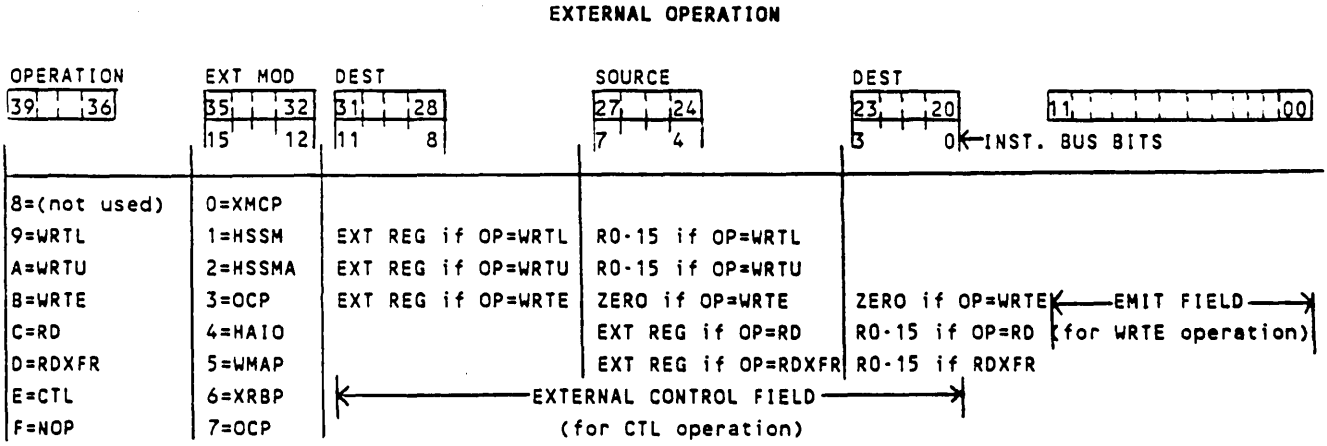
2MINST Bits 20-23

Bits 20-23 further define the Destination Define (bits 28-31) or the Source (bits 24-27) input fields. If the Destination Define field is Fout or B, bits 20-23 show the output of the result. If the Source field is B, bits 20-23 further define the register per the table below. The page numbers below refer to pages in the Logics Manual.

Hex Code	Mnemonic	Description
9	IREGH	IREG bits 12 & 13 FH3 page 10A (XMC section)
A	UBR1	U Bus register bits 0-11 page 4 (XMC section)
B	UBR2	U Bus register bits 12-23 page 4 (XMC section)
C	UBR3	U Bus register bits 24-35 page 4 (XMC section)
D	RAMI	SMB RAM as addressed by the IREG page 30 (XMC section)
E	IREG	IREG = DK5, DH5 page 6 (XMC section)
F	RAME	SMB RAM as addressed by the Emit field page 30 (XMC section)

6.2.5.2 External Operations

External operations are defined when bit 39 is active. Bits 36-38 define the type of operation to be performed and bits 20-35 further define which external board will be accessed, which bus will be used, which register will be accessed (source or destination) or in the case of a control function, which gates will be enabled or disabled.



When the microinstruction code indicates an external operation, bits 20-35 pass through a bus driver chip. These bits are driven out on bits 0-15 of the instruction bus. The XMC sends instructions to the other boards via the instruction bus. Figure 6-27 provides a listing of the boards and registers. The following sections describe the function of bits 20-39 when bit 39 is active.

XMCP CONTROL FUNCTIONS

Mnemonic	Meaning	Hexadecimal Representation			
HSSMRST	Reset HSSM Interrupts	0	0	8	2
SMCRST	XMC Reset	0	0	8	4
WMARST	Reset & Deselect High Speed Memory	0	0	8	8
SYSRST	System Reset	0	0	8	F
UMPRST	Deselect Current HAIO	0	0	9	0
SCHDAK	Search Data Acknowledge	0	1	0	8
RSTODAK	Reset Output Data Acknowledge	0	2	0	2
RSTIDAK	Reset Input Data Acknowledge	0	2	0	4
AUTOLD	Autoload (Pad Zeros) Mode	0	2	0	8
	SET PAGE		4	0	X

X = 0, 1, 2, 3, 4, 5

memory page

Figure 6-28
XMCP External Read/Write/Control Functions

Operation (2MINST Bits 36-39)

Bits 36-39 define the type of external operation which will be performed.

Hex Code	Mnemonic	Description
8	ROTATE	Not Used.
9	WRTL	Write the ALU Y bus (bits 0-11) to an external register specified by instruction bus bits 0-15.
A	WRTU	Write the ALU Y bus (bits 12-23) to an external register specified by instruction bus bits 0-15.
B	WRTE	Write the Emit Field contents (bits 0-11) to an external register specified by instruction bus bits 0-15.
C	RD	Read into the ALU D bus (bits 0-11) from an external register specified by instruction bus bits 0-15.
D	RDXFER	Transfer bits 0-11 on the ALU D bus to bits 12-23 on the ALU D bus (see page 2 of the XMC in the Logics Manual).
E	CTL	Perform a control operation to an external board (or XMC). The CTL determines which gates are enabled.

External Module (2MINST Bits 32-25)

Bits 32-34 (instruction bus bits 12-14) define which board the instruction is going to. See section 6.2.7 for instruction bus information.

Destination (2MINST Bits 28-31)

If the Source field indicates R0-R15, bits 28-31 (instruction bus bits 8-11) define the destination of the information being sent to a specific board. These bits indicate what external register is to be used and what operation is being performed in the external register of a particular board.

Source (2MINST Bits 24-27)

Bits 24-27 (instruction bus bits 4-7) indicate where information came from on the ALU. The Source defines the register which the XMC uses to read from or write to.

For example, if the operation is a write operation, data is written to the Destination field and read from the Source field. If the operation is a read operation, data is read from the Destination field and written to the Source field.

(2MINST Bits 20-23)

Bits 20-23 (instruction bus bits 0-3) define the source of the register if the Source field (bits 24-27) indicates R0 to R15.

Emit Field (2MINST Bits 0-11)

The Emit field is used when a Write Emit (WRTE) is indicated in the OPER field (bits 36-39). When a Write Emit occurs, data which is to be written to a board is placed in the microcode in the Write Emit field. Then the value in the emit field is written to the register on one of the external boards.

The next several pages show examples of various External Operations.

EXAMPLES OF EXTERNAL FUNCTIONS

Example A - Write Lower (WRTL)

```
9    3    5          0    F
WRTLSCP  LDDISP1    R0
```

where:

9 = WRTL
3 = SCP CT Bus
5 = 2INST Bus Bits 8 and 10 are set
0 = 2INST Bus Bits 4-7 are not set
(These bits are used to determine the R register.)
F = 2INST Bus Bits 0-3 are set (not used)

The lower 12 bits of R0 (bits 0-11) are written to register LDDISP1 on the SCP using the CT Bus. The SCP is the system control panel portion of the OCP. Refer to page 20 of the OCP section in the Logics Manual.

FF3 is the write decode. Pins 1 through 6 are represented as follows:

FF3 pin 6 is active (3 WRTEXT)
FF3 pin 5 is active low (AND of SCP select)
FF3 pin 4 is active low (3INST Bus Bit 11 is not set)
FF3 pin 3 - set (3INST10)
FF3 pin 2 - not set (3INST09)
FF3 pin 1 - set (3INST08)

Example B - Write Upper (WRTU)

Write Upper (WRTU) is the same format as described above, however the upper 12 bits (bits 12-23) of the specified register (R0-R15) are used as the source.

Example C - Write Emit (WRTE)

B1100 F0002

The following example shows the outcome of the emit field (002) after it is written to the SM address register MSB's on the HSSM using the CT bus.

B = WRTEMIT
1 = HSSM board
1 = LDSARM
0 = NOT USED
0 = NOT USED

F = NOP
0 = NOT USED
0 = EMIT FIELD
0 = EMIT FIELD
2 = EMIT FIELD

Example D - Read Operation (RD)

C	3	0	3	0
RD	SCP		PGRMSEL	R0

Read register PGRMSEL on the SCP into R0

where:

C = Read
3 = SCP - use the CT bus
0 = 2INST bus bits 8-11 are not set
3 = 2INST bus bits 4 and 5 are set
0 = R0

Refer to OCP logics - SCP instruction decode sheet 20. FF2-74S138.

FF2 pin 1 = 3INST 04	=	1
FF2 pin 2 = 3INST 05	=	1
FF2 pin 3 = 3INST 06	=	0
FF2 pin 4 = 3INST 07	=	0
FF2 pin 5 = 9SCPSEL	=	0
FF2 pin 6 = 3RDALU	=	1

FF2 decodes a 3. Pin 12 goes low and enables register PRGMSEL (Thumbwheel switch) to the CT bus.

Example E - Control Operation (CTL)

```
E          7    C          0   0
Control    OCP  OCPDSEL
```

where:

E = Control
7 = OCP
C = 2MINST 11 and 10 set
0 = 2MINST 4-7 (low)
0 = 2MINST 0-3 (low)

For further information refer to OCP logics page 6 in the Data Logics manual.

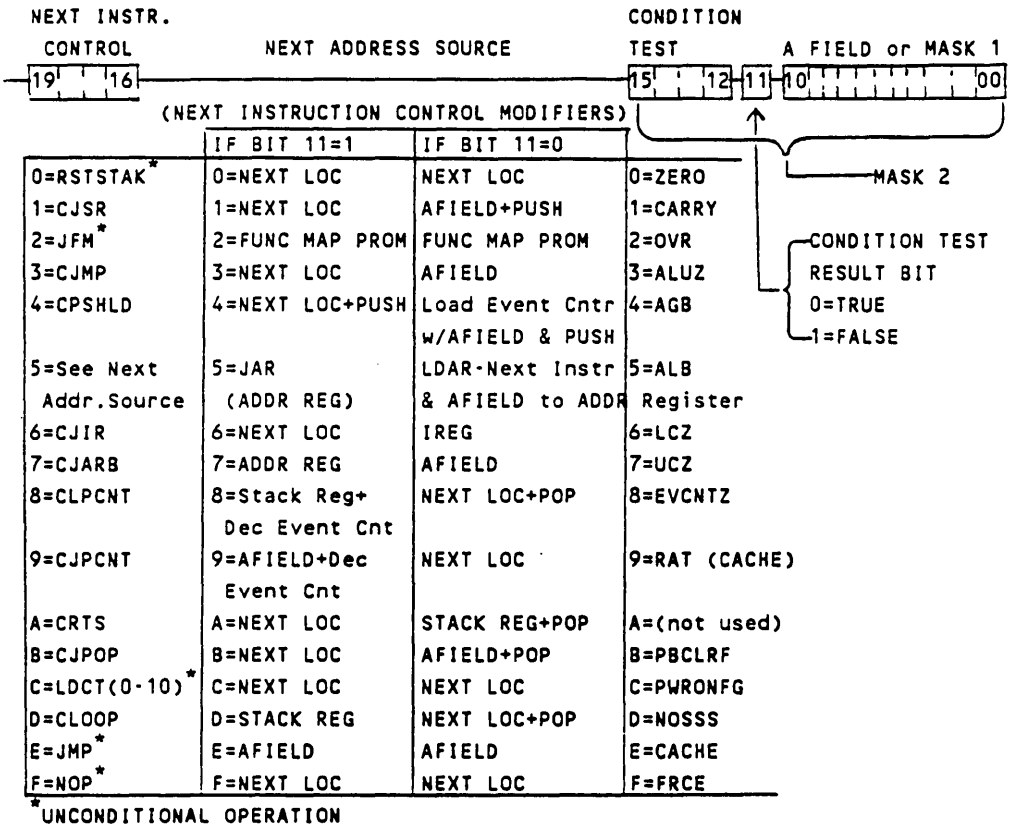
CM1 - 1, 2, 3 and CK1 - 1, 2, 13,and 12.

CM1 -	pin 1	=	2OCPSEL = 1
	pin 2	=	2OCTRLALU = 1
	pin 3	=	2OCPCTL = 1
CM1 -	pin 1	=	2OCPCTL=1
	pin 2	=	2INSTB 10=1
	pin 13	=	2INSTB 11=1
	pin 12	=	2 OCPRST=1

Causes the OCPREQUEST Flip-Flop; CM3 to reset through the K input, or OCP DESELECT.

6.2.6 Next Instruction Indicator

Bits 00-19 identify the next instruction to be executed by the microprogram.



	IF BIT 11=1	IF BIT 11=0	
0=RSTSTAK*	0=NEXT LOC	NEXT LOC	0=ZERO
1=CJSR	1=NEXT LOC	AFIELD+PUSH	1=CARRY
2=JFM*	2=FUNC MAP PROM	FUNC MAP PROM	2=OVR
3=CJMP	3=NEXT LOC	AFIELD	3=ALUZ
4=CPSHLD	4=NEXT LOC+PUSH	Load Event Cntr w/AFIELD & PUSH	4=AGB
5=See Next Addr.Source	5=JAR (ADDR REG)	LDAR-Next Instr & AFIELD to ADDR	5=ALB Register
6=CJIR	6=NEXT LOC	IREG	6=LCZ
7=CJARB	7=ADDR REG	AFIELD	7=UCZ
8=CLPCNT	8=Stack Reg+ Dec Event Cnt	NEXT LOC+POP	8=EVCNTZ
9=CJPCNT	9=AFIELD+Dec Event Cnt	NEXT LOC	9=RAT (CACHE)
A=CRTS	A=NEXT LOC	STACK REG+POP	A=(not used)
B=CJPOP	B=NEXT LOC	AFIELD+POP	B=PBCLRF
C=LDCT(0-10)*	C=NEXT LOC	NEXT LOC	C=PWRONFG
D=CLOOP	D=STACK REG	NEXT LOC+POP	D=NOSSS
E=JMP*	E=AFIELD	AFIELD	E=CACHE
F=NOP*	F=NEXT LOC	NEXT LOC	F=FRCE

*UNCONDITIONAL OPERATION

Next Instruction Control (2MINST Bits 16-19)

Information on bits 16-19 is driven to the Next Instruction Control PROM and causes the PROM to output information to the sequencer. The PROM controls the sequencer. All of the control lines for the sequencer are driven by the outputs of PROM 6-31A at DH3 on XMC sheet 9 as indicated in Figure 6-29 - Next Address PROM.

An explanation of the Next Instruction Control bits is provided on the following pages.

		2MINST 19	2MINST 18	2MINST 17	2MISNT 16	TEST 1=TRUE 0=FALS		PLE VECTOR	COUNTER EN	COUNTER LD	S0	S1	FE	PUP	MAP E	OUTPUT	XMC NEXT PROM WITH PPS	
	HEX	ADDRESS					ADDR	PINS										
	CODE	A4	A3	A2	A1	A0	(DEC.)	9	7	6	5	4	3	2	1	HEX	MNEMONIC	SUBMNEMONIC
00		0	0	0	0	0	0	H	H	H	L	L	H	H	H	E 7	RSTSTAK	
01	0	0	0	0	0	1	1	H	H	H	L	L	H	H	H	E 7		N/U
02		0	0	0	1	0	2	H	H	H	L	L	H	H	H	E 7	CJSR	INC1
03	1	0	0	0	1	1	3	H	H	H	H	H	L	H	H	F 8		JSR
04		0	0	1	0	0	4	H	H	H	H	H	H	H	L	F E	JFM	
05	2	0	0	1	0	1	5	H	H	H	H	H	H	H	L	F E		N/U
06		0	0	1	1	0	6	H	H	H	L	L	H	H	H	E 7	CJMP	INC2
07	3	0	0	1	1	1	7	H	H	H	H	H	H	H	H	F 7		
08		0	1	0	0	0	8	H	H	H	L	L	L	H	H	E 3	CPSHLD	PUSH
09	4	0	1	0	0	1	9	H	H	L	L	L	L	H	H	E 3		PSHLD
0A		0	1	0	1	0	10	H	H	H	H	L	H	H	H	F 7	N/U	JAR
0B	5	0	1	0	1	1	11	H	H	H	L	L	H	L	H	E 5		LDAR
0C		0	1	1	0	0	12	L	H	H	L	L	H	H	H	6 7	CJIR	
0D	6	0	1	1	0	1	13	L	H	H	H	H	H	H	H	7 E		JIR
0E		0	1	1	1	0	14	H	H	H	H	L	H	H	H	F 7	CJARB	
0F	7	0	1	1	1	1	15	H	H	H	H	H	H	H	H	F F		
10		1	0	0	0	0	16	H	L	H	H	H	H	H	H	B F	CLPCNT	
11	8	1	0	0	0	1	17	H	H	H	L	L	L	L	H	E 1		POP
12		1	0	0	1	0	18	H	L	H	H	H	H	H	H	B F	CJPCNT	JPCNT
13	9	1	0	0	1	1	19	H	H	H	L	L	H	H	H	E 7		
14		1	0	1	0	0	20	H	H	H	L	L	H	H	H	E 7	CRTS	
15	A	1	0	1	0	1	21	H	H	H	H	H	L	L	H	F 9		RTS
16		1	0	1	1	0	22	H	H	H	L	L	H	H	H	E 7	CJPOP	
17	B	1	0	1	1	1	23	H	H	H	H	H	L	L	H	F 9		JPOP
18		1	1	0	0	0	24	H	H	L	L	L	H	H	H	C 7	LDCT	
19	C	1	1	0	0	1	25	H	H	L	L	L	H	H	H	C 7		N/U
1A		1	1	0	1	0	26	H	H	H	H	H	H	H	H	F F	CLOOP	LOOP
1B	D	1	1	0	1	1	27	H	H	H	L	L	L	L	H	E 1		
1C		1	1	1	0	0	28	H	H	H	H	H	H	H	H	F F	JMP	
1D	E	1	1	1	0	1	29	H	H	H	H	H	H	H	H	F F		N/U
1E		1	1	1	1	0	30	H	H	H	L	L	H	H	H	E 7	INC	
1F	F	1	1	1	1	1	31	H	H	H	L	L	H	H	H	E 7		N/U

Figure 6-29
Next Address PROM

Condition Test Definitions (2MINST Bits 12-15)

Bits 12-15 define the type of condition being tested. These bits determine the test that must be satisfied as part of the condition test. Only 1 input can be enabled to the output line at any one time. DK2 allows test 0-7 and DM2 allows test 8-F, as defined below.

DM2 and DK2 are two 7 to 1 muxs with outputs tied together which feed the EXCLUSIVE OR gates feeding the PROM. The multiplexers are enabled by 2MINST bus bits 12-15. Refer to the Logics Manual, page 8 of the XMC section, for more details.

DEFINITIONS OF CONDITION TEST

logic pages 8 DK2 = 0-7 DM2 = 8-F

Hex Code	Mnemonic	Description
0	ZERO	Zero, low, 0 never satisfy condition
1	CARRY	Is the carry out of the ALU set?
2	OVR	Is the overflow status flag on the ALU set?
3	ALUZ	Is the entire ALU out lines (0-23) zero?
4	AGB	Used with subtract function: A greater than B (See section 6.2.5.1.)
5	ALB	Used with subtract function: A less than B (See section 6.2.5.1.)
6	LCZ	Are ALU outputs 0-11 = 0?
7	UCZ	Are ALU outputs 12-23 = 0?
8	EVCNTZ	Is the event counter = 0?
9	RAT	Is the system RATQUIC (CACHE)? No jumper between AR1-11->12 (for non-multihost envrionments) OR switch 2-8 open (for multihost environments.) (See page 6.75.)
A	NOT USED	
B	PBCLRF	Was the reset push button pushed?
C	PWRONFG	Is the power-up flag set?
D	NOSSS	No solid state storage option. No jumper between AR1-5->6 (for non-multihost environments) OR Switch 2-3 open (for multihost environments.) (See page 6.75.)
E	CACHE	Cache option: jumper, no jumper between AR1-13->14 (for non-multihost environments) OR switch 2-1 open (for multihost environments.) (See page 6.75.)
F	FRCE	1, HIGH, ONE, ALWAYS SATISFY CONDITION

Condition Test Next Address Source (2MINST Bit 11)

The condition test bit indicates if the condition test is to be true or false. If bit 11 equals 0, the condition test is true. If bit 11 equals 1, the condition test is false.

(2MINST Bits 0-10)

Bits 0-10 are used to select the Next Address Source, or to perform a Masking Operation.

The Next Address Source (bits 0-10) defines the address to jump to. Masks are used to determine an unknown number (i.e., a known number is placed in the mask to determine the unknown number). When performing a masking operation the number to be masked is placed in either MSK1 or MSK2, depending on the size of the number. MSK1 tests a number up to 11 bits (bits 0-10). MSK2 tests a number up to 16 bits (bits 0-15).

6.2.7 Input/Output Busses

A bus is two or more conductors running in parallel used for carrying information between two electronic devices (e.g. two boards). Unisys uses a tri-stated, bi-directional bus which utilizes 8T-Series driver and receiver integrated circuit (IC) chips. This section describes the functions of the U, CT, and Instruction busses which are used in the mass storage subsystem.

Input/output busses have 3 voltage levels: low (0), inactive (2), or high (+5). Data is transmitted through a bus using low or high signals. When data is not being transmitted through the bus, the signal is inactive. The bus is the communication device which allows the boards to communicate with each other. The diagram in Figure 6-30 shows the flow of the busses.

6.2.9 Display Indicators and Module Options

SCRATCH PAD MEMORY

DISPLAY	ADDR.	LABEL	CONTENTS	
400-555	000-3FF		HSSM Buffer Data	
400	000	SEN00	Sense Byte 0	
"	001	SEN01	Sense Byte 1	
"	002	SEN02	Sense Byte 2	
401	003	SEN03	Sense Byte 3	(Recovery Action)
"	004	SEN04	Sense Byte 4	(Drive Physical I.D.)
"	005	SEN05	Sense Byte 5	(Emulated Cyl. LSBs)
402	006	SEN06	Sense Byte 6	(Emulated Cyl. MSBs/Head)
"	007	SEN07	Sense Byte 7	(Error Format/Message)
"	008	SEN108	Sense Byte 8, Format 1	
403	009		Sense Byte 9, Format 1	
"	00A	SEN110	Sense Byte 10, Format 1	
"	00B	SEN111	Sense Byte 11, Format 1	
404	00C	SEN112	Sense Byte 12, Format 1	
"	00D	SEN113	Sense Byte 13, Format 1,2	(Drive No.)
"	00E	SEN114	Sense Byte 14, Format 1,2	(Emulated Drive Status)
405	00F	SEN115	Sense Byte 15, Format 1,2	
"	010	SEN121	Sense Byte 21, Format 1,2	
"	011	SEN408	Sense Byte 8, Format 4,5	(Emulated Cyl. MSBs)
406	012	SEN409	Sense Byte 9, Format 4,5	(Emulated Cyl. LSBs)
"	013		Sense Byte 10, Format 4,5	
"	014	SEN411	Sense Byte 11, Format 4,5	(Emulated Head no.)
407	015	SEN412	Sense Byte 12, Format 4,5	(Emulated Record no.)
"	016		Sense Byte 13, Format 4,5	
"	017		Sense Byte 14, Format 4,5	
408	018	SEN415	Sense Byte 15, Format 4	(SM-Error Retry Count)
"	019	SEN416	Sense Byte 16, Format 4	(Drive Physical I.D.)
"	01A	SEN515	Sense Byte 15, Format 5	
409	01B	SEN516	Sense Byte 16, Format 5	
"	01C	SEN517	Sense Byte 17, Format 5	
"	01D	SEN521	Sense Byte 21, Format 5	(ECC Correction Pattern MSBs)
40A	01E	SEN522	Sense Byte 22, Format 5	(ECC Correction Pattern LSBs)
"	01F		Sense Byte 21, Format 6	
"	020	SEN208	Sense Byte 8, Format 2	
40B	021		Sense Byte 9, Format 2	
"	022	SEN210	Sense Byte 10, Format 2	
"	023	SEN211	Sense Byte 11, Format 2	
40C	024	SEN212	Sense Byte 12, Format 2	
"	025	SEN216	Sense Byte 16, Format 2	
"	026	NEXTCYL	Next Cylinder	
40D	027	NEXTHD	Next Head	

DISPLAY	ADDR.	LABEL	CONTENTS
"	028	NEXTREC	Next Record No.
"	029	RELREC	Relative Record no. (in MDB)
40E	02A	R5SAVE	R5 temp. save (various routines)
"	02B	STRTWD	Starting Word no.
"	02C	SKRETRY	Seek Error Retry Count
40F	02D	EFALLOW	E.F. Allowed Mask
"	02E	BITHIO	Bit for current HAIO
"	02F	ATTNHIO	Attention HAIO No. (-1)
410	030		Current Cylinder Drive 0
"	031		Current Cylinder Drive 1
"	032		Current Cylinder Drive 2
411	033		Current Cylinder Drive 3
"	034		Current Cylinder Drive 4
"	035		Current Cylinder Drive 5
412	036		Current Cylinder Drive 6
"	037		Current Cylinder Drive 7
"	038		Current Cylinder Drive 8
413	039		Current Cylinder Drive 9
"	03A		Current Cylinder Drive 10
"	03B		Current Cylinder Drive 11
414	03C		Current Cylinder Drive 12
"	03D		Current Cylinder Drive 13
"	03E		Current Cylinder Drive 14
415	03F		Current Cylinder Drive 15
"	040		Current Cylinder Drive 16
"	041		Current Cylinder Drive 17
416	042		Current Cylinder Drive 18
"	043		Current Cylinder Drive 19
"	044		Current Cylinder Drive 20
417	045		Current Cylinder Drive 21
"	046		Current Cylinder Drive 22
"	047		Current Cylinder Drive 23
418	048		Current Cylinder Drive 24
"	049		Current Cylinder Drive 25
"	04A		Current Cylinder Drive 26
419	04B		Current Cylinder Drive 27
"	04C		Current Cylinder Drive 28
"	04D		Current Cylinder Drive 29
41A	04E		Current Cylinder Drive 30
"	04F		Current Cylinder Drive 31
"	050		(spare)
41B	051	SKMASK	
"	052		Seek Complete Mask (1 bit per drive)
"	053		

DISPLAY	ADDR.	LABEL	CONTENTS
41C	054	SKPEND	
"	055		Seek Complete Pending (1 bit per drive)
"	056		
41D	057	SKHI01	
"	058		Seek Complete Pending HAIO-1 (1 bit per drive)
"	059		
41E	05A		
"	05B		Seek Complete Pending HAIO-2 (1 bit per drive)
"	05C		
41F	05D		
"	05E		Seek Complete Pending HAIO-3 (1 bit per drive)
"	05F		
420	060		
"	061		Seek Complete Pending HAIO-4 (1 bit per drive)
"	062		
421	063	SKILD	
"	064		ILD Seek Complete Pending (1 bit for ILD drive)
"	065		
422-424	066-06E		Reserved
425	06F	BITILD	
"	070		Bit for the ILD Drive (1 of 32)
"	071		
426	072	ATTN1	
"	073		Attention Pending HAIO-1 (1 bit per drive)
"	074		
427	075		
"	076		Attention Mask HAIO-1 (1 bit per drive)
"	077		
428	078	ATTN2	
"	079		Attention Pending HAIO-2 (1 bit per drive)
"	07A		
429	07B		
"	07C		Attention Mask HAIO-2 (1 bit per drive)
"	07D		
42A	07E	ATTN3	
"	07F		Attention Pending HAIO-3 (1 bit per drive)
"	080		
42B	081		
"	082		Attention Mask HAIO-3 (1 bit per drive)
"	083		
42C	084	ATTN4	
"	085		Attention Pending HAIO-4 (1 bit per drive)
"	086		

DISPLAY	ADDR.	LABEL	CONTENTS
42D	087		
"	088		Attention Mask HAIO-4 (1 bit per drive)
"	089		
42E	08A	BITDRV	
"	08B		Bit for Current Drive (1 of 32)
"	08C		
42F	08D	SKERRBIT	
"	08E		Seek Error Bit (1 bit per drive)
"	08F		
430	090	OVFLWBIT	
"	091		Error Usage Log overflow (1 bit per drive)
"	092		
431	093		Correctable Disk ECC History 1 (Cylinder)
"	094		Correctable Disk ECC History 1 (Head/Record)
"	095		Correctable Disk ECC History 1 (Count/Drive No.)
432	096		Correctable Disk ECC History 2 (Cylinder)
"	097		Correctable Disk ECC History 2 (Head/Record)
"	098		Correctable Disk ECC History 2 (Count/Drive No.)
433	099		
"	09A		Correctable Disk ECC Count
"	09B		
434	09C		Uncorrectable Disk ECC History 1 (Cylinder)
"	09D		Uncorrectable Disk ECC History 1 (Head/Record)
"	09E		Uncorrectable Disk ECC History 1 (Count/Drive No.)
435	09F		Uncorrectable Disk ECC History 2 (Cylinder)
"	0A0		Uncorrectable Disk ECC History 2 (Head/Record)
"	0A1		Uncorrectable Disk ECC History 2 (Count/Drive No.)
436	0A2		
"	0A3		Uncorrectable Disk ECC Count
"	0A4		
437	0A5	R5SAVEU	R5-Upper Temp. Save (ECC Correction)
"	0A6	PARCNT	XMC Parity Error Retry Count
"	0A7	ECCPAT	ECC Error Pattern
438	0A8	SMRTNA	SM-Error Return Loc. (MSB)
"	0A9	RDLNTHM	Initial Read Xfer. Length (MSBs)
"	0AA	RDLNTHL	Initial Read Xfer. Length (LSBs)
439	0AB	SMRTN	SM-Error Return Loc. (LSBs)
"	0AC	RBAU	
"	0AD	RBAL	Record Byte Address (Write)
43A	0AE	PADLNTH	Pad Zeros length (words)
"	0AF	ALTCYL	Alternate Cylinder
"	0BO	ALTHEAD	Alternate Head
43B	0B1		
"	0B2		Main ILD Display
"	0B3		

DISPLAY	ADDR.	LABEL	CONTENTS
43C	0B4	ILDDRV	ILD Drive No.
"	0B5	CURCYL	ILD Current Cylinder
"	0B6	CURHD	ILD Current Head
43D	0B7		(not used)
"	0B8	STCYL	ILD Start Cylinder
"	0B9	NDCYL	ILD Ending Cylinder
43E	0BA	ILDFLG	ILD Flags
"	0BB	STHD	ILD Start Head
"	0BC	NDHD	ILD Ending Head
43F	0BD	ILDNBR	ILD Test Number
"	0BE	RETURNA	
"	0BF	RETURN	ILD Wait Loop Return
440	0C0		
"	0C1		Drive 0 Error/Usage Log (Bytes Read)
"	0C2		(80,000,000-hex max.)
441	0C3		Drive 0 Error/Usage Log (Correctable ECC Count)
"	0C4		(200-hex max.)
"	0C5		Drive 0 Error/Usage Log (Uncorrectable ECC Count)
442	0C6		Drive 0 Error/Usage Log (Seek Count)
"	0C7		(8000-hex max.)
"	0C8		Drive 0 Error/Usage Log (Seek Error Count)
443	0C9		
"	0CA		Drive 1 Error/Usage Log (Bytes Read)
"	0CB		(80,000,000-hex max.)
444	0CC		Drive 1 Error/Usage Log (Correctable ECC Count)
"	0CD		(200-hex max.)
"	0CE		Drive 1 Error/Usage Log (Uncorrectable ECC Count)
445	0CF		Drive 1 Error/Usage Log (Seek Count)
"	0D0		(8000-hex max.)
"	0D1		Drive 1 Error/Usage Log (Seek Error Count)
446	0D2		
"	0D3		Drive 2 Error/Usage Log (Bytes Read)
"	0D4		(80,000,000-hex max.)
447	0D5		Drive 2 Error/Usage Log (Correctable ECC Count)
"	0D6		(200-hex max.)
"	0D7		Drive 1 Error/Usage Log (Uncorrectable ECC Count)
448	0D8		Drive 2 Error/Usage Log (Seek Count)
"	0D9		(8000-hex max.)
"	0DA		Drive 2 Error/Usage Log (Seek Error Count)
449	0DB		
"	0DC		Drive 3 Error/Usage Log (Bytes Read)
"	0DD		(80,000,000-hex max.)
44A	0DE		Drive 3 Error/Usage Log (Correctable ECC Count)

DISPLAY	ADDR.	LABEL	CONTENTS
"	0DF		(200-hex max.)
"	0E0		Drive 3 Error/Usage Log (Uncorrectable ECC Count)
44B	0E1		Drive 3 Error/Usage Log (Seek Count)
"	0E2		(8000-hex max.)
"	0E3		Drive 3 Error/Usage Log (Seek Error Count)
44C	0E4		
"	0E5		Drive 4 Error/Usage Log (Bytes Read)
"	0E6		(80,000,000-hex max.)
44D	0E7		Drive 4 Error/Usage Log (Correctable ECC Count)
"	0E8		(200-hex max.)
"	0E9		Drive 4 Error/Usage Log (Uncorrectable ECC Count)
44E	0EA		Drive 4 Error/Usage Log (Seek Count)
"	0EB		(8000-hex max.)
"	0EC		Drive 4 Error/Usage Log (Seek Error Count)
44F	0ED		
"	0EE		Drive 5 Error/Usage Log (Bytes Read)
"	0EF		(80,000,000-hex max.)
450	0F0		Drive 5 Error/Usage Log (Correctable ECC Count)
"	0F1		(200-hex max.)
"	0F2		Drive 5 Error/Usage Log (Uncorrectable ECC Count)
451	0F3		Drive 5 Error/Usage Log (Seek Count)
"	0F4		(8000-hex max.)
"	0F5		Drive 5 Error/Usage Log (Seek Error Count)
452	0F6		
"	0F7		Drive 6 Error/Usage Log (Bytes Read)
"	0F8		(80,000,000-hex max.)
453	0F9		Drive 6 Error/Usage Log (Correctable ECC Count)
"	0FA		(200-hex max.)
"	0FB		Drive 6 Error/Usage Log (Uncorrectable ECC Count)
454	0FC		Drive 6 Error/Usage Log (Seek Count)
"	0FD		(8000-hex max.)
"	0FE		Drive 6 Error/Usage Log (Seek Error Count)
455	0FF		
"	100		Drive 7 Error/Usage Log (Bytes Read)
"	101		(80,000,000-hex max.)
456	102		Drive 7 Error/Usage Log (Correctable ECC Count)
"	103		(200-hex max.)
"	104		Drive 7 Error/Usage Log (Uncorrectable ECC Count)
457	105		Drive 7 Error/Usage Log (Seek Count)
"	106		(8000-hex max.)
"	107		Drive 7 Error/Usage Log (Seek Error Count)
458	108		
"	109		Drive 8 Error/Usage Log (Bytes Read)
"			(80,000,000-hex max.)

DISPLAY	ADDR.	LABEL	CONTENTS
459	10B		Drive 8 Error/Usage Log (Correctable ECC Count)
"	10C		(200-hex max.)
"	10D		Drive 8 Error/Usage Log (Uncorrectable ECC Count)
45A	10E		Drive 8 Error/Usage Log (Seek Count)
"	10F		(8000-hex max.)
"	110		Drive 8 Error/Usage Log (Seek Error Count)
45B	111		
"	112		Drive 9 Error/Usage Log (Bytes Read)
"	113		(80,000,000-hex max.)
45C	114		Drive 9 Error/Usage Log (Correctable ECC Count)
"	115		(200-hex max.)
"	116		Drive 9 Error/Usage Log (Uncorrectable ECC Count)
45D	117		Drive 9 Error/Usage Log (Seek Count)
"	118		(8000-hex max.)
"	119		Drive 9 Error/Usage Log (Seek Error Count)
45E	11A		
"	11B		Drive 10 Error/Usage Log (Bytes Read)
"	11C		(80,000,000-hex max.)
45F	11D		Drive 10 Error/Usage Log (Correctable ECC Count)
"	11E		(200-hex max.)
"	11F		Drive 10 Error/Usage Log (Uncorrectable ECC Count)
460	120		Drive 10 Error/Usage Log (Seek Count)
"	121		(8000-hex max.)
"	122		Drive 10 Error/Usage Log (Seek Error Count)
461	123		
"	124		Drive 11 Error/Usage Log (Bytes Read)
"	125		(80,000,000-hex max.)
462	126		Drive 11 Error/Usage Log (Correctable ECC Count)
"	127		(200-hex max.)
"	128		Drive 11 Error/Usage Log (Uncorrectable ECC Count)
463	129		Drive 11 Error/Usage Log (Seek Count)
"	12A		(8000-hex max.)
"	12B		Drive 11 Error/Usage Log (Seek Error Count)
464	12C		
"	12D		Drive 12 Error/Usage Log (Bytes Read)
"	12E		(80,000,000-hex max.)
465	12F		Drive 12 Error/Usage Log (Correctable ECC Count)
"	130		(200-hex max.)
"	131		Drive 12 Error/Usage Log (Uncorrectable ECC Count)
466	132		Drive 12 Error/Usage Log (Seek Count)
"	133		(8000-hex max.)
"	134		Drive 12 Error/Usage Log (Seek Error Count)
467	135		
"	136		Drive 13 Error/Usage Log (Bytes Read)

DISPLAY	ADDR.	LABEL	CONTENTS
"	137		(80,000,000-hex max.)
468	138		Drive 13 Error/Usage Log (Correctable ECC Count)
"	139		(200-hex max.)
"	13A		Drive 13 Error/Usage Log (Uncorrectable ECC Count)
469	13B		Drive 13 Error/Usage Log (Seek Count)
"	13C		(8000-hex max.)
"	13D		Drive 13 Error/Usage Log (Seek Error Count)
46A	13E		
"	13F		Drive 14 Error/Usage Log (Bytes Read)
"	140		(80,000,000-hex max.)
46B	141		Drive 14 Error/Usage Log (Correctable ECC Count)
"	142		(200-hex max.)
"	143		Drive 14 Error/Usage Log (Uncorrectable ECC Count)
46C	144		Drive 14 Error/Usage Log (Seek Count)
"	145		(8000-hex max.)
"	146		Drive 14 Error/Usage log (Seek Error Count)
46D	147		
"	148		Drive 15 Error/Usage Log (Bytes Read)
"	149		(80,000,000-hex max.)
46E	14A		Drive 15 Error/Usage Log (Correctable ECC Count)
"	14B		(200-hex max.)
"	14C		Drive 15 Error/Usage Log (Uncorrectable ECC Count)
46F	14D		Drive 15 Error/Usage Log (Seek Count)
"	14E		(8000-hex max.)
"	14F		Drive 15 Error/Usage Log (Seek Error Count)
470	150		
"	151		Drive 16 Error/Usage Log (Bytes Read)
"	152		(80,000,000-hex max.)
471	153		Drive 16 Error/Usage Log (Correctable ECC Count)
"	154		(200-hex max.)
"	155		Drive 16 Error/Usage Log (Uncorrectable ECC Count)
472	156		Drive 16 Error/Usage Log (Seek Count)
"	157		(8000-hex max.)
"	158		Drive 16 Error/Usage Log (Seek Error Count)
473	159		
"	15A		Drive 17 Error/Usage Log (Bytes Read)
"	15B		(80,000,000-hex max.)
474	15C		Drive 17 Error/Usage Log (Correctable ECC Count)
"	15D		(200-hex max.)
"	15E		Drive 17 Error/Usage Log (Uncorrectable ECC Count)
475	15F		Drive 17 Error/Usage Log (Seek Count)
"	160		(8000-hex max.)
"	161		Drive 17 Error/Usage Log (Seek Error Count)
476	162		

DISPLAY	ADDR.	LABEL	CONTENTS
"	163		Drive 18 Error/Usage Log (Bytes Read)
"	164		(80,000,000-hex max.)
477	165		Drive 18 Error/Usage Log (Correctable ECC Count)
"	166		(200-hex max.)
"	167		Drive 18 Error/Usage Log (Uncorrectable ECC Count)
478	168		Drive 18 Error/Usage Log (Seek Count)
"	169		(8000-hex max.)
"	16A		Drive 18 Error/Usage Log (Seek Error Count)
479	16B		
"	16C		Drive 19 Error/Usage Log (Bytes Read)
"	16D		(80,000,000-hex max.)
47A	16E		Drive 19 Error/Usage Log (Correctable ECC Count)
"	16F		(200-hex max.)
"	170		Drive 19 Error/Usage Log (Uncorrectable ECC Count)
47B	171		Drive 19 Error/Usage Log (Seek Count)
"	172		(8000-hex max.)
"	173		Drive 19 Error/Usage Log (Seek Error Count)
47C	174		
"	175		Drive 20 Error/Usage Log (Bytes Read)
"	176		(80,000,000-hex max.)
47D	177		Drive 20 Error/Usage Log (Correctable ECC Count)
"	178		(200-hex max.)
"	179		Drive 20 Error/Usage Log (Uncorrectable ECC Count)
47E	17A		Drive 20 Error/Usage Log (Seek Count)
"	17B		(8000-hex max.)
"	17C		Drive 20 Error/Usage Log (Seek Error Count)
47F	17D		
"	17E		Drive 21 Error/Usage Log (Bytes Read)
"	17F		(80,000,000-hex max.)
480	180		Drive 21 Error/Usage Log (Correctable ECC Count)
"	181		(200-hex max.)
"	182		Drive 21 Error/Usage Log (Uncorrectable ECC Count)
481	183		Drive 21 Error/Usage Log (Seek Count)
"	184		(8000-hex max.)
"	185		Drive 21 Error/Usage Log (Seek Error Count)
482	186		
"	187		Drive 22 Error/Usage Log (Bytes Read)
"	188		(80,000,000-hex max.)
483	189		Drive 22 Error/Usage Log (Correctable ECC Count)
"	18A		(200-hex max.)
"	18B		Drive 22 Error/Usage Log (Uncorrectable ECC Count)
484	18C		Drive 22 Error/Usage Log (Seek Count)
"	18D		(8000-hex max.)
"	18E		Drive 22 Error/Usage Log (Seek Error Count)

DISPLAY	ADDR.	LABEL	CONTENTS
485	18F		
"	190		Drive 23 Error/Usage Log (Bytes Read)
"	191		(80,000,000-hex max.)
486	192		Drive 23 Error/Usage Log (Correctable ECC Count)
"	193		(200-hex max.)
"	194		Drive 23 Error/Usage Log (Uncorrectable ECC Count)
487	195		Drive 23 Error/Usage Log (Seek Count)
"	196		(8000-hex max.)
"	197		Drive 23 Error/Usage Log (Seek Error Count)
488	198		
"	199		Drive 24 Error/Usage Log (Bytes Read)
"	19A		(80,000,000-hex max.)
489	19B		Drive 24 Error/Usage Log (Correctable ECC Count)
"	19C		(200-hex max.)
"	19D		Drive 24 Error/Usage Log (Uncorrectable ECC Count)
48A	19E		Drive 24 Error/Usage Log (Seek Count)
"	19F		(8000-hex max.)
"	1A0		Drive 24 Error/Usage Log (Seek Error Count)
48B	1A1		
"	1A2		Drive 25 Error/Usage Log (Bytes Read)
"	1A3		(80,000,000-hex max.)
48C	1A4		Drive 25 Error/Usage Log (Correctable ECC Count)
"	1A5		(200-hex max.)
"	1A6		Drive 25 Error/Usage Log (Uncorrectable ECC Count)
48D	1A7		Drive 25 Error/Usage Log (Seek Count)
"	1A8		(8000-hex max.)
"	1A9		Drive 25 Error/Usage Log (Seek Error Count)
48E	1AA		
"	1AB		Drive 26 Error/Usage Log (Bytes Read)
"	1AC		(80,000,000-hex max.)
48F	1AD		Drive 26 Error/Usage Log (Correctable ECC Count)
"	1AE		(200-hex max.)
"	1AF		Drive 26 Error/Usage Log (Uncorrectable ECC Count)
490	1B0		Drive 26 Error/Usage Log (Seek Count)
"	1B1		(8000-hex max.)
"	1B2		Drive 26 Error/Usage Log (Seek Error Count)
491	1B3		
"	1B4		Drive 27 Error/Usage Log (Bytes Read)
"	1B5		(80,000,000-hex max.)
492	1B6		Drive 27 Error/Usage Log (Correctable ECC Count)
"	1B7		(200-hex max.)
"	1B8		Drive 27 Error/Usage Log (Uncorrectable ECC Count)
493	1B9		Drive 27 Error/Usage Log (Seek Count)
"	1BA		(8000-hex max.)

DISPLAY	ADDR.	LABEL	CONTENTS
"	1BB		Drive 27 Error/Usage Log (Seek Error Count)
494	1BC		
"	1BD		Drive 28 Error/Usage Log (Bytes Read)
"	1BE		(80,000,000-hex max.)
495	1BF		Drive 28 Error/Usage Log (Correctable ECC Count)
"	1C0		(200-hex max.)
"	1C1		Drive 28 Error/Usage Log (Uncorrectable ECC Count)
496	1C2		Drive 28 Error/Usage Log (Seek Count)
"	1C3		(8000-hex max.)
"	1C4		Drive 28 Error/Usage Log (Seek Error Count)
497	1C5		
"	1C6		Drive 29 Error/Usage Log (Bytes Read)
"	1C7		(80,000,000-hex max.)
498	1C8		Drive 29 Error/Usage Log (Correctable ECC Count)
"	1C9		(200-hex max.)
"	1CA		Drive 29 Error/Usage Log (Uncorrectable ECC Count)
499	1CB		Drive 29 Error/Usage Log (Seek Count)
"	1CC		(8000-hex max.)
"	1CD		Drive 29 Error/Usage Log (Seek Error Count)
49A	1CE		
"	1CF		Drive 30 Error/Usage Log (Bytes Read)
"	1D0		(80,000,000-hex max.)
49B	1D1		Drive 30 Error/Usage Log (Correctable ECC Count)
"	1D2		(200-hex max.)
"	1D3		Drive 30 Error/Usage Log (Uncorrectable ECC Count)
49C	1D4		Drive 30 Error/Usage Log (Seek Count)
"	1D5		(8000-hex max.)
"	1D7		Drive 30 Error/Usage Log (Seek Error Count)
49D	1D7		
"	1D8		Drive 31 Error/Usage Log (Bytes Read)
"	1D9		(80,000,000-hex max.)
49E	1DA		Drive 31 Error/Usage Log (Correctable ECC Count)
"	1DB		(200-hex max.)
"	1DC		Drive 31 Error/Usage Log (Uncorrectable ECC Count)
49F	1DD		Drive 31 Error/Usage Log (Seek Count)
"	1DE		(8000-hex max.)
"	1DF		Drive 31 Error/Usage Log (Seek Error Count)
4A0	1E0		
"	1E1		Reserved for Error/Usage Log assembly
"	1E2		
4A1	1E3		
"	1E4		Reserved for Error/Usage Log assembly
"	1E5		
4A2	1E6		

DISPLAY	ADDR.	LABEL	CONTENTS
"	1E7		Reserved for Error/Usage Log assembly
"	1E8		
4A3	1E9		
"	1EA		Reserved for Error/Usage Log assembly
"	1EB		
4A4	1EC	RETURN1	ILD Return Location 1
"	1ED	RETURN2	ILD Return Location 2
"	1EE	RETURN3	ILD Return Location 3
4A5	1EF	MSGFLG	ILD Message Sent & Loop Flags
"	1F0	ILDCONTA	ILD Continuation Location (MSB)
"	1F1	ILDCONT	ILD Continuation Location (LSB)
4A6	1F2	R15SAVL	ILD R14 Temp. Save
"	1F3	R15SAVU	ILD R15-upper Temp. Save
"	1F4	R15SAVL	ILD R15-lower Temp. Save
4A7	1F5	OCPCMD	ILD OCP Command
"	1F6	PARAM1	ILD OCP Parameter 1
"	1F7	PARAM2	ILD OCP Parameter 2
4A8	1F8	RETURN1A	ILD Return 1 (MSB)
"	1F9	RETURN2A	ILD Return 2 (MSB)
"	1FA	RETURN3A	ILD Return 3 (MSB)
4A9	1FB	PASCNT1	
"	1FC	PASCNT	Wait Loop Pass Counter
"	1FD	SEEDWRD	Random Seek Test Seed Word
4AA	1FE	SAVCYL	ILD Next Cylinder temp. save
"	1FF	SAVHD	ILD Next Head/Record temp. save
"	200	R5RAT	R5 temp. save during Seek Processing
4AB	201		(not used)
"	202	NEWDRV	Read (Function) Drive No.
"	203	OLDDRV	Write (Pushed-off) Drive No.
4AC	204	FLAGSAV	Status Flags
"	205	LASTDRV	Last Drive Selected
"	206	URELREC	U-Side Relative Record No.
4AD	207		Call to FRBHAND if FRB Error
"	208	BADCNT	Count of tracks unable to write back
"	209		Pass Counter (Short Backscan)
4AE	20A	MAXCYLI	ILD Max. Usable Cylinder
"	20B		
"	20C		Pushed-off Tracks Count
4AF	20D	MAXHDI	ILD Max. Head
"	20E		
"	20F		Backscan Seek Tracks Count
4B0	210		ILD Sense Byte 0
"	211		ILD Sense Byte 1
"	212		ILD Sense Byte 2

DISPLAY	ADDR.	LABEL	CONTENTS	
4B1	213		ILD Sense Byte 3	(Recovery Action)
"	214		ILD Sense Byte 4	(Drive Physical I.D.)
"	215		ILD Sense Byte 5	(Emulated Cyl. LSBs)
4B2	216		ILD Sense Byte 6	(Emulated Cyl. MSBs/Head)
"	217		ILD Sense Byte 7	(Error Format/Message)
"	218		ILD Sense Byte 8, Format 1	
4B3	219		ILD Sense Byte 9, Format 1	
"	21A		ILD Sense Byte 10, Format 1	
"	21B		ILD Sense Byte 11, Format 1	
4B4	21C		ILD Sense Byte 12, Format 1	
"	21D		ILD Sense Byte 13, Format 1,2	(Physical Drive No.)
"	21E		ILD Sense Byte 14, Format 1,2	(Drive Status)
4B5	21F		ILD sense Byte 15, Format 1,2	
"	220		ILD Sense Byte 21, Format 1,2	
"	221		ILD Sense Byte 8, Format 4,5	(Actual Cyl. MSBs)
4B6	222		ILD Sense Byte 9, Format 4,5	(Actual Cyl. LSBs)
"	223		ILD Sense Byte 10, Format 4,5	
"	224		ILD Sense Byte 11, Format 4,5	(Actual Head No.)
4B7	225		ILD Sense Byte 12, Format 4,5	(Actual Record No.)
"	226		ILD Sense Byte 13, Format 4,5	
"	227		ILD Sense Byte 14, Format 4,5	
4B8	228		ILD Sense Byte 15, Format 4	(SM-Error Retry Count)
"	229		ILD Sense Byte 16, Format 4	(Drive Physical I.D.)
"	22A		ILD Sense Byte 15, Format 5	
4B9	22B		ILD Sense Byte 16, Format 5	
"	22C		ILD Sense Byte 17, Format 5	
"	22D		ILD Sense Byte 21, Format 5	(ECC Correction MSBs)
4BA	22E		ILD sense Byte 22, Format 5	(ECC Correction LSBs)
"	22F		ILD Sense Byte 21, Format 6	
"	230		ILD Sense Byte 8, Format 2	
4BB	231		ILD Sense Byte 9, Format 2	
"	232		ILD sense Byte 10, Format 2	
"	233		ILD Sense Byte 11, Format 2	
4BC	234		ILD Sense Byte 12, Format 2	
"	235		ILD Sense Byte 16, Format 2	
"	236		(scratch)	
4BD	237		Pushed-off Track Upper Address	
"	238		Pushed-off Track Lower Address	
"	239	SEEKFLG	Seek Only flag	
4BE	23A	SAVREC	ILD Next Record temp. save	
"	23B	RETURN4A	ILD Return 4 (MSBs)	
"	23C	RETURN4	ILD Return 4 (LSBs)	
4BF	23D	R5SAVU	R5-upper Save if ILD error	
"	23E	R5SAVL	R5-lower Save if ILD error	

DISPLAY	ADDR.	LABEL	CONTENTS
"	23F	SAV415	ILD Error Retry Count temp. save
4C0	240	MAINRETU	
"	241	MAINRETL	READ1TRK & WRIT1TRK Main Return Location
"	242	CASHSTAT	Caching Status
4C1	243	RATRETU	
"	244	RATRETL	Caching Read/Write Return Location
"	245	MAXCYLDI	ILD Max. Drive Cylinder
4C2	246	SAVCYL	Save Cylinder before Caching
"	247	SAVHED	Save Head before Caching
"	248	SAVSTRWL	Save Start Word No. before Caching
4C3	249	SAVER15	R15 Save thru Read & Write One Track
"	24A	SAVXFRU	Save Transfer Length (upper) before Caching
"	24B	SAVXFRL	Save Transfer Length (lower) before Caching
4C4	24C	SKSTART	Seek Started Flag
"	24D	SAVEREC	Save Record before caching
"	24E	CACHECNT	Caching Retry Counter
4C5	24F	SAVER14U	Save R14-upper before Caching
"	250	SAVER14L	Save R14-lower before Caching
"	251		(Not Used)
4C6	252	SAVEQU	Save Cache Cyl. before Caching
"	253	SAVEQL	Save cache Unit/head before Caching
"	254	SAVER2	Save Cache Track No. before Caching
4C7	255	ECCSTAT	IAS ECC Status
"	256	SAVECYL	Save Cylinder for track to cache
"	257	SAVEHEAD	Save Unit/head for track to cache
4C8	258	SAVE05	Emulated Cylinder Save (8 LSBs)
"	259	SAVE06	Emulated Cyl. (MSBs) & Head Save
"	25A	SAVE2B	Emulated Record Save
4C9	25B	WAITRETU	Return Loc. from WAITSEEK (MSBs)
"	25C	INITADRH	Initial Cache Addr. (MSBs)
"	25D	INITADRL	Initial Cache Addr. (LSBs)
4CA	25E	SAVUREC	Saved Emulated Record No.
"	25F		R10 temp. save (Ending)
"	260	COMMAND	OCP Command
4CB	261	REQUNIT	Requested Unit
"	262	REQSTATE	Requested State
"	263	PRSSTATE	Present State
4CC	264	CSTART	1/2 Cache Disk Lowest Address (MSBs)
"	265	CMDADDRU	
"	266	CMDADDRL	Command Relative Address
4CD	267		(Not Used)
"	268	UADDRU	Saved next U-start Address MSBs
"	269	UADDRL	Saved next U-start Address LSBs
4CE	26A	FORDAT3	

DISPLAY	ADDR.	LABEL	CONTENTS
"	26B	FORDAT2	Format & Cache prep. Data
"	26C	FORDAT1	
4CF	26D	BADDAT3	ILD-4 Bad read Data bits 24-35
"	26E	BADDAT2	ILD-4 Bad read Data bits 12-23
"	26F	BADDAT1	ILD-4 Bad Read Data bits 0-11
4D0	270		
"	271		Last E.F.
"	272		
4D1	273		
"	"		Previous E.F.s
4D6	284		
4D7	285		
"	286		E.F. Count
"	287		
4D8	288		
"	289		Last E.F. Address
"	28A		
4D9	28B		
"	"		Previous E.F. Addresses
4DE	29C		
4DF	29D		(Not Used)
"	29E		(Not Used)
"	29F		(Not Used)
4E0	2A0		
"	2A1		Last E.I.
"	2A2		
4E1	2A3		
"	"		Previous E.I.s
4E6	2B4		
4E7	2B5		DRONCYL
"	2B6		Drive on Cylinder (1 bit per drive)
"	2B7		
4E8	2B8		
"	2B9		Last Channel Sense 0-3
"	2BA		
4E9	2BB		
"	2BC		Last Channel Sense 4-7
"	2BD		

DISPLAY	ADDR.	LABEL	CONTENTS
4EA	2BE		
"	2BF		Last Channel Sense 8-11
"	2C0		
4EB	2C1		
"	2C2		Last Channel Sense 12-15
"	2C3		
4EC	2C4		
"	2C5		Last Channel Sense 16-19
"	2C6		
4ED	2C7		
"	2C8		Last Channel sense 20-23
"	2C9		
4EE	2CA	MAXCYLU	Max. Emulated Cylinder
"	2CB	MAXHDU	Max. Emulated Head
"	2CC	MAXREC	Max. Emulated Record No.
4EF	2CD	RECLNTH	Record Length - words (112, 448, 1792)
"	2CE	HDMULTU	1/4 Emulated Head Multiplier
"	2CF	BUFCAP	1/4 HSSM Buffer Capacity
4F0	2D0	MAXREL	Max. Relative Record No.
"	2D1	CYLDIVUM	
"	2D2	CYLDIVUL	1/4 Emulated Cylinder Divisor
4F1	2D3	MAXCYLA	Max. Emulated Usable Cylinder
"	2D4	MAXCYLD	Max. Emulated Drive Cylinder
"	2D5	MAXHDA	Max. Emulated Drive Head
4F2	2D6	AMPREC	Max. Emulated Record No.
"	2D7	CYLDIVAM	
"	2D8	CYLDIVAL	1/4 Emulated Cylinder Divisor
4F3	2D9	WRDSTRK	1/4 Words per Track
"	2DA	WRDSMAX	1/4 Max. Words per Track
"	2DB	RECSREAD	Records Read
4F4	2DC	SMTIME	SM-timer (LSBs)
"	2DD	UTIME	U-timer (LSBs)
"	2DE	UREC	Emulated Record No.
4F5	2DF	LIMIT1	
"	2E0	LIMIT2	Max. Relative Word No.
"	2E1	LIMIT3	
4F6	2E2	SMTIMEA	SM-timer (MSBs)
"	2E3	UTIMEA	U-timer (MSBs)
"	2E4	IRPRTNA	SM-done Interrupt Processing...
4F7	2E5	IRPRTN	Normal Return loc.
"	2E6	ADVLOC	Adv. to Next Record Jump location
"	2E7	SAVXMCJ	Saved Next XMCI Jump Command

SCRATCH PAD MEMORY

DISPLAY	ADDR.	LABEL	CONTENTS	
4F8	2E8	SAVR1U	R1-upper save	
"	2E9	SAVR1L	R1-lower save	
"	2EA	SAVR2	R2 save	(routine CHKAVAL)
4F9	2EB	SAVR3	R3 save	(routine CHKAVAL)
"	2EC	SAVR5U	R5-upper save	(routine CHKAVAL)
"	2ED	SAVR5L	R5-lower save	(routine CHKAVAL)
4FA	2EE	SAVQU	Q-upper save	(routine CHKAVAL)
"	2EF	SAVQL	Q-lower save	(routine CHKAVAL)
"	2F0	INITRETU	INITSEEK Return location (MSBs)	
4FB	2F1	WAITRETL	WAITSEEK Return location (LSBs)	
"	2F2	SAVR6	R6 save	(routine CHKAVAL)
"	2F3	HOLDCNT	Track Held Counter	
4FC	2F4	TWODRIV	Two Drives per Unit flag	
"	2F5	WMAFLG	WMA ECC Test flags	
"	2F6	INITRET	INITSEEK Return location (LSBs)	
"	2F7	CSEN05	Initial Emulated cyl. LSBs (Conversion)	
"	2F8	CSEN06	Initial Emulated cyl. MSBs/Head (Conversion)	
"	2F9	CWORD	Initial Word Number (Conversion)	
4FE	2FA	CSEN408	Initial Actual cyl. MSBs (Conversion)	
"	2FB	CSEN409	Initial Actual cyl. LSBs (Conversion)	
"	2FC	CSEN411	Initial Actual Head no. (Conversion)	
4FF	2FD	CSEN412	Initial Actual Record (Conversion)	
"	2FE	RETURN5A	\	
"	2FF	RETURN5	ILD Return 5	
500	300	CACHADDR	Cache Addr. Search Argument	
"	301		(Not Used)	
"	302	SCAN	Current FRB Scan Pointer	
501	303	FRBUNIT	FRB Scan Unit No.	
"	304	FILEMAX	Value of FILEMAX	
"	305	FRBADDR	Current FRB Address	
502	306	FRBFNCT	FRB Function	
"	307	FRBWRTST	FRB Write Error History (cumulative)	
"	308	FRBWRTER	FRB Write Error Count	
503	309	FSTAT	FRB Status	
"	30A	FRBRETU		
"	30B	FRBRET	FRB Handler Return location	
504	30C	STATUS	WMA Status	
"	30D	WMARETU		
"	30E	WMARET	WMA Handler Return location	
505	30F	PREPRTNA	Cache Prep. Return location (MSB)	
"	310	INITDEV	Initial WMA Device No.	
"	311	FUNCTWRD	WMA Handler Function Word	
506	312	STRTDEV	WMA Starting Device No.	
"	313	STRTADRH	WMA Starting Address (MSBs)	
"	314	STRTADRL	WMA start Address (LSBs)	

DISPLAY	ADDR.	LABEL	CONTENTS	
507	315	WMCSTAT0	Last WMC Status if error	
"	316	ERRSTAT1	Last WMA Error Status 1	
"	317	ERRSTAT2	Last WMA Error Status 2	
508	318	PREPRTN	Cache Prep. return loc. (LSBs)	
"	319	XFRLNTHU	Cache Xfer. Length (4 MSBs)	
"	31A	SFRLENTH	Cache Xfer. Length (12 LSBs)	
509	31B		Lamp Test (all ones)	
"	31C		Lamp Test (all ones)	
"	31D		Lamp Test (all ones)	
50A	31E	FRBRTCNT	FRB Write Error Retry Count	
"	31F	FRBRDST	FRB Read Error status (cumulative)	
"	320	FRBRDERR	FRB Read Error Count	
50B	321	ERRDEV	WMA Error Device No.	35-24 Device Address
"	322	ERRADRH	WMA Error Address (MSBs)	23-21 Group Address
"	323	ERRADRL	WMA Error Address (LSBs)	
50C	324	ERRDEVC	WMC Error Device No.	32-24 Device Address
"	325	ERRADRHC	WMC Error address (MSBs)	23-21 Group Address
"	326	ERRADRLC	WMC Error address (LSBs)	
50D	327	FRBR2B	FRB bad data (Track No.)	
"	328	FRBR1UB	FRB bad data (Cylinder)	
"	329	FRBR1LB	FRB bad data (Unit/Head)	
50E	32A	FRBR3B	FRB bad data (Flags)	
"	32B	FRBRTRY	FRB Read Error Retry Count	
"	32C	FRBR3	FRB Write data (Flags)	
50F	32D	FRBR2	FRB Write data (Track No.)	
"	32E	FRBR1U	FRB Write data (Cylinder)	
"	32F	FRBR1L	FRB Write data (Unit/Head)	
510	330	CORECCLG		
"	"		Correctable WMA ECC Error Log	
516	344			
517	345			
"	346		Correctable WMA ECC Count	
"	347	CORRCNT		
518	348	ECCTEMP		
"	"		Disk ECC Error assembly word	
"	34A			
519	34B		(Not Used)	
"	34C	ECCADR	Last ECC Address from WMA (ECCADDR)	
"	34D	ECCDISP	Last ECC Displacement from WMA (ECCDISPL)	
51A	34E	SECMASK	Sector Polling Mask [1 bit per drive]	
51F	35F		Sector Polling Mask [1 bit per drive]	
"	350		Sector Polling Mask [1 bit per drive]	
51B	351	NEXTSMU	Next SM-DMA Address (MSBs)	
"	352	NEXTSML	Next SM-DMA Address (LSBs)	
"	353		(Not Used)	

DISPLAY	ADDR.	LABEL	CONTENTS
51C	354	DMABADU	Bad SM-DMA Address (MSBs) if error
"	355	DMABADL	Bad SM-DMA Address (LSBs if error
"	356		(Not Used)
51D	357	DMAGOODU	Expected SM-DMA Address (MSBs) if error
"	358	DMAGOODL	Expected SM-DMA Address (LSBs) if error
"	359	OVCOPY	Only Valid Copy flag
51E	35A	UDMBADU	Bad U-DMA Address (MSBs) if error
"	35B	UDMBADL	Bad U-DMA Address (LSBs) if error
"	35C	URDDMAU	Ending U-DMA Address MSBs (Read Data)
51F	35D	UDMGOODU	Expected U-DMA Address (MSBs) if error
"	35E	UDMGOODL	Expected U-DMA Address (LSBs) if error
"	35F	URDDMAL	Ending U-DMA Address LSBs (Read Data)
520	360	ERLOCLOG	
"	"		Uncorrectable WMA ECC Error Log
526	374		
527	375		
"	376		Uncorrectable WMA ECC Count
"	377	UNCORCNT	
528	378		
"	"		Saved Drive Flags (per drive)
532	397		
"	398		Saved Drive Flag (Data Copy Drive)
533	399		SSS max Unit Size (megawords)
"	39A		(Not Used)
535	3A1		(Not Used)
536	3A2	UNITHD	
"	"		Saved Unit/Head for each drive
540	3C1		
541	3C3	TRKNBR	
"	"		FRB Track No. for each drive
54B	3E3		
54C	3E4	DLAYDE	Device End Delay Timer
"	3E5	LASTFLG	Last Drive Flags
"	3E6	RECSAV	Record save for WRITPART
54D	3E7	HDSAV	Head save for WRITPART
"	3E8	XFRLUSAV	Xfer. Length MSBs for WRITPART
"	3E9	XFRLLSAV	Xfer. Length LSBs for WRITPART
54E	3EA	STRWDSAV	Start Word No. Save for WRITPART
"	3EB	SAVER12	R12 temp. save
"	3EC	SAVER9	R9 temp. save
54F	3ED	AFTRINDX	1st Record after Index
"	3EE		Backscan Seek Hold-Off Counter (Secondary)
"	3EF	TRKCNTR	Track Counter (FRB Handler)

SCRATCH PAD MEMORY

DISPLAY	ADDR.	LABEL	CONTENTS
550	3F0	WORD0	HSSM Confidence Test Ref. Word 0
"	3F1		HSSM Confidence Test Ref. Word 0
"	3F2		HSSM Confidence Test Ref. Word 0
551	3F3		HSSM Confidence Test Ref. Word 1
"	3F4		HSSM Confidence Test Ref. Word 1
"	3F5		HSSM Confidence Test Ref. Word 1
552	3F6		HSSM Confidence Test Ref. Word 2
"	3F7		HSSM Confidence Test Ref. Word 2
"	3F8		HSSM Confidence Test Ref. Word 2
553	3F9		HSSM Confidence Test Ref. Word 3
"	3FA		HSSM Confidence Test Ref. Word 3
"	3FB		HSSM Confidence Test Ref. Word 3
554	3FC		(Not Used)
"	3FD		(Not Used)
"	3FE		(Not Used)
555	3FF	CSW	Confidence Test error bits (1 bit per board)

6.4.3 Interface Specifications

Note: The SCP is a separately addressable part of the OCPM board.

Module Addresses: SCP: H#3
OCPM: H#7

SCP CONTROL TERMS

Mnemonic	Meaning	Hexadecimal Representation			
CPSTCLR	CT bus, parity, error reset	3	0	8	0
MPPGCLR	Reset pushbutton register	3	0	C	0
RPOWFLG	Reset power-on flag	3	0	D	0

SCP READ REGISTERS

Mnemonic	Meaning	Hexadecimal Representation			
PRGCPB	Prog. control buttons	3	X	0	R0-R15
PRGTGL	Prog. control switches	3	X	1	↓
MODESW	Mode switches	3	X	2	
PGRMSEL	Thumbwheel switches	3	X	3	
DATSW1	Data switches 0-11	3	X	4	
DATSW2	Data switches 12-23	3	X	5	
DATSW3	Data switches 24-35	3	X	6	

SCP WRITE REGISTERS

Mnemonic	Meaning	Hexadecimal Representation			
LDPRGD	Load Prog. Disp. register	3	4	X	X
LDDISP1	Display bits 24-35	3	5	X	X
LDDISP2	Display bits 12-23	3	6	X	X
LDDISP3	Display bits 0-11	3	7	X	X

Figure 6-36
SCP Read/Write/Control Functions

OCPM CONTROL TERMS

Mnemonic	Meaning	Hexadecimal Representation			
SCMDACT	Set command active	7	1	4	0
RCMDACT	Reset command active	7	0	4	0
SRESRV	Set reserve	7	1	2	0
RRESRV	Reset reserve	7	0	2	0
OCPRST	Reset OCP	7	8	0	0
OCPDSEL	Reset and deselect OCP	7	C	0	0
OCPREQ	Request OCP	7	0	0	0
SDATCOPY	Set Data Copy Mode (green light)	7	1	1	0
RDATCOPY	Clear Data Copy Mode	7	0	1	0
SSAFE	Set Data Copy Safe to Power	7	1	1	1
RSAFE	Reset Data Copy Safe	7	0	1	1

OCPM READ REGISTERS

Mnemonic	Meaning	Hexadecimal Representation			
OCPSTAT	OCP Status	7	F	0	RX
OCPDATA	OCP Buffer Data	7	F	1	RX

OCPM WRITE REGISTERS

Mnemonic	Meaning	Hexadecimal Representation			
OCPADR	OCP Buffer Address	7	0	X	X
OCPDATA	OCP Buffer Data	7	1	X	X

Figure 6-37
OCPM Read/Write/Control Functions

6.5.3 Interface Specifications

HIGH SPEED DISK INTERFACE

WRITE COMMANDS

Mnemonic	Equ.	File Register Addrress	Meaning
			(Board Decode = H#1 (HSSM))
LDSARL	0	0	Load SM-start Addr. (8 LSBs)
LDSARM	1	1	Load SM-start Addr. (8 MSBs)
LDSBCL	2	2	Load SM-byte Count (8 LSBs) (Note 1)
LDSBCM	3	3	Load SM-byte Count (8 MSBs) (Note 1)
LDUARL	4	4	Load U-start Address (8 LSBs)
LDUARM	5	5	Load U-start Address (8 MSBs)
LDUBCL	6	6	Load U-byte Count (8 LSBs) (Note 2)
LDUBCM	7	7	Load U-byte Count (8 MSBs)
LDRTPTR	8	D	Load Drive Type Pointer (8 bits)
LDDRFLG	9	8	Load Header Flag Byte
LDDRCYL	A	9	Load Header Cylinder (8 LSBs)
LDDRCYM	B	A	Load Header Cylinder (8 MSBs)
LDDRHD	C	B	Load Header Head (5 bits)
LDDRREC	D	C	Load Header Record (7 bits)
LDDRUSEL	E		Load Unit Select Req. (7 bits)
LDXMCJ	F	F	Load MPC Jump Reg. (8 bits)
			(Board Decode = 2 (HSSMA))
LDMDARL	0		Load Memory Data Buffer Address (8 LSBs)
LDMDARM	1		Load Memory Data Buffer Address (8 MSBs)
LDDRBO	2		Load Drive Bus Out Reg. (11 bits)
LDMDAT	3		Load Memory Data Buffer Data (8 bits) (Note 3)
LDECTLR	4		Load ECC Control Reg. (8 bits)

Note 1: Also Format Record Length (bytes)
Note 2: Number of Records to Format
Note 3: Increments Memory Data Buffer Address

CONTROL COMMANDS

(Board Decode = 1 (HSSM))

Mnemonic	Equ.	Meaning
DIFRST	000	Reset Disk Interface Error Status
DIFSELR	001	Disk Interface Selective reset (not used)
RSDIPER	002	Reset Disk Interface Parity Error
MPCRST	003	Reset MPC Control Reg.
MSEQRST	004	Reset MPC Micro-sequencer/Reset SM/U Done Intr
MDBRST	005	YMC Continue
WRTCONT	006	Write Continue
SETUSEL	007	Set Unit Select tag/Reset SM Intr (Compl.)
SETAG1	008	Set Tag 1 (Set Cylinder)
SETAG2	009	Set Tag 2 (Set Head)
SETAG3	00A	Set Tag 3 (Control)
RSTUSEL	00B	Reset Unit Select tag
RSXMPER	00C	Reset XMCI Parity Error
XMCJCMD	00D	Execute MPC Jump to Jump Reg. (Note 1)
ECCCK	00F	Clock ECC Chip (Note 2)
SETECTLR	010	Enable XMCI Control Reg. to ECC chip
RSECTLR	011	Disable XMCI Control reg. from ECC chip
RSTAG1	012	Reset Tag 1
RSTAG2	013	Reset Tag 2
RSTSIRPT	014	Reset SM-done Interrupt
RSTUIRPT	015	Reset U-done Interrupt
RSTAG3	016	Reset Tag 3
SETBUSY	017	Set Interface Busy Flag
SETAG4	018	Set Tag 4 (Read Sector)
RSTAG4	019	Reset Tag 4

Note 1: Jump Register must be previously loaded (LDXMCJ)
Note 2: The command must be executed 3 times to be ONE valid ECC chip clock.

READ COMMANDS

Mnemonic	Equ.	File Register Addr.	Meaning
			(Board Decode = 1 (HSSM))
RDSARL	00		Read Current SM-addr. (8 LSBs) (not used) *
RDSARM	01		Read Current SM-addr. (8 MSBs) (not used) *
RDUARL	02		Read Current U-addr. (8 LSBs) *
RDUARM	03		Read Current U-addr. (8 MSBs) *
RDDRST1	04		Read Drive Status (See TABLE 1) *
RSDIFST	05		Read Disk Interface Status (See TABLE 2) *
RDHDSST	06		Read High Speed Disk Interface Status (See TABLE 3)
RDECCPAT	07		Read ECC Error Pattern (12 bits) *
RDDRFLG	08	8	Read Header Flag byte (See TABLE 4)
RDDRCYLL	09	9	Read Header Cylinder (8 LSBs)
RDDRCYLM	0A	A	Read Header Cylinder (8 MSBs)
RDDRHD	0B	B	Read Header Head (5 bits)
RDDREC	0C	C	Read Header Record (7 bits)
RDMDBDA	0D		Read Memory Data Buffer Data (8 bits) (Note 1) *
RDECSTA	0E		Read ECC Status (6 bits) *
			(Board Decode = 2 (HSSMA))
RDINTR	00		Read Interrupt Register

INTERRUPT REGISTER

Normal Done	Error
0 - U-done	0 - XMCI Parity
1 - SM-done	1 - MDB Parity
2 - (not used)	2 - MPC Parity
3 - (not used)	3 - DIF Error (SM error)
4 - Interface Busy	4 - Interface Busy
	5 - Self Test Active

* Two reads must be done to ensure valid data on the CT-bus.

Note 1: Each double read (required) increments the Memory Data Buffer address + 1.

TABLE 1 : Drive Status (RDDRST1)

0	Unit Ready
1	On Cylinder
2	Seek Error
3	Fault
4	Write Protected
5	Unit Selected
6	Drive Busy
7	Seek End

TABLE 2: Disk Interface Status (RSDIFST)

0	Sync Error (header only)
1	Defective Track
2	Cylinder Miscompare
3	Head Miscompare
4	Record not found
5	ECC Error on header
6	ECC Error on data
7	No Drive Clocks

TABLE 3: High Speed Disk Interface Error Status (RDHDSST)

0	DIF Parity Error, CMC Parity Error detected by DIFP
1	DIF Parity Error, MDB Parity Error detected by DIFP
2	HSSM Internal Parity Error, CMC Parity Error detected by MPC
3	HSSM Buffer Memory Parity Error, CMC Parity Error detected by MDB
4	HSSM Buffer Memory Parity Error, UMD/CMC Parity Error detected by XMCI
5	CT-bus Parity Error
6	Instruction Bus Parity Error
7	U-bus Parity Error
8	DIF FIFO Error

TABLE 4: Header Flags (RDDRFLG)

0	Defective Track				
1					
2	Drive type	0 = Undefined	1 = M2351*	2 = CDS 513	3 = M2333K
3		4 = Swallow 5	5 = Swallow 4	6 = MPI 9720	7 = MPI 9720 with
4					factory defects
5	Record Length	0 = Undefined	1 = 112	2 = 448	3 = Undefined
6					
7	Emulation	0 = 8470	1 = 8434	2 = 8450	3 = Data Copy

* For systems operating under a multihost environment, this drive type is CDC 1.2GB.

DATA INPUT SEQUENCE

AN EXTERNAL DEVICE SENDS DATA TO THE PROCESSOR BY WAY OF THE CONTROLLER IN THE FOLLOWING MANNER.

1. THE PROCESSOR PLACES A FUNCTION WORD IN THE CHANNEL REGISTER AND SETS THE FULL FLAG AND THE CHANNEL ACTIVE FLAG. COINCIDENTLY. IT SENDS THE WORD AND A FUNCTION SIGNAL TO THE CONTROLLER. THE FUNCTION SIGNAL IDENTIFIES THE WORD AS A FUNCTION CODE RATHER THAN A DATA WORD.

2. THE CONTROLLER SENDS AN INACTIVE SIGNAL TO THE PROCESSOR INDICATING ACCEPTANCE OF THE FUNCTION CODE. THE SIGNAL DROPS THE CHANNEL ACTIVE FLAG WHICH IN TURN DROPS THE FULL FLAG AND CLEARS THE CHANNEL REGISTER.

3. THE PROCESSOR SETS THE CHANNEL ACTIVE FLAG AND SENDS AN ACTIVE SIGNAL TO THE CONTROLLER WHICH SIGNALS THE DEVICE TO START SENDING DATA.

4. THE DEVICE READS A WORD AND THEN SENDS THE WORD TO THE CHANNEL REGISTER WITH A FULL SIGNAL WHICH SETS THE CHANNEL FULL FLAG.

5. THE PROCESSOR STORES THE WORD, DROPS THE FULL FLAG, AND RETURNS AN EMPTY SIGNAL INDICATING ACCEPTANCE OF THE WORD. THE DEVICE CLEARS ITS DATA REGISTER AND PREPARES TO SEND THE NEXT WORD.

6. REPEAT STEPS 4 AND 5 FOR EACH WORD TRANSFERRED.

7. AT THE END OF THE TRANSFER, THE CONTROLLER CLEARS ITS ACTIVE CONDITION AND SENDS AN INACTIVE SIGNAL TO THE PROCESSOR TO INDICATE END-OF-DATA. THE SIGNAL CLEARS THE CHANNEL ACTIVE FLAG TO DISCONNECT THE CONTROLLER AND THE PROCESSOR FROM THE CHANNEL.

8. AS AN ALTERNATIVE, THE PROCESSOR MAY CHOOSE TO DISCONNECT FROM THE CHANNEL BEFORE THE DEVICE HAS SENT ALL OF ITS DATA. THE PROCESSOR DOES THIS BY DROPPING THE ACTIVE FLAG AND SENDING AN INACTIVE SIGNAL TO THE CONTROLLER WHICH IMMEDIATELY CLEARS ITS ACTIVE CONDITION AND SENDS NO MORE DATA.

```
 165  0026  373F3 F00BA                RDRAMB R3,ILDFLG                ;GET ILD FLAGS
 166  0027  45053 F0002                TSTRBIT R3,2                    ;IF ANY ILD SEEK COMPLETE...
 167  0028  EC401 33CDA                SETPGE 1 & BNZ POLL12           ;PENDING, GO TO POLLING
 168                            ;
 169  0029  371FE F00BF       WAIT18:  MOVE RAME,IREGL& NOP RETURN     ;GET ILD RETURN ADDR
 170  002A  371F9 F00BE                MOVE RAME,IREGH & NOP RETURNA
 171  002B  45053 F0001                TSTRBIT R3,1                    ;ILD ACTIVE?
 172  002C  C3000 63FFF                RD SCP,PRGCPB,R0 & CJIR NALUZ   ;YES, RETURN TO THE ILD
 173                            ;
 174  002D  E30C0 FFFFF                CTL SCP,MPPGCLR                 ;RESET PUSH-BUTTON REG.
 175  002E  45340 F000F                AND DB,B,MSK1,R0 & NOP H#F      ;CHECK FOR ILD 1-F
 176  002F  433F9 33002                RESETR R9 & BOZ WAIT00          ;NO, ONCE MORE THRU WAIT LOOP
 177  0030  FFFFF E1005                JMP ILD00                       ;START THE ILD


 179                            ;       DISPLAY ROUTINE
 180                            ;
 181  0031  E7C00 4F001        DISP00:  CTL OCP,OCPDSEL & PSHLD 1
 182  0032  C3030 887FF                RD SCP,PGRMSEL,R0 & CLPCNT EVCNTZ ;READ THUMBWHEEL SWITCHES
 183  0033  EC403 1F2C7                SETPGE 3 & JSR FRBDISP          ;CHECK FOR XRB DISPLAY
 184  0034  45050 F0400                TSTRBIT R0,400                  ;CHECK FOR DISPLAY < 400
 185  0035  60000F 3303E               XOR AQ,Q,R0 & BOZ SMDISP        ;IF < 400, SM-BUFFER DISPLAY
 186                            ;
 187  0036  327F0 FFFFF                OR ZQ,LSBZ,,R0                  ;MULTIPLY: THUMBWHEEL SWITCHES...
 188  0037  0C10E 1F03D                ADD AQ,FOUTL,R0,IREG & JSR DISP02+1 ; X 3 = SMB MEMORY ADDRESS
 189  0038  9350F 1F03C                WRTL SCP,LDDISP1,R0 & JSR DISP02 ;DISPLAY BITS 24-35
 190  0039  9360F 1F03C                WRTL SCP,LDDISP2,R0 & JSR DISP02 ;DISPLAY BITS 12-23
 191  003A  3706F FFFFF                RDREGQ SMCST                    ;RESET XMC PARITY ERRORS
 192  003B  9370F 5FFFF                WRTL SCP,LDDISP3,R0 & JAR       ;DISPLAY BITS 0-11 & RETURN
 193                            ;
 194  003C  0F1EE FFFFF        DISP02:  INCRD IREG,IREG
 195  003D  373D0 AF7FF                RDREGB RAMI,R0 & RTS            ;GET SMB DATA
 196                            ;
 197  003E  FFFFF E3044        SMDISP:  JMP SMDISPA
```

DATA OUTPUT SEQUENCE

THE PROCESSOR SENDS DATA TO AN EXTERNAL DEVICE IN THE FOLLOWING MANNER.

1. THE PROCESSOR PLACES A FUNCTION WORD IN THE CHANNEL REGISTER AND SETS THE FULL FLAG AND THE CHANNEL ACTIVE FLAG. COINCIDENTLY, IT SENDS THE WORD AND A FUNCTION SIGNAL TO THE CONTROLLER. THE FUNCTION SIGNAL IDENTIFIES THE WORD AS A FUNCTION CODE RATHER THAN A DATA WORD.

2. THE CONTROLLER SENDS AN INACTIVE SIGNAL TO THE PROCESSOR, INDICATING ACCEPTANCE OF THE FUNCTION CODE. THE SIGNAL DROPS THE CHANNEL ACTIVE FLAG WHICH IN TURN DROPS THE FULL FLAG AND CLEARS THE CHANNEL REGISTER.

3. THE PROCESSOR SETS THE CHANNEL ACTIVE FLAG AND SENDS AN ACTIVE SIGNAL TO THE CONTROLLER WHICH SIGNALS THE DEVICE THAT DATA FLOW IS STARTING.

4. THE PROCESSOR PLACES A DATA WORD IN THE CHANNEL REGISTER AND SETS THE FULL FLAG. COINCIDENTLY, IT SENDS THE WORD AND A FULL SIGNAL TO THE CONTROLLER.

5. THE CONTROLLER ACCEPTS THE WORD AND SENDS AN EMPTY SIGNAL TO THE PROCESSOR WHERE IT CLEARS THE CHANNEL REGISTER AND DROPS THE FULL FLAG.

6. REPEAT STEPS 4 AND 5 FOR EACH PROCESSOR WORD.

7. AFTER THE LAST WORD IS TRANSFERRED AND ACKNOWLEDGED BY THE CONTROLLER EMPTY SIGNAL, THE PROCESSOR DROPS THE CHANNEL ACTIVE FLAG AND SENDS AN INACTIVE SIGNAL TO THE CONTROLLER TO TURN IT OFF.

STATUS REQUEST

A STATUS REQUEST IS A SPECIAL ONE-WORD DATA INPUT TRANSFER IN WHICH AN EXTERNAL DEVICE INDICATES A READY OR ERROR CONDITION TO A PROCESSOR.

1. THE PROCESSOR PLACES A FUNCTION WORD IN THE CHANNEL REGISTER AND SETS THE FULL FLAG AND THE CHANNEL ACTIVE FLAG. AT THE SAME TIME, IT SENDS THE WORD AND A FUNCTION SIGNAL TO THE CONTROLLER. THE FUNCTION SIGNAL TELLS THE CONTROLLER THE WORD IS A FUNCTION RATHER THAN A DATA WORD.

2. THE CONTROLLER SENDS AN INACTIVE SIGNAL TO THE PROCESSOR INDICATING ACCEPTANCE OF THE STATUS FUNCTION CODE. THE SIGNAL DROPS THE CHANNEL ACTIVE FLAG WHICH IN TURN DROPS THE FULL FLAG AND CLEARS THE CHANNEL REGISTER.

3. THE PROCESSOR SETS THE CHANNEL ACTIVE FLAG AND SENDS AN ACTIVE SIGNAL TO THE CONTROLLER WHICH SIGNALS THE DEVICE TO SEND THE STATUS WORD.

4. THE CONTROLLER SENDS THE STATUS WORD TO THE CHANNEL REGISTER WITH A FULL SIGNAL WHICH SETS THE CHANNEL FULL FLAG.

5. THE PROCESSOR STORES THE WORD, DROPS THE FULL FLAG, AND RETURNS AN EMPTY SIGNAL INDICATING ACCEPTANCE OF THE WORD.

6. THE PROCESSOR DROPS THE CHANNEL ACTIVE FLAG TO DISCONNECT THE CHANNEL AND SENDS AN ACTIVE SIGNAL TO THE CONTROLLER TO DISCONNECT IT.

QUALITY ASSURANCE SYSTEM CHECK LIST

****

7000

****

* CUSTOMER NAME : _____

* SALES ORDER NO. : _____

* SYSTEM CONFIGURATION : _____

* SYSTEM MODEL NO. : _____

* SYSTEM S/N : _____

* SYS. OPER. SFTWR. NO. : _____

* O.C.P. OPER. SFTWR. NO. : _____

* MPC MICROCODE NO. : _____

* HP/A MICROCODE NO. : _____

* INSPECTED BY : _____

* DATE : _____

AUTHORIZED SIGNATURE

_____

System S/N:____ 7000 Page ___ of ___

CONTROLLER CARD CAGE PCBA's

P/N	S/N	Description	Rev.	-X01	-X02	Q.A.REM.
1601553-20_		DIFP		E	A	
1120012-301		DIFP		E	n/a	
1120016-302		MPCP		n/a	C	
1120014-20_		MDBP		E	C	
1120010-20_		XMCIP		A	A	
1106062-30_		XMCP		A	B	
1601494-20_		XM16KP		A	A	
1601495-701		XM16KP-D		B	n/a	
1601875-101		WMAP		B	n/a	
21002000		UBI				
21002100		HSP				
n/a	n/a	n/a	n/a	n/a	n/a	n/a
1106064-30_		XRBP		A	A	
21002100		HSP				
21002000		UBI				
1601875-101		WMAP		B	n/a	
1601495-701		XM16KP-D		B	n/a	
1601494-20_		XM16KP		A	A	
1106062-30_		XMCP		A	B	
1120010-20_		XMCIP		A	A	
1120014-20_		MDBP		E	C	
1120016-302		MPCP		n/a	C	
1120012-301		DIFP		E	n/a	
1601553-20_		DIFP		E	A	
0601071-20_		SLBP		A	B	

CDC INTERFACE FEATURE

P/N	S/N	Description	Rev.	-X01	-X02	Q.A.REM.
21002200		CDCI0				
21002200		CDCI1				
21002200		CDCI2				
21002200		CDCI3				
21002200		CDCI0				
21002200		CDCI1				
21002200		CDCI2				
21002200		CDCI3				

NOTE : LAL = LOWEST ACCEPTABLE REVISION LEVEL

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OPERATOR CONTROL PANEL PCBA's

****

P/N	S/N	Description	Rev.	LAL -X01	LAL -X02	Q.A.REM.
20055612	_____	DSPLY. BRD.	____	n/a	n/a	_____
1106011	_____	KEY BRD.	____	A	n/a	_____
1106012-401	_____	8085 BRD.	____	A	n/a	_____
1106059-20_	_____	COCP	____	A	A	_____
1106010-103	_____	LED BRD.	____	A	n/a	_____

DISK I/O CARD CAGE PCBA's

****

P/N	S/N	Description	Rev.	LAL -X01	LAL -X02	Q.A.REM.
1601138-10_	_____	AIX	____	B	A ("A" W/ -103)	
1106095	_____	AIO	____	G	n/a	_____
1106095	_____	AIO	____	G	n/a	_____
1601140-20_	_____	BIX	____	B	A	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1106097-201	_____	BIO	____	A	n/a	_____
1601140-20_	_____	BIX	____	B	A	_____
1106095	_____	AIO	____	G	n/a	_____
1106095	_____	AIO	____	G	n/a	_____
1601138-10_	_____	AIX	____	B	A ("A" W/ -103)	
0601112-20_	_____	IOBP	____	A	A	_____

NOTE : LAL = LOWEST ACCEPTABLE REVISION LEVEL

EXPANSION CARD CAGE PCBA's

P/N	S/N	Description	Rev.	LAL -X01	LAL -X02	Q.A.REM.
1601136		EXIO		B	n/a	
1601136		EXIO		B	n/a	
1601271-00_		EXBP		C	A	

DISK DRIVE MODULES - (LOGICAL 0 THRU 7)

P/N	DRV. S/N	Description	SER. CODE	Q.A.REM.
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	

DISK DRIVE MODULES - (LOGICAL 8 THRU 15)

P/N	DRV. S/N	Description	SER. CODE	Q.A.REM.
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	
30147525-001		SWAL4 DRIVE		
20130101-001		P.S.U.	n/a	

NOTE : LAL = LOWEST ACCEPTABLE REVISION LEVEL

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EXPANSION CARD CAGE PCBA's

P/N	S/N	Description	Rev.	LAL -X01	LAL -X02	Q.A.REM.
1601136		EXIO		B	n/a	
1601136		EXIO		B	n/a	
1601271-00_		EXBP		C	A	

DISK DRIVE MODULES - (LOGICAL 0 THRU 7)

P/N	DRV. S/N	Description	SER. CODE	Q.A.REM.
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	

DISK DRIVE MODULES - (LOGICAL 8 THRU 15)

P/N	DRV. S/N	Description	SER. CODE	Q.A.REM.
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	
30150825-001		SWAL5 DRIVE		
20153401-001		P.S.U.	n/a	

NOTE : LAL = LOWEST ACCEPTABLE REVISION LEVEL

System S/N 7000 Page ___ of ___

CACHE CARD CAGE PCBA's

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Item	P/N	S/N	Description	Rev.	LAL	Q.A.REM.
1	11030351	_____	256K MEM.	_____	H	_____
2	11030351	_____	256K MEM.	_____	H	_____
3	11030351	_____	256K MEM.	_____	H	_____
4	11030351	_____	256K MEM.	_____	H	_____
5	11030351	_____	256K MEM.	_____	H	_____
6	11030351	_____	256K MEM.	_____	H	_____
7	11030351	_____	256K MEM.	_____	H	_____
8	11030351	_____	256K MEM.	_____	H	_____
9	11030351	_____	256K MEM.	_____	H	_____
10	11030351	_____	256K MEM.	_____	H	_____
11	11030351	_____	256K MEM.	_____	H	_____
12	11030351	_____	256K MEM.	_____	H	_____
13	11030351	_____	256K MEM.	_____	H	_____
14	11030351	_____	256K MEM.	_____	H	_____
15	11030351	_____	256K MEM.	_____	H	_____
16	1116052	_____	WMCM	_____	J(L W/REV E PCB)	
17	n/a	n/a	n/a	n/a	n/a	n/a
18	11030351	_____	256K MEM.	_____	H	_____
19	11030351	_____	256K MEM.	_____	H	_____
20	11030351	_____	256K MEM.	_____	H	_____
21	11030351	_____	256K MEM.	_____	H	_____
22	11030351	_____	256K MEM.	_____	H	_____
23	11030351	_____	256K MEM.	_____	H	_____
24	11030351	_____	256K MEM.	_____	H	_____
25	11030351	_____	256K MEM.	_____	H	_____
26	11030351	_____	256K MEM.	_____	H	_____
27	11030351	_____	256K MEM.	_____	H	_____
-	1103033-001	_____	HSMB	_____	P	_____
-	1103033-002	_____	HSMB	_____	R	_____

NOTE : LAL = LOWEST ACCEPTABLE REVISION LEVEL

S.S.S. CARD CAGE PCBA's

****

Item	P/N	S/N	Description	Rev.	LAL	Q.A.REM.
1	11030351	_____	256K MEM.	_____	H	_____
2	11030351	_____	256K MEM.	_____	H	_____
3	11030351	_____	256K MEM.	_____	H	_____
4	11030351	_____	256K MEM.	_____	H	_____
5	11030351	_____	256K MEM.	_____	H	_____
6	11030351	_____	256K MEM.	_____	H	_____
7	11030351	_____	256K MEM.	_____	H	_____
8	11030351	_____	256K MEM.	_____	H	_____
9	11030351	_____	256K MEM.	_____	H	_____
10	11030351	_____	256K MEM.	_____	H	_____
11	11030351	_____	256K MEM.	_____	H	_____
12	11030351	_____	256K MEM.	_____	H	_____
13	11030351	_____	256K MEM.	_____	H	_____
14	11030351	_____	256K MEM.	_____	H	_____
15	11030351	_____	256K MEM.	_____	H	_____
16	1116052	_____	WMCM	_____	J(L W/REV E PCB)	
17	n/a	n/a	n/a	n/a	n/a	n/a
18	11030351	_____	256K MEM.	_____	H	_____
19	11030351	_____	256K MEM.	_____	H	_____
20	11030351	_____	256K MEM.	_____	H	_____
21	11030351	_____	256K MEM.	_____	H	_____
22	11030351	_____	256K MEM.	_____	H	_____
23	11030351	_____	256K MEM.	_____	H	_____
24	11030351	_____	256K MEM.	_____	H	_____
25	11030351	_____	256K MEM.	_____	H	_____
26	11030351	_____	256K MEM.	_____	H	_____
27	11030351	_____	256K MEM.	_____	H	_____
-	1103033-001	_____	HSMB	_____	P	_____
-	1103033-002	_____	HSMB	_____	R	_____

NOTE : LAL = LOWEST ACCEPTABLE REVISION LEVEL

System S/N : ____ 7000 Page ___ of ___

P/N	S/N	Description	Q.A.REM.
20130101-001	_____	P.S.U.(OCP)	_____
20114801	_____	P.S.U.(CH. A)	_____
20114801	_____	P.S.U.(CH. B)	_____
20114401	_____	P.S.U.(CACHE)	_____
20114401	_____	P.S.U.(S.S.S.)	_____
20114901	_____	P.S.U.(CH. A)(-5V)	_____
20114901	_____	P.S.U.(CH. B)(-5V)	_____

VERIFY THE FOLLOWING:	YES/NO
**********	******
1. SAFETY CHECKLIST	_____
2. HIGH POT TEST	_____
3. LEAKAGE TEST	_____
4. UL/CSA LABEL	_____
5. SYSTEM LOGO AND ID LABEL	_____
6. DOCUMENT PACKAGE (P/N 1601576-001)	_____
7. FINAL Q.A. TEST COMPLETED	_____

NOTE : AC POWER CONFIGURED TO : _____

DATA SAVE JUMPER SET - UP

PCBA'S	JUMPER POST NAME	FROM POST NO.	TO POST NO.	DESCRIPTION
DSIO (P/N 1601269)	JX	5	12	SELECT ADDRESS DRIVE TO MOD. # 32 OR PHYSICAL DRIVE # 64
	JY	2	5	

CACHE DIP SWITCH SET - UP

PCBA'S	DIP SW.	DIP SWITCH POSITION 8	7	6	5	4	3	2	1	DESCRIPTION
WMAP	SW1	n/a	n/a	n/a	n/a	n/a				CACHE SIZE
	SW2	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	REF. TABLE I
XRBP	BC4									XRB FILE MAX.
	BE4									REF. TABLE II

XMCP

* = JUMPER POST

AR1 (JUMPER POST)

URSB	*	*	SDI
URSP	*	*	URSA
SSS	*	*	OPTIONAL
DL12	*	*	DO12
DL13	*	*	DO13
RAT	*	*	N/C
CAC	*	*	OPTIONAL

AR2 (JUMPER POST)

EOF0	2	*	*	NO. OF SSS UNITS-1 32 MAX
1	4	*	*	
2	6	*	*	
3	8	*	*	
4	10	*	*	
5		*	*	SSSU #0 (BIT)
UCNT		*	*	

AR3 (JUMPER POST)

SW0	*	*	SSSU #1(BIT)
1	*	*	SEE NOTE 2
2	*	*	DATA COPY INH.
3	*	*	BACK SCAN ENB.
4	*	*	DCHL ENB.
5	*	*	DISK ARRAY ENB
SS	*	*	SMI

NOTE 1: OPTIONAL REF. TABLE III, SSSU#=SSS STARTING ADDR.REF.TABLE IV

NOTE 2: HALF REV. INH. / ENABLE ILD1, ILD4

NOTE 3: AR3 JUMPER POST DESCRIPTIONS ARE ON PAGE 10

TABLE I

CACHE SIZE	SW POSITION		
	3	2	1
1 MEG	0	0	0
2 MEG	0	0	1
3 MEG	0	1	0
4 MEG	0	1	1
5 MEG	1	0	0
6 MEG	1	0	1
7 MEG	1	1	0
8 MEG	1	1	1

TABLE II

CACHE SIZE	FUJI DRV. 2344		FUJI DRV. 2382	
	FILE MAX.	NO. TRACK	FILE MAX.	NO. TRACK
1 MEG	1EC	123	194	101
2 MEG	3D8	246	32C	203
3 MEG	5C4	369	4C4	305
4 MEG	7B0	492	658	406
5 MEG	99C	615	7F0	508
6 MEG	B88	738	988	610
7 MEG	D74	861	B20	712
8 MEG	F64	985	CB4	813
9 MEG	FFC	1023	E4C	915
10 MEG	---	---	FFC	1023

TABLE III

	DESCRIP.	JUMPER
CAC	WRITE THRU	OUT
	BYPASS	IN
	CACHE	OUT
SSS	SSS	IN
	NO SSS	OUT

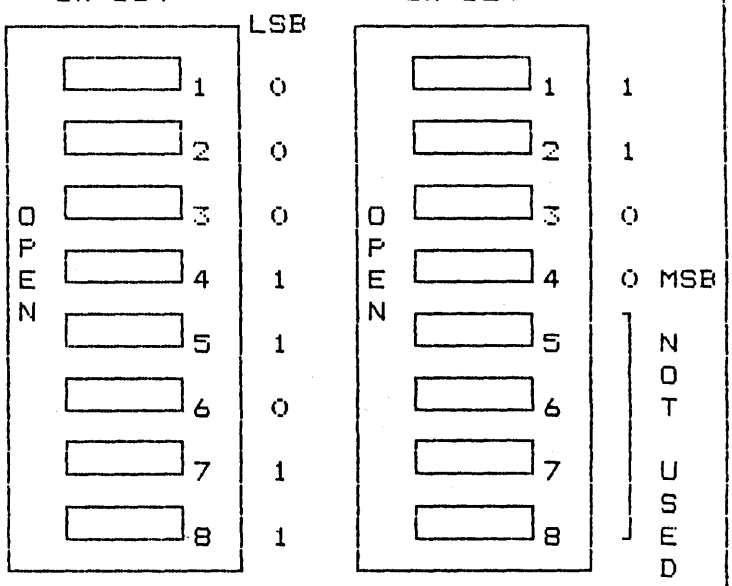
TABLE IV

SSSU # BIT 1	SSSU # BIT 0	STARTING ADDRESS
0	0	0
0	1	8
1	0	16
1	1	24

0 = JUMPER IN
1 = JUMPER OUT

THE ACTUAL MEMORY SIZE MUST BE INSTALLED TO SUPPORT THE CACHE AT THE SELECTED XRB SETTINGS. ALSO, THE WMAP CACHE MEMORY SIZE SWITCHES MUST REFLECT THE ACTUAL MEMORY SIZE BEING USED. 0 = OPEN 1 = CLOSED.

EXAMPLE, HEX VALUE 3D8 = 2 MEG



TOGGLE SWITCH SET - UP			
PCBA'S	TOGGLE SWITCH	POSITION	DESCRIPTION
MPCP	SW1	UP	RUN CLOCKS (NORMAL)
		DOWN	HALT CLOCKS
WMCM	SW1	UP	ENABLE CONTROL UNIT 'A' (NORMAL)
		DOWN	DISABLE CONTROL UNIT 'A'
	SW2	UP	ENABLE CONTROL UNIT 'B' (NORMAL)
		DOWN	DISABLE CONTROL UNIT 'B'

XMCP (ON PAGE 8)

AR3 (JUMPER POST) DEFINITIONS / OPTIONS

SW0 - MSB OFF SSS STARTING ADDRESS
SW1 - HALF REV. INH. (DO NOT INSTALL JUMPER)
SW2 - JUMPER "IN" IF NO DATA COPY DRIVE
SW3 - ENABLE BACKSCAN SEEK, INSTALL JUMPER
SW4 - DUAL CHANNEL ENABLE, INSTALL JUMPER
SW5 - DISK ARRAY MODE JUMPER 'IN' IF 1 PHY DRV = 1 LOG DRV
SS - DO NOT INSTALL JUMPER

HSSM DIP SWITCH SET - UP									
PCBA	SWITCH BB12								
XMCIP	1	2	3	4	5	6	7	8	SW BB12 - 1 & 6 OPEN SW BB12 - 2,3,4,5,7 & 8 ARE ALWAYS CLOSED
	0	1	1	1	1	0	1	1	

\ IF THIS SW IS CLOSED LED (DISK ERROR) STAYS ON

NOTE :
1=ON
0=OFF

UBI & HSP DIP SWITCH SET - UP
AS SHIPPED

PCBA'S	DIP SW.	DIP SWITCH POSITION								DESCRIPTION
		1	2	3	4	5	6	7	8	
UBI	SW1	1	0	0	0	n/a	n/a	n/a	n/a	SPLCH-IDENTIFIES WHAT CH.ADAPTER IS TO XMCP
	SW2	1	0	0	0	n/a	n/a	n/a	n/a	SPIF - EXTERNAL FUNCTION INTERRUPT
	SW3	0	0	0	0	n/a	n/a	n/a	n/a	PORT ADDRESS
HSP	SW1	1	1	0	0	n/a	n/a	n/a	n/a	STATUS BUFFER PORT
	SW2	1	1	1	1	n/a	n/a	n/a	n/a	SYSTEM PORT
	SW3	0	0	0	0	0	0	0	0	STATUS BUFFER WRITE-THRU
	SW4	1	1	1	1	1	1	1	1	SYSTEM STATUS (NOT USED)

EXPANSION I/O BOARD JUMPER SET - UP

PCBA	FROM PIN	TO PIN	DESCRIPTION
EXIO J3	1	16	SELECTS MODULE 0 THRU 15
	2	15	SELECTS MODULE 16 THRU 31

DISK I/O BOARD JUMPER SET - UP

PCBA'S	FUJITSU 2344 DRIVE	DESCRIPTION
AIO	E1 TO E3	0 - 7(PHYSICAL) 0 - 7(LOGICAL)
	E2 TO E3	0 - 7(PHYSICAL) 8 - 15(LOGICAL)
AIX	PIN 3 TO PIN 4	FOR 103 BOARDS ONLY

System S/N : _____ Page ___ of ___

NOTE :

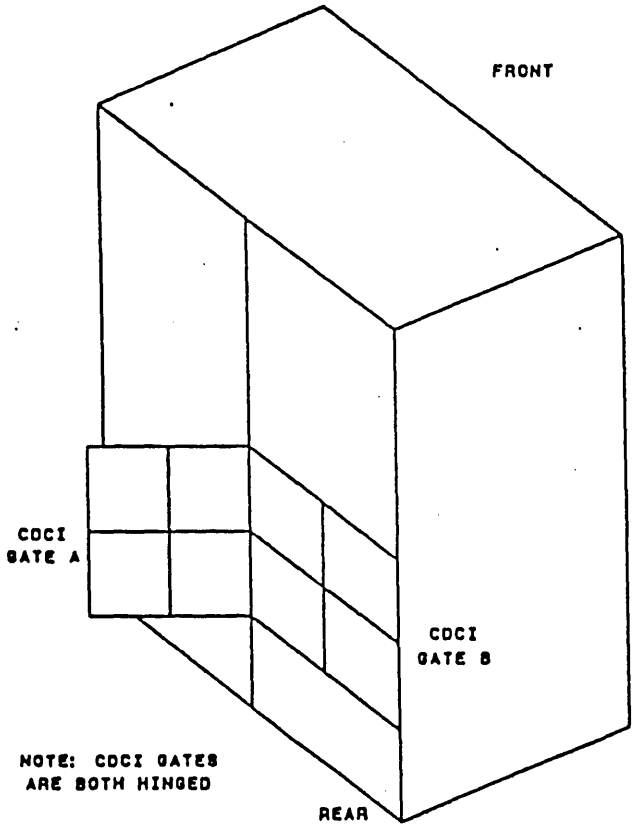
1=ON
0=OFF

CDCI DIP SWITCH SET - UP
AS SHIPPED

CDCI PCBA's	DIP SW.	DIP SWITCH POSITION								DESCRIPTION
		1	2	3	4	5	6	7	8	
GATE A CH. A CDCI 0	SW1*	1	0	0	1	0	0	0	0	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMING
GATE A CH. A CDCI 1	SW1*	1	0	1	0	1	0	1	0	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMING
GATE A CH. A CDCI 2	SW1*	1	0	1	1	1	0	1	1	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMING
GATE A CH. A CDCI 3	SW1*	1	1	0	0	1	1	0	0	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMING
GATE B CH. B CDCI 0	SW1*	1	0	0	1	0	0	0	1	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMING
GATE B CH. B CDCI 1	SW1*	1	0	1	0	1	0	1	0	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMIMG
GATE B CH. B CDCI 2	SW1*	1	0	1	1	1	0	1	1	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMING
GATE B CH. B CDCI 3	SW1*	1	1	0	0	1	1	0	0	PORT SELECT
	SW2	0	0	0	0	0	1	0	0	CHANNEL TIMING

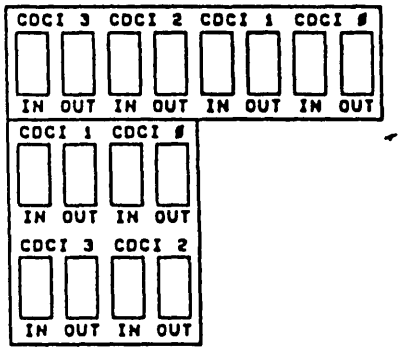
* SW1 DIP SWITCH LABELS "ON & OFF" ARE REVERSED; i.e. ON=OFF & OFF=ON

System S/N : ____ 7000 Page ___ of ___

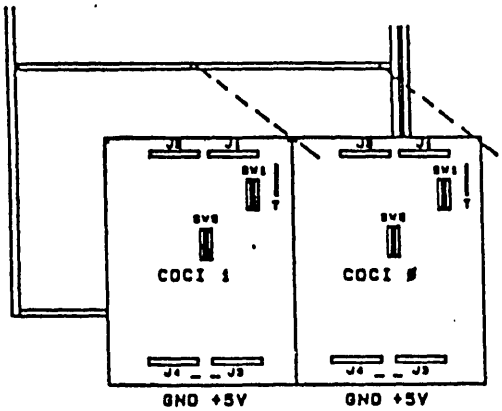


NOTE: COCI GATES ARE BOTH HINGED

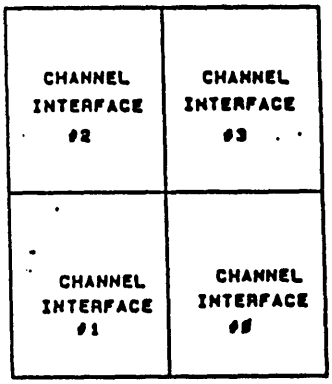
COCI CONNECTORS PANEL



2 COCI BOARDS



COCI GATES



COCI GATES

7. POWER ON/OFF PROCEDURES

This section provides procedures for powering on and off a 7001 Mass Storage System.

7.1 7001 Power On Procedure

All circuit breakers for the dual controller and disk drives are located at the rear of the 7001 cabinet beneath the power supply panel in the AC power box. See figure 7-1 for an illustration of the AC power box within the cabinet.

1. Turn on power to the controller. Turn on circuit breakers, located in the AC power box, in the following order: MAIN POWER, FANS, OCP, CHANNEL A, CHANNEL B (CHANNEL refers to each controller), and the drives.

2. The system automatically reinitializes both controllers.

3. Powering up the controller automatically initiates the 7001 controller confidence test. If these tests pass, **CHANNEL READY** appears at the OCP display indicating both controllers have been cleared. If a controller confidence test fails, a message is displayed on the Function/Status display of the OCP or on thumbwheel display 555, bits 35-24. See section 7.2 below for details about the 7001 controller confidence tests.

4. Turn on power to all disk drives in the system as follows:

   a. Press the PWR switch for disk drive 0; this switch is located on the drive control panel of the 7001 cabinet.

   b. Wait several seconds and then press the PWR switch for disk drive 1. A short interval is required between PWR switch activations.

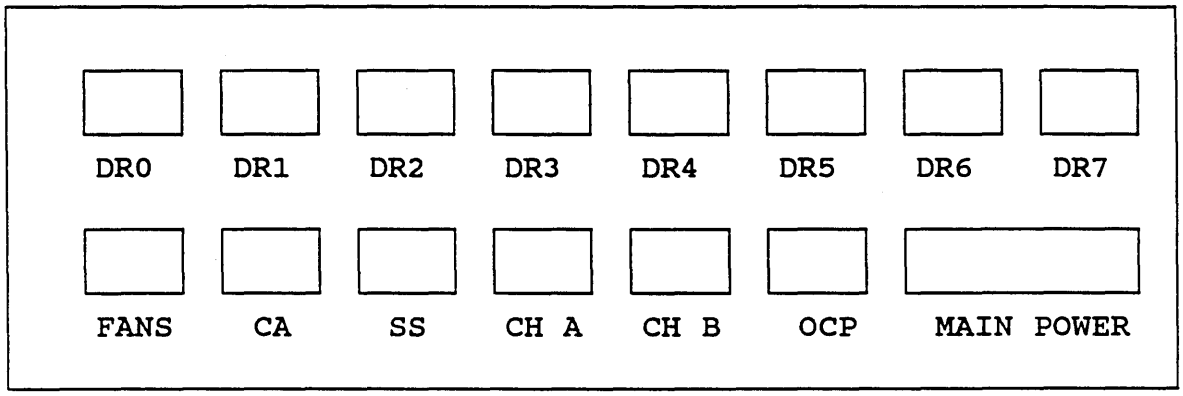
   c. Repeat steps a and b to apply power to every disk drive in the system.

   d. Ensure that the RDY indicator is lit for every disk drive. This indicator should light about 15 seconds after the PWR switch is pressed. It indicates that disks are up to speed and that the disk drive is ready for operation.

5. At the OCP keypad, set the current time by pressing **LOAD 0**. Then enter the current time as HH MM SS. Note: See section 5.2.2 for further information.

6. If applicable, set the backup time (press **LOAD 1**) and interval time (press **LOAD 2**) to the desired values. See sections 5.2.3 and 5.2.4 respectively for further information.

7. Remove the drives from write protect. At the drive panel, depress the WRITE PROTECT switch so it is no longer illuminated; the system is now ready for normal operation.



NOTES: *DR1 controls drives 0 and 1; DR3 controls drives 2 and 3; DR5 controls drives 4 and 5. DR0, DR2, DR4, DR6, DR7, CA, and SS are nonfunctional in the 7001.*

Figure 7-1
AC Power Box in 7001 Cabinet

7.2 7001 Controller Confidence Test

The 7001 controller confidence test is designed to verify the proper operation of controller hardware. It is automatically executed in the following cases:

- o On powering up the controller
- o When Toggle 7 is issued from the OCP
- o When Toggle 17 is issued from the OCP

7.2.1 How to Monitor Test Results

XMCP and XM16KP Tests. To determine the results of the XMCP and XM16KP test, set the DISPLAY/SELECT thumbwheel switch on the OCP to EXX, (where XX represents any two hexadecimal characters). If one or both of these tests fail, a binary code significant of the type of error will be displayed on the operations/maintenance display, bits 13-0. The binary codes are listed and explained in section 7.2.2.

Information about the XMCP and XM16KP tests and about communication between these boards and other parts of the system is also available from thumbwheel switch setting 555, as described below under "OCP Test."

Note that if the XMCP and XM16KP tests pass, the OCP test commences. If an XMCP or XM16KP test fails, the 7001 confidence test program enters an endless loop, and no further tests are performed.

UBI and HSP Tests. The UBI and HSP tests are run at the same time that the OCP tests are run. To determine the results of the UBI and HSP tests, set the DISPLAY/SELECT thumbwheel switch on the OCP to 4D0. If the tests were successful, the hex display shows 81F100000. If either of the tests produced an error, the following bits are set:

bits 18,19	A NO OP command.
bit 35	An external function has been sent from the host.

Bits 0-11 shows an error code which tells you what the error was. Refer to section 5.4.3 for detailed information about these error codes.

OCP Test. To determine the results of the OCP test, set the DISPLAY/SELECT thumbwheel switch to 555, bits 35-24. This is the display associated with the SMB memory location 3FF, which is used as the Controller Status Word (CSW) for all these tests. Only the five LSBs are meaningful, and each of them is assigned to a particular board or set of boards as follows:

Bit 0: If 0, the XMCP and XM16KP boards pass. If 1, the XMCP and/or XM16KP board is failing.

Bit 1: If 0, communication between the XMCP and the OCP passes. This also indicates that the CT bus and the INST bus probably pass, subject to further verification. If 1, the communication between the XMCP and the OCP is bad.

Bit 2: If 0, communication between the XMCP and the XMCIP passes. Also, the CT bus, and the INST bus probably pass, subject to further verification. If 1, there is bad communication between the XMCP and XMCIP boards.

(Note that the CT bus and INST bus cannot be directly tested by the program. However, most test routines use these buses for communication between the XMCP and other tested boards. so that the successful completion of these tests indicates high probability of the buses' proper operation.)

In the process of testing the controller boards, the bit corresponding to the board or set of boards under test is reset if the test is passed. If a board is failing, the corresponding bit is left set. The program branches to the next test regardless of the previous test results. (The XMCP and XM16KP board tests are exceptions to this rule; see below.)

HSSM Test. Check the Function/Status display on the OCP: If the HSSM test fails, an error message is shown on this display. Error messages are listed and explained later in section 7.2.

When more than one board fails. When more than one board fails, the message corresponding to the first failure detected is the only one displayed. The order of failure detection is identical to the order of tests:

1. XMCP & XM16KP
2. OCP
3. HSSM

7.2.2 XMCP and XM16KP Test

This routine checks the proper operation of the various blocks on the XMCP and XM16KP boards. Each such block is assigned a bit at SMB location 3FE. Bit definition of SMB memory location 3FE (thumbwheel display location 554, bits 11-0) is as follows:

Bit Number	Definition
0	Push pop stack
1	Event counter related operations
2	Transfer register
3	ALU internal operations (2901s)
4	I REG
5	Vector priority encoder
6	Scratchpad memory (SMB) (including parity check)
7	U bus driver and receiver (including parity test)
8	Sequencer address register
9	Sequencer/AR related operations
10,11	Not used (always 00)

In the process of testing, the bit corresponding to the block under test is reset if the block passes. If the block fails, execution of the entire program terminates, leaving the corresponding bit and the bits of the untested blocks set, and the program enters an infinite loop. In this case, no further tests are possible.

The type of error is determined by setting the display select thumbwheel switch to EXX and reading the Operations/Maintenance display. The Operations/Maintenance display readouts and their associated errors are as follows:

Operations/Maintenance Display Readout	Error Description
2DF0	Push pop stack error
2DF1	Event counter error
2DF2	Transfer register error
2DF3	ALU (2901s) error
2DF4	IREG error
2DF5	Vector priority encoder error
2DF6	SMB error
2DF7	U bus error
2DF8	Sequencer address register
2DF9	Sequencer AR error

If all the tests are passed, all the bits at memory location 3FE plus bit 0 of memory location 3FF are reset, and the program proceeds to the OCP test.

7.2.3 OCP Test

This routine tests communication between the XMCP and the OCP. The following tests are performed in the order indicated:

1. The program attempts to select the OCP for 250ms. If successful, the test continues; if not successful, the test fails.

2. If the OCP is successfully selected in step 1 above, the following tests are performed:

   a. Instruction bus parity is checked. If the test is passed, the test continues; if it does not pass, the test fails.
   b. For each of the BUFFER RAM bytes 0-32, the following operations are performed:

      i) The contents are saved.

      ii) The values 15H and 2AH (only the 6 LSBs are meaningful) are written into each location. Each write operation is verified by a read operation. Each read operation is followed by a CT bus parity check. If the read and write data match, and parity checks out, the test continues; if not, the test fails.

      iii) The original contents of the memory location under test are restored.

   c. For each of the BUFFER RAM bytes 33-37 and 39, steps i, ii, and iii above are repeated, except the values written into each of those locations are 55H and AAH (all 8 bits are meaningful).

   d. The program deselects the OCP.

   e. The OCP display cursor is set at position 0.

   If all the above tests are passed, Bit 1 at SMB location 3FF is reset, indicating that communication with the OCP checks out, and the program proceeds to the HSSM test. This test also indicates that the CT bus and INST bus probably pass, subject to further verification.

   If any of the above tests fail, the program branches off to the HSSM test, leaving Bit 1 at SMB location 3FF set.

Error Messages. No messages are generated regardless of whether the OCP passes or fails the confidence tests. In case of an OCP failure, no messages will be generated by any subsequent controller confidence tests.

7.2.4 HSSM Test

This routine tests the communication between the XMCP and the HSSM boards. The following tasks are performed:

1. The test writes and reads to and from the registers in the XMCIP file register that are accessible to the XMCP. The registers accessed are tested as follows:

   The values 55H and AAH are written into each register. Each write operation is verified by a read operation. If read and write data match, the test continues; if not, the test fails.

2. The program writes and reads sequential numbers to and from these registers, beginning with a value of 1, into file register 8.

3. The program checks the parity of the XMCP CT bus, as well as the parity of the HSSM CT bus and INST bus.

   If all file register tests are passed, and the parity tests are passed, bit 2 at SMB location 3FF is reset, and the program proceeds to the HSM test. This test also indicates whether the control (CT) and instruction (INST) buses pass, subject to further verification.

   If any of the above tests fail, the program branches to the HSM test, leaving bit 2 at SMB location 3FF set. An appropriate message is generated on the OCP's Function/Status display. One of the following messages may appear:

   CODE=200 This message indicates that a file register data error has been detected on the XMCIP board.

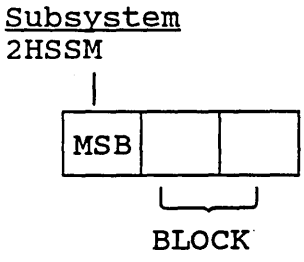
   CODE=201 This message indicates that a CT bus parity error has been detected on the XMCP board when data is passed between the XMCP and XMCIP boards.

   CODE=202 This message indicates that a CT bus parity error has been detected on the HSSM.

   CODE=203 This message indicates that an INST bus parity error has been detected on the HSSM.

7.2.5 Controller Confidence Test Failure Codes

How to read failure code table. The failure codes defining a hardware failure consist of three hexadecimal characters. The first (MSB) specifies the subsystem, while the other two specify a failed block within the subsystem.



7.2.6 UBI and HSP Test

These routines test the operation of the UBI and HSP boards.

7.3 7001 Power Off Procedure

All circuit breakers for the dual controller and disk drives are located at the rear of the cabinet in the AC power box. See figure 7-1 for an illustration of the AC power box.

1. Place the dual controller offline from the CDC system processor.
2. At the OCP keypad, press BYPASS ALL.
3. **BBBBBB PRSNT** should be displayed at the OCP, verifying that all disk drives are in bypass mode.
4. At the drive panel, place all disk drives in write protect mode (that indicator should be illuminated).
5. Power off the disk drives by pressing the PWR switch on the drive panel. Allow 30 seconds for drives to spin down, then turn off the disk drive circuit breakers located in the AC power box.
6. Turn off the circuit breakers located in the AC power box in the following order: drives, CHANNEL B, CHANNEL A, OCP, FANS, and MAIN POWER.

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8. PROBLEM ANALYSIS AND CORRECTION (TROUBLESHOOTING)

This section provides procedures for analyzing and interpreting problems which may occur in a mass storage system.

8.1 Online Channel Sense Byte Analysis

The following sections provide detailed information for analyzing sense byte information.

8.1.1 Sense Byte Format Interpretation

The sense byte information, both what is transferred to the host and what is available at the thumbwheel display, gives the technician a good understanding of what has transpired in the system if an error has occurred. Introductory information about sense bytes appears below; for detailed sense byte information, see section 8.6.

Sense byte information is separated into two groups:

GROUP A represents error conditions that can exist within the system and that are detectable at the controller/host channel interface level. These are divided into three broad categories:

- o Storage device checks
- o Controller equipment checks
- o Data checks

GROUP B represents error conditions than can occur in the system, where there is little or no information available at the controller/host channel interface. These are in two basic categories:

- o Channel timeouts
- o Undetected data corruption

In Group A, the channel sense byte data can be analyzed and used to determine the failing device(s). Also, the type of failure can be determined along with the required corrective action necessary to return the system to an online status.

8.1.2 Group A Error Conditions

Storage Device Checks. Storage device equipment checks are within the Format 1 Sense error category, as shown in figure 8-1, and can be divided into eight sections as described below.

Format 1	Message 0	NO MESSAGE (see sense bytes 8-23)
Format 1	Message 6	SET CAR ERROR
Format 1	Message 7	SET HAR ERROR
Format 1	Message 9	DRIVE STATUS NOT AS EXPECTED
Format 1	Message A	SEEK ERROR
Format 1	Message C	HSSM SM-INTERRUPT TIME-OUT
Format 1	Message E	UNABLE TO DETERMINE DRIVE TYPE
Format 1	Message F	INITIAL SELECT BUSY TIME-OUT

In addition to the above information, the sense bytes that follow sense byte 7 also contain error information that will assist in determining the failing device(s), as shown in figure 8-4.

Controller Equipment Checks. These checks are in the Format 2 Sense error category, as shown in figure 8-1, and are broken up into two sections as described below.

Format 2	Message 0	NO MESSAGE (see sense bytes 8-23)
Format 2	Message 5	HSSM U-INTERRUPT TIME-OUT

Most of the error information for Format 2 messages are in the sense bytes following sense byte 7, as shown in figure 8-5. Format 2 sense byte data can be read from the OCP via the thumbwheel display locations 404, 405, 40A, 40B, and 40C.

Data Checks. Data checks are generally media related, but can also be an indication of a controller or drive problem; for example, a defective head, faulty read/write board, failing memory, or an ESMD-I/O PCB. The type of error will point to whether there is a media defect or a hardware error in a disk drive or controller. These are described below:

Format 4	Message 1	COUNT ECC UNCORRECTABLE
Format 4	Message 3	DATA ECC UNCORRECTABLE
Format 4	Message 5	HEADER NO SYNC BYTE
Format 4	Message 7	DATA NO SYNC BYTE

Again, the sense bytes that follow sense byte 7 contain additional information for these errors, as shown in figure 8-6.

Figures 8-6, 8-7, and 8-8 contain information pertaining to error counts (logging) and configuration information. This data can be used for plotting failing trends in the equipment and also by system log analyzers.

When an error condition occurs, the sense byte data can be read at the console by responding to the error message with an "M" response. This will print out the 24 sense bytes that are associated with the error. With this information, using the Format/Message decode matrix charts, a fairly quick analysis can be done to determine in which device the problem is occurring.

The sense byte data can also be read from the controller via the thumbwheel displays. The thumbwheel display locations are listed in the final pages of this section.

8.1.3 Group B Error Conditions

Channel Timeouts. Channel timeouts are generally a result of a failure in communication between the host CPU and the 7001. This type of problem will be displayed at the console as a "Timeout Message," either answerable or not. Unanswerable timeouts generally happen when a device end was not received for a seek pending on a storage device. If this problem persists and it is only happening to a single storage device, the problem is most likely in the device. If the problem is present in several devices, the fault is more likely in the controller, where one side is causing a problem for the other device. On answerable timeouts, when the "M" response is given, generally there are no sense bytes available. This usually means the controller is in a "hang condition" and cannot return to the wait loop. If this is the case, an examination of the microprogram address display may tell you how tight a "loop" the controller is hung in. This can be determined by displaying thumbwheel location E00 and placing the system in step Run Mode (PROGM F); see section 5.2.25. Unless the problem is solid, a reset will clear this condition.

8.2 Diagnostic Testing

Refer to section 5.4 for information on diagnostic testing.

8.3 Replacement Procedures for Failed Modules

Replacement procedures for failed devices are provided in section 10 of this manual.

8.4 Verifying Failed Module Replacements

These procedures are no longer included in this manual.

8.5 Verifying Corrective Action

These procedures are no longer included in this manual.

8.6 Sense Byte Information

Sense information is constructed by the controller whenever Unit Check status is presented to the I/O channel indicating that an error or unusual condition has occurred on the current command. The sense information is retrieved by issuing a Sense I/O command. No unsolicited status is presented for one second following presentation of a Unit Check unless a Sense I/O command is received.

8.6.1 Sense Data Bytes

Twenty-four bytes of sense data are developed by the mass storage system to provide detailed information about error or unusual conditions. (Note that the recovery action field is used for error recovery. Since sense bytes are strictly informational, they are not required for recovery.) Each sense byte contains eight bits to reflect the error or unusual conditions associated with the current command. Figure 8-1 shows this format for the 24 sense bytes.

Sense bytes 0-6	Provide information about error or unusual conditions.
Sense byte 7	Indicates the format of bytes 8-23.
Sense bytes 8-23	Provide detailed information on the type of error or unusual condition.

The interpretation of bytes 8 through 23 varies according to the format presented. The sense bytes and formats are described in the following sections.

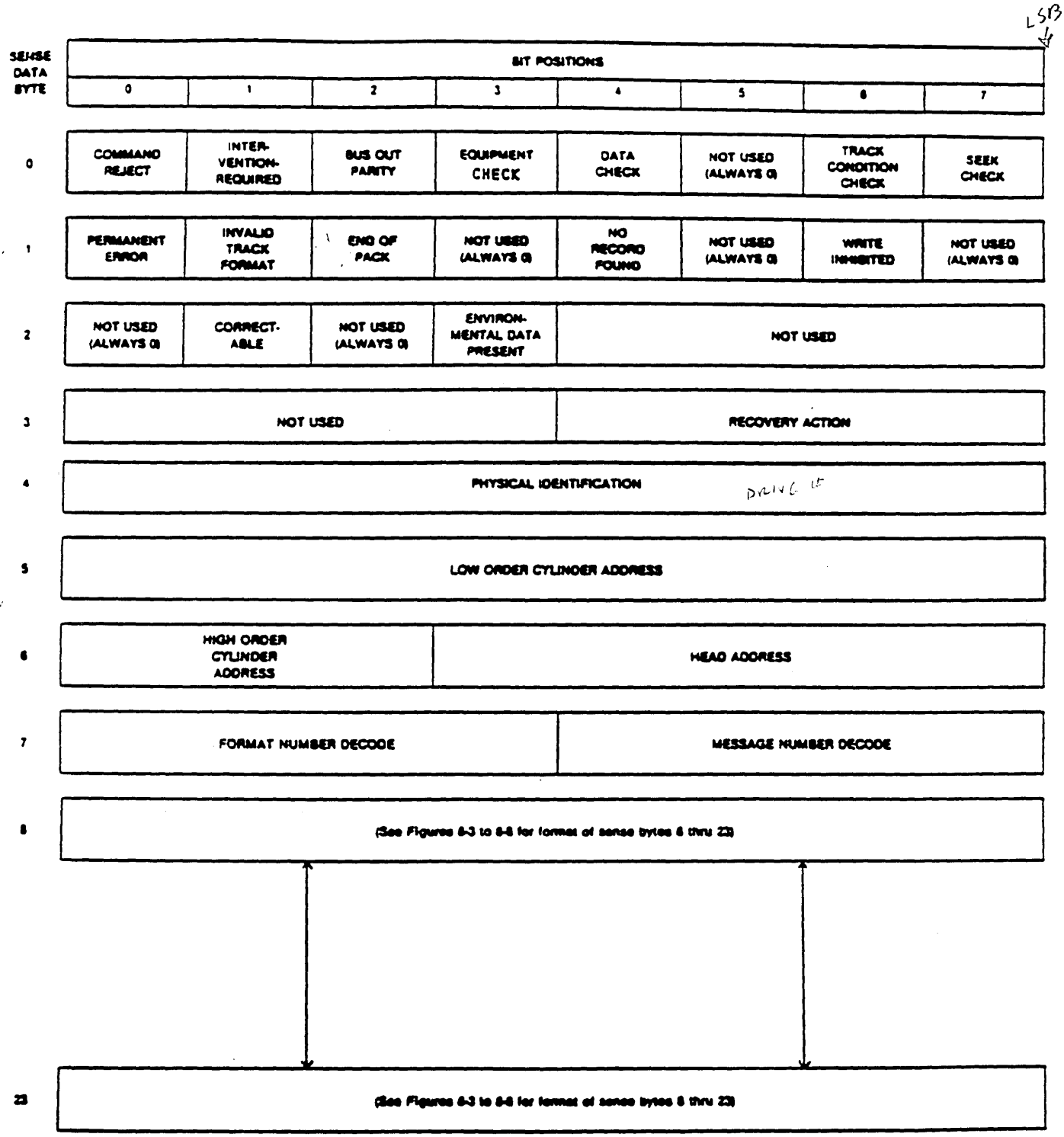

Figure 8-1
Sense Data Bytes Format

8.6.2 Message Number Decode

The message number decode sense bits indicate a message number (hexadecimal). The meaning of each message number depends on the format number. Figure 8-2 shows the format and message number decode and gives the error type.

Format	Description
0	Programming and controller errors
1	Disk device errors
2	Controller errors
3	Not used
4	ECC uncorrectable data errors
5	ECC correctable data errors
6	Error and usage counts
7	Not used
8	Read configuration
9	Drive error counters
A -> F	Not used

Figure 8-2
Message Number Decode

Format Number
(Hexadecimal)
Decoded by bits 0 through 3 of Sense byte 7

Message number (Hexadecimal) Decoded by bits 4 through 7 of Sense byte 7

	FORMAT 0	FORMAT 1	FORMAT 2	FORMAT 3	FORMAT 4	FORMAT 5	FORMAT 6	FORMAT 8	FORMAT 9
0	NO MESSAGE	NO MESSAGE	NO MESSAGE				ERROR & USAGE COUNTS	CONFIG-URATION	DEVICE ERROR COUNTERS
1	INVALID COMMAND				COUNT ECC UNCOR	COUNT CORR			
2	INVALID SEQUENCE								
3	WORD COUNT LESS THAN REQUIRED				DATA ECC UNCOR	DATA CORR			
4	DATA VALUE NOT AS REQUIRED								
5	INVALID PREP KL = 0 DL > 512		HSSM U-INTERRUPT TIME-OUT		HEADER NO SYNC BYTE				
6	BUSY TO OTHER CHANNEL	SET CAR ERROR							
7	CANNOT SET PREP LENGTH	SET HAR ERROR							
8	WRONG PREP LENGTH				CACHE ECC UNCOR				
9	TERMINA-TION BY FORCED EF	DRIVE STATUS NOT AS EXPECTED							
A	READ LABEL REQUIRED	SEEK ERROR							
B	IMPRO ALTER-NATE TRACK POINTER								
C		HSSM SM-INTERRUPT TIME-OUT							
D									
E		UNABLE TO DETERMINE DRIVE TYPE							
F		INITIAL SELECT BUSY TIME-OUT							

Figure 8-3
Format and Message Number Decode Matrix

8.6.3 Recovery Action Table

The recovery action table, table 8-1, describes the values of bits 18 through 21 of the External Interrupt. These values are returned in the EI word as well as in bits 4 through 7 of sense data byte 3.

Table 8-1
Recovery Action Table

Recovery Action	Meaning
1	Write inhibited
2	Seek in progress for another channel, correctable data check, or data check (not permanent)
3	Improper alternate track pointer
4	Command reject (except special cases) or end of pack
5	Read label command required
6	Intervention required
7	Bus out parity error
8	Equipment check
9	Permanent data check
A 10	Invalid track format or no record found
B 11	Environmental data present
C 12	Only valid copy latch set for first record partially updated on write data or write data and pad zeros
D 13	Only valid copy latch set for last record partially updated on write data

8.6.4 Format 1 Sense

Format 1 sense provides details of storage device errors. Figure 8-4 shows the significance of Format 1 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	NOT USED		SEEK INCOMPLETE	SEEK COMPLETE	ON-LINE	PACK CHANGE	BUSY	NOT USED
9		HSSM TEST FAILURE	ALL ZEROS					
10	ZEROS		ACCESS READY	ZEROS				HEAD LOAD
11	PERMANENT SEEK ERROR AND FAULT	ZEROS						
12	NOT USED		READ ONLY	ZEROS		NO DRIVE CLOCKS	ZEROS	
13	NOT USED		PHYSICAL DRIVE NUMBER					
14	SEEK END	BUSY	SELECTED	WRITE PROTECT	FAULT	SEEK ERROR	ON CYLINDER	READY
15	MODULE SELECT	TAG GATE	ENABLED TAG-VALID CHECK	NOT USED	TAG 8	TAG 4	TAG 2	TAG 1
16	ALL ZEROS							
17	ALL ZEROS							
18	ALL ZEROS							
19	ALL ZEROS							
20	ALL ZEROS							
21	ZEROS		DISK UNIT FAULT	ZEROS		NO DISK UNIT CLOCKS	ZEROS	
22	ALL ZEROS							
23	ALL ZEROS							

Figure 8-4
Format 1--Device Errors

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8.6.5 Format 2 Sense

Format 2 sense provides details of controller errors. Figure 8-5 shows the significance of Format 2 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	HAIO 1 PARITY	HAIO 2 PARITY	HAIO 3 PARITY	HAIO 4 PARITY	U-BUS→ HAIO PARITY	WMA TEST FAILURE	MDB U-DMA CHECK	UNABLE TO SELECT HAIO
9	ALU FAILURE	HSSM TEST FAILURE	HAIO SEQUENCER ERROR	DIF FIFO CHECK	MDB SM-DMA CHECK	WMA/HSSM TEST FAILURE CODE		
10	U-BUS→XMC PARITY 0-17	U-BUS→XMC PARITY 18-35	CT BUS→XMC PARITY	FRB SEARCH NO FIND	HSSM U-BUS PARITY	SMB→XMC PARITY	HSSM-WMA INST. PARITY	DIF PARITY
11	XRB MEM PARITY	CT→XRB PARITY	XRB INST. PARITY	XRB NOT AVAILABLE	HSSM BUSY TIMEOUT	CT-HSSM PARITY	HSSM INTERNAL PARITY	HSSM BUFFER MEM PARITY
12	XRB INVALID CACHE ADDR.	OCP PARITY	OCP NOT AVAILABLE	WMC SELECT ERROR	WMA PARITY	WMC PARITY	WMA CT-BUS PARITY	WMA U-BUS PARITY
13	NOT USED			DRIVE NUMBER				
14	SEEK END	BUSY	SELECTED	WRITE PROTECT	FAULT	SEEK ERROR	ON CYLINDER	READY
15	MODULE SELECT	TAG GATE	ENABLE TAG-VALID CHECK	NOT USED	TAG 8	TAG 4	TAG 2	TAG 1
16	ZERO	READ DATA TRANSFER	ZEROS		WRITE DATA TRANSFER	ZERO	READ HEADERS	READ VERIFY
17	ALL ZEROS							
18	ALL ZEROS							
19	ALL ZEROS							
20	ALL ZEROS							
21	ZEROS		DISK UNIT FAULT	ZEROS		NO DISK UNIT CLOCKS	ZERO	WMA ADDRESS CHECK
22	ALL ZEROS							
23	ALL ZEROS							

Figure 8-5
Format 2--Controller Errors

8.6.6 Format 4 Sense

Format 4 sense provides details of ECC uncorrectable data errors on disk drives. Figure 8-6 shows the significance of Format 4 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	CYLINDER HIGH ORDER BYTE							
9	CYLINDER LOW ORDER BYTE							
10	ALL ZEROS							
11	ZEROS				AMPERIF HEAD NO.			
12	ZERO	RECORD NO.						
13	ALL ZEROS							
14	ALL ZEROS							
15	ZEROS						ERROR RECOVERY RETRY COUNT	
16	STRING NO. 00 = Units 0-7 01 = Units 8-15 10 = Units 16-23 11 = Units 24-31		DISK UNIT NO. (COMPLEMENTED)				DISK UNIT NO.	
17	ALL ZEROS							
18	ALL ZEROS							
19	ALL ZEROS							
20	ALL ZEROS							
21	ALL ZEROS							
22	ALL ZEROS							
23	ALL ZEROS							

Figure 8-6
Format 4--ECC Uncorrectable

8.6.7 Format 5 Sense

Format 5 sense provides details of ECC correctable data errors. Figure 8-7 shows the significance of Format 5 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	CYLINDER HIGH ORDER BYTE (AMPERIF FORMAT)							
9	CYLINDER LOW ORDER BYTE (AMPERIF FORMAT)							
10	ALL ZEROS							
11	ZEROS				AMPERIF HEAD NO.			
12	zero	RECORD NO.						
13	ALL ZEROS							
14	ALL ZEROS							
15	ALL ZEROS							
16	RECORD LENGTH (BYTES) (MSBs)							
17	RECORD LENGTH (BYTES) (LSBs)							
18	ALL ZEROS							
19	ALL ZEROS							
20	ALL ZEROS							
21	ALL ZEROS					ECC CORRECTION PATTERN (MSBs)		
22	ECC ERROR CORRECTION PATTERN (LSBs)							
23	ALL ZEROS							

Figure 8-7
Format 5--ECC Correctable

8.6.8 Format 6 Sense

Format 6 sense provides details about error and usage counts. Figure 8-8 shows the significance of Format 6 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	TOTAL NUMBER OF BYTES READ UNDER THIS LOGICAL ADDRESS (HIGH ORDER BYTE)							
9	TOTAL NUMBER OF BYTES READ UNDER THIS LOGICAL ADDRESS							
10	TOTAL NUMBER OF BYTES READ UNDER THIS LOGICAL ADDRESS							
11	TOTAL NUMBER OF BYTES READ UNDER THIS LOGICAL ADDRESS (LOW ORDER BYTE)							
12	NUMBER OF ECC CORRECTABLE DATA CHECKS UNDER THIS LOGICAL ADDRESS (HIGH ORDER BYTE)							
13	NUMBER OF ECC CORRECTABLE DATA CHECKS UNDER THIS LOGICAL ADDRESS (LOW ORDER BYTE)							
14	ALL ZEROS							
15	NUMBER OF UNCORRECTABLE DATA CHECKS UNDER THIS LOGICAL ADDRESS (LOW ORDER BYTE)							
16	NUMBER OF SEEKS UNDER THIS LOGICAL ADDRESS (HIGH ORDER BYTE)							
17	NUMBER OF SEEKS UNDER THIS LOGICAL ADDRESS (LOW ORDER BYTE)							
18	ALL ZEROS							
19	NUMBER OF SEEK CHECKS UNDER THIS LOGICAL ADDRESS							
20	ALL ZEROS							
21	ALL ZEROS							
22	ALL ZEROS							
23	ALL ZEROS							

Figure 8-8
Format 6--Usage Error Count

8.6.9 Format 8 Sense

Format 8 sense provides details about the read configuration bytes. Figure 8-9 shows the significance of Format 8 sense bytes 8 through 23.

Sense Bytes	Bits							
	0	1	2	3	4	5	6	7
8	5			(CONTROLLER TYPE)			0	
9	5			(CONTROLLER TYPE)			6	
10	NUMBER OF USABLE CYLINDERS (MSBs)							
11	NUMBER OF USABLE CYLINDERS (LSBs)							
12	NUMBER OF HEADS							
13	RECORDS PER TRACK							
14	8				4			
15	SPERRY EMULATION 8434, 8430, 8450, 8470							
16	NOT USED				DRIVE TYPE OR SIZE IN MEGAWORDS IF SOLID STATE STORAGE UNIT			
17	NOT USED				NATIVE MODE	NOT USED	RECORD LENGTH WORDS (1=112, 2=448)	
18	NOT USED							
19	NOT USED							
20	MONTH OF MICROCODE ASSEMBLY							
21	DAY OF MICROCODE ASSEMBLY							
22	YEAR OF MICROCODE ASSEMBLY							
23	MICROCODE REVISION LEVEL							

Figure 8-9
Format 8-- Read Configuration

UNISYS SYSTEM COMMAND

8.6.10 Thumbwheel Display Locations

The following pages contain thumbwheel setting information for other systems as well as the 7001. Therefore, you will see references to items (cache, for example) which are not part of the 7001. In these cases, refer to the items which are part of the 7001 and ignore any others.

The DISPLAY/SELECT thumbwheel switches, located at the upper right of the OCP, are used in conjunction with the Operation/Maintenance Data Display. The thumbwheel switch setting selected determines the data which is displayed at the Operation/Maintenance Data Display. This display is used for diagnostic purposes.

The thumbwheel settings are as follows:

000-3FF MDBP memory data, using a single 36-bit word format

400-555 XMCP scratchpad memory data, using three 12-bit characters as a format

E00-EFF XMCP microcode address

Display settings between 400 and 555 are listed below; the sense byte data described earlier in this section may be read from these displays. For each of these descriptions, only those bits which are used are displayed; if a bit does not appear in the display location description, then it is not being used.

800-BFF Seem to have 800-CFF stored

THUMBWHEEL DISPLAY LOCATION 400: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 00				Sense Byte 01			Sense Byte 02	

Bit	Bit	Bit
31 - Command Reject	19 - Permanent Error	06 - Correctable ECC
30 - Intervention Required	18 - Invalid Track Format	04 - Env. Data Present
29 - Bus Out Parity	17 - End of Pack	
28 - Equipment Check	15 - No Record Found	
27 - Data Check	13 - Write Inhibited	
25 - Track Condition Check		
24 - Seek Check		

THUMBWHEEL DISPLAY LOCATION 401: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 03				Sense Byte 04			Sense Byte 05	
Recovery Action				Physical Drive ID			Emulated Cylinder LSBs	

Recovery Action
0 - No Error
1 - Write Inhibited
2 - Data Check (Correctable)
3 - Bad Track Pointer
4 - Command Reject
5 - Read Label Required
6 - Intervention Required
7 - Bus Out Parity
8 - Equipment Check
9 - Permanent Data Check
A - No Record Found
B - Env. Data Present
C - Only Valid Copy First
D - Only Valid Copy Last

Bits 19	Bits 18:	Drive Group
0	0	Drives 0-7
0	1	Drives 8-15
1	0	Drives 16-23
1	1	Drives 24-31

Drive Number	Complemented			Actual		
Bit:	17	16	15	14	13	12
Unit						
0	1	1	1	0	0	0
1	1	1	0	0	0	1
2	1	0	1	0	1	0
3	1	0	0	0	1	1
4	0	1	1	1	0	0
5	0	1	0	1	0	1
6	0	0	1	1	1	0
7	0	0	0	1	1	1

THUMBWHEEL DISPLAY LOCATION 402: Channel Sense Bytes

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 06 ----------|---------- Sense Byte 07 ----------|----- Sense Byte 08 -----|
            |           |           |           | Format    | Message   |        Format 1
              Emulated    Emulated Head           Decode      Decode
              Cyl.MSBs    Number      (Format/Message Decoder - See Figure 8-2)
```

Bit	Bit
05 - Seek Incomplete	02 - Pack Change
04 - Seek Complete	01 - Busy
03 - Online	

THUMBWHEEL DISPLAY LOCATION 403: Channel Sense Bytes

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 09, Format 1 -----|----- Sense Byte 10, Format 1 -----|-Sense Byte 11, Format 1-|
```

Bit	Bit	Bit
30 - HSSM Test Failure	17 - Access Ready	07 - Permanent Seek
	12 - Head Load	Error/Fault

THUMBWHEEL DISPLAY LOCATION 404: Channel Sense Bytes

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 12, Format 1 -----|----- Sense Byte 13, Format 1 -----|Sense Byte 14, Format 1,2|
                                      Physical Drive #                    Current Drive Status
```

Bit	Bit	Bit
29 - Read Only	07 - Seek End	03 - Fault
26 - No Drive Clocks	06 - Busy	02 - Seek Error
	05 - Selected	01 - On Cylinder
	04 - Write Protected	00 - Ready

THUMBWHEEL DISPLAY LOCATION 405: Channel Sense Bytes

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---- Sense Byte 15, Format 1,2 ----|---- Sense Byte 21, Format 1,2 ----|Sense Byte 8, Format 4,5 |
                                                                          Actual Cyl. MSBs
```

Bit	Bit	Bit
31 - Mod. Select	27 - Tag 8	17 - Drive Fault
30 - Tag Gate	26 - Tag 4	13 - Write Inhibit
29 - Valid Check	25 - Tag 2	
28 - Enable Tag	24 - Tag 1	

THUMBWHEEL DISPLAY LOCATIONS 406 through 409: Channel Sense Bytes

Display Location	35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
406	Sense Byte 9, Format 4,5 Actual Cyl. LSBs			Sense Byte 10, Format 4,5			Sense Byte 11, Format 4,5 Actual Head #		
407	Sense Byte 12, Format 4,5 Actual Record			Sense Byte 13, Format 4,5			Sense Byte 14, Format 4,5		
408	Sense Byte 15, Format 4 SM Error Retry Count			Sense Byte 16, Format 4 See Sense Byte 4 breakdown			Sense Byte 15, Format 5		
409	Sense Byte 16, Format 5 Record Length MSB			Sense Byte 17, Format 5 Record Length LSB			Sense Byte 21, Format 5 ECC Correction MSB		

THUMBWHEEL DISPLAY LOCATION 40A: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 22, Frmt 5 ECC Correction LSBs				Sense Byte 21, Format 6			Sense Byte 8, Format 2		

Bit		Bit	
07	HAIO Parity Error 1	03	HAIO Detected U Bus Parity Error
06	HAIO Parity Error 2	02	WMA Test Failure (See Display Location 40B)
05	HAIO Parity Error 3	01	MDB U-DMA Check
04	HAIO Parity Error 4	00	Unable to Select HAIO

THUMBWHEEL DISPLAY LOCATION 40B: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 9, Format 2				Sense Byte 10, Format 2			Sense Byte 11, Format 2		

Bit		Bit		Bit	
31	ALU Failure	19	XMCP Detected U Bus PE (0-17)	07	XRB Memory PE
30	HSSM Test Failure	18	XMCP Detected U Bus PE (18-35)	06	XRB Detected CT Bus PE
29	HAIO Sequencer Error	17	XMCP Detected CT Bus PE	05	XRB Inst. PE
28	DIFP FIFO Check	16	XRB No Find	04	XRB Not Available
27	MDBP SM-DMA Check	15	HSSM Detected U Bus PE	03	HSSM Busy Timeout
26	WMA/HSSM Test Failure Code*	14	SMB to XMCP PE	02	HSSM Detected CT Bus PE
25		13	HSSM/WMA Inst. PE	01	HSSM Internal PE
24		12	DIFP PE	00	HSSM Buffer Memory PE

* If Display Location 40A bit 2=1, use WMA Test Failure Codes;
if Display Location 40B bit 30=1, use HSSM Test Failure Codes.

HSSM Test Failure Code

0 - See other bytes
1 - Word-to-byte miscompare
2 - Byte-to-word miscompare
3 - DMA failure (early complete)
4 - U-side DMA failure (no complete)
5 - Header flag miscompare
6 - ODR or IDR tag missing
7 - Undefined error

WMA Test Failure Code

0 - See other bytes
1 - No ECC uncorrectable status on write
2 - Data miscompare (good data is always 0)
3 - Early write complete (all words not written)
4 - "Complete" interrupt not received
5 - No ECC correctable status on read
6 - ODR or IDR tag missing
7 - Undefined error

THUMBWHEEL DISPLAY LOCATION 40C: Channel Sense Bytes

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 12, Format 2			Sense Byte 16, Format 2			Next Cylinder		

Bit		Bit		Bit	
31	XRB Invalid Data or Address	27	WMAP PE	18	Read Data Transfer
30	OCP PE	26	WMCM PE	15	Write Data Transfer
29	OCP Not Available	25	WMAP CT-Bus PE	13	Read Header
28	WMC Select Error	24	WMAP U-Bus PE	12	Read Verify

FOR CRAIG: READ AHEAD — WE DON'T USE

THUMBWHEEL DISPLAY LOCATION 400

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Next Head			Next Record			Relative Record No.		

THUMBWHEEL DISPLAY LOCATION 40E

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
R5Save			Starting Word No.			Seek Error Retry Count		

THUMBWHEEL DISPLAY LOCATION 40F

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
E.F.Allowed Mask, HAIO #:4	3	2	1	Last EI on HAIO #:4	3	2	1	Attention HAIO #:4-3-2-1

CHANNEL 2

THUMBWHEEL DISPLAY LOCATIONS 410 through 41A

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Current Drive Cylinder (see below)	Current Drive Cylinder (see below)	Current Drive Cylinder (see below)

Display Location			
410	00	01	02
411	03	04	05
412	06	07	08
413	09	10	11
414	12	13	14
415	15	16	17
416	18	19	20
417	21	22	23
418	24	25	26
419	27	28	29
41A	30	31	(Spare)

THUMBWHEEL DISPLAY LOCATIONS 41B through 421

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
0 ------- 0	31 ---------- Bit Position = Logical Drive # ---------- 0							

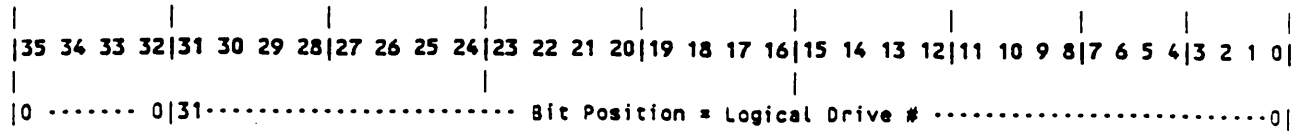
Display Location	
41B	Seek Complete Pending Mask
41C	Seek Complete Pending this Drive
41D	Seek Complete Pending on HAIO-1
41E	Seek Complete Pending on HAIO-2
41F	Seek Complete Pending on HAIO-3
420	Seek Complete Pending on HAIO-4
421	Seek Complete Pending for an ILD Drive

THUMBWHEEL DISPLAY LOCATIONS 422 through 424

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sector Timer for Drives (see below)			Sector Timer for Drives (see below)			Sector Timer for Drives (see below)		

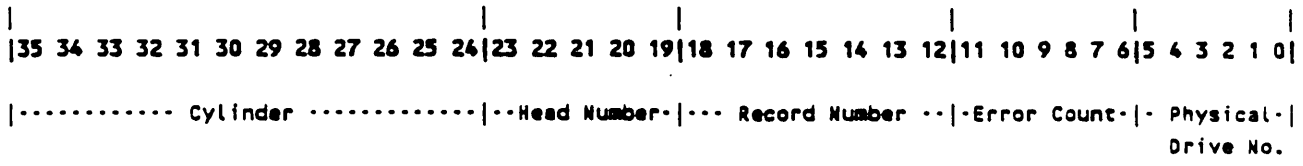
Display Location			
422	0,8,16,24	1,9,17,25	2,10,18,26
423	3,11,19,27	4,12,20,28	5,13,21,29
424	6,14,22,30	7,15,23,31	Not Used

THUMBWHEEL DISPLAY LOCATIONS 425 through 430



Display Location	
425	Bit for the ILD Drive
426	Attention Pending to HAIO-1
427	Attention Pending HAIO-1 Mask
428	Attention Pending to HAIO-2
429	Attention Pending HAIO-2 Mask
42A	Attention Pending to HAIO-3
42B	Attention Pending HAIO-3 Mask
42C	Attention Pending to HAIO-4
42D	Attention Pending HAIO-4 Mask
42E	Bit for the Current Drive (only one bit at a time can be set)
42F	Bit for Seek Error While Polling (one bit per drive)
430	Error/Usage Log Flow (one bit per drive)

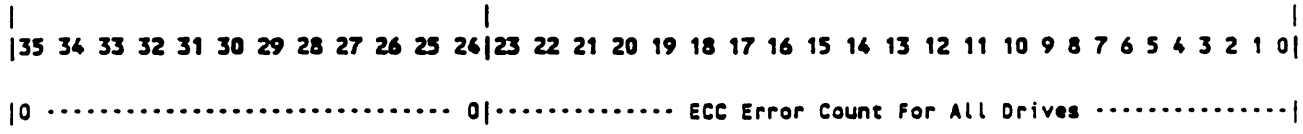
THUMBWHEEL DISPLAY LOCATIONS 431, 432, 434 and 435



Display Locations:

431: Correctable ECC Error - History #1
432: Correctable ECC Display - History #2
434: Uncorrectable ECC Display - History #1
435: Uncorrectable ECC Display - History #2

THUMBWHEEL DISPLAY LOCATIONS 433 and 436



Display Locations:

433: Count of Correctable ECC Errors
436: Count of Uncorrectable ECC Errors

THUMBWHEEL DISPLAY LOCATION 437: ECC Correction Pattern

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
R 5-Upper-Temp. Save			XMC Parity Error Retry Count			ECC Error Correction Pattern		

THUMBWHEEL DISPLAY LOCATION 438

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
SM Error Return Location (MSBs)			0			Initial Read Transfer Length		

THUMBWHEEL DISPLAY LOCATION 439

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
SM Error Return Location (LSBs)					Record Byte Address (Write)			

THUMBWHEEL DISPLAY LOCATION 43A — TO LOCATE ALT TRACKS?

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Pad Zeros Length (Write Data and Pad Zeros Function)			Alternate Cylinder			Alt. Head		

THUMBWHEEL DISPLAY LOCATION 43B - 43D: ILD Displays

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Display Location								
43B	Main ILD Display: variable depending on state of ILD							
43C	Drive Number			Current Cylinder			Current Head	
43D	(Not Used)			Starting Cylinder			Ending Cylinder	

THUMBWHEEL DISPLAY LOCATION 43E: ILD Display

```
|                                   |                   |         |         |         |
|35 34 33 32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17|16 15 14 13 12|11 10 9 8 7 6 5|4 3 2 1 0|

|---------- ILD Flags ------------|--------- Starting Head ----------|------ Ending Head ------|
```

Bit		Bit	
35	Online Format Defective	29	Last Operation
34	Format Defective	28	Format-to-Verify
33	Defective Alternate	27	Seek Initiated
32	Alt. Cyl/Reverse Seek Flag	26	ILD Running
31	Power Fail Timer Running	25	Seek Comp. Pending
30	Data Copy/Restore Running	24	ILD Active

THUMBWHEEL DISPLAY LOCATION 43F

```
|         |         |         |         |         |         |         |         |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- ILD Test No -----------|-------------- ILD Return from Wait Loop -----------------|
```

THUMBWHEEL DISPLAY LOCATIONS 440-49F: Drives 0-31 Error/Usage Log

```
|         |                                                                                 |
|35 34 33 32|31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0|

|0 ------- 0|----------Error/Usage Log Bytes Read This Drive (80,000,000₁₆ maximum) ------------|
```

Drive	Display	Drive	Display	Drive	Display	Drive	Display	Drive	Display
0	440	7	455	13	467	19	479	25	488
1	443	8	458	14	46A	20	47C	26	48E
2	446	9	45B	15	46D	21	47F	27	491
3	449	10	45E	16	470	22	482	28	494
4	44C	11	461	17	473	23	485	29	497
5	44F	12	464	18	476	24	488	30	49A
6	452							31	49D

```
|                     |                                                   |                   |         |
|35 34 33 32 31 30 29 28|27 26 25 24 23 22 21 20 19 18 17 16|15 14 13 12 11 10 9 8|7 6 5 4 3 2 1 0|

|0 ------------------ 0|--Correctable ECC (200₁₆ maximum)--|0 ---------------- 0| Uncorrectable |
                                                                                  ECC Errors
                                                                                  (40₁₆ maximum)
```

Drive	Display	Drive	Display	Drive	Display	Drive	Display	Drive	Display
0	441	7	456	13	468	19	47A	25	48C
1	444	8	459	14	46B	20	47D	26	48F
2	447	9	45C	15	46E	21	480	27	492
3	44A	10	45F	16	471	22	483	28	495
4	44D	11	462	17	474	23	486	29	498
5	450	12	465	18	477	24	489	30	498
6	453							31	49E

GOOD FOR A LOG.

THUMBWHEEL DISPLAY LOCATIONS 440-49F: Drives 0-31 Error/Usage Log (continued)

35 34 33 32	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4	3 2 1 0
0 ····· 0	···· Number of Seeks (8000_{16} maximum) ·····	0 ····· 0	Seek Errors (8 max)

Drive	Display	Drive	Display	Drive	Display	Drive	Display	Drive	Display
0	442	7	457	13	467	19	478	25	48D
1	445	8	45A	14	46A	20	47E	26	490
2	448	9	45D	15	460	21	481	27	493
3	448	10	460	16	470	22	484	28	496
4	44E	11	463	17	473	23	487	29	499
5	451	12	466	18	476	24	48A	30	49C
6	454							31	49F

THUMBWHEEL DISPLAY LOCATION 4A0-4A3

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
····· Reserved for Error/Usage Log Assembly ·····								

THUMBWHEEL DISPLAY LOCATION 4A4

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
····· ILD Return Location 1 ·····			····· ILD Return Location 2 ·····			·· ILD Return Location 3 ··		

THUMBWHEEL DISPLAY LOCATION 4A5

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
·· ILD Message Sent and Loop Flags ··			····· ILD Continuation Location ·····					

THUMBWHEEL DISPLAY LOCATIONS 4A6 THROUGH 4AF

	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
Display Location				
4A6	R14 Temporary Save	R15 Upper Temporary Save	R15 Lower Temporary Save	
4A7	ILD OCP Command[1]	ILD/OCP Parameter 1	ILD/OCP Parameter 2	
4A8	ILD Return 1 MSB	ILD Return 2 MSB	ILD Return 3 MSB	
4A9	---------- Wait Loop Pass Counter ----------		Random Seek Seed Word	
4AA	ILD Next Cylinder Save	ILD Next Head Save	R5 Temporary Save	
4AB	Not Used	Cache Read Drive Number	Drive No. for Pushed Track	
4AC	Cache Operating Status Flags[2]	Last Drive Selected	MDB U-Side Relative Record Number	
4AD	XRB Error Call to FRB Hand	No. of Tracks Unable to Write Back	Backscan Hold Off Counter (Primary)	
4AE	ILD Max Usable Cylinder	---------- Count of Pushed-Off Tracks ----------		
4AF	ILD Max Head	---------- Count of Backscan Tracks Written ----------		

[1] ILD OCP Command information appears below:

Octal Command	Description	Parameter 1	Parameter 2
01	Print Message	Message Number	
02	Reset Clock Interrupt		
03	Load Hit Ratio	Drive (0-31)	1 = Hit; 0 = Miss
04	Reset State Change Interrupt		
85	Wait for "YES/NO"	0 = no; 1 = yes	
86	Enter number (hex)	No. of Digits Data Max	
87	Enter number (decimal)	No. of Digits Data Max	
08	Print Hex Number	Data	No. of Digits to Print
09	Print Decimal Number	Data	No. of Digits to Print
0A	Set Cursor Position	Position (0-39)	
0B	Store Current Message		
0C	Reset Interrupts & State Change Requests		
8E	Enter number (0-F) and Print Alternate Message	Message Number	
0F	Clear Message Buffers		
10	Initiate Timer	No. of Seconds	
11	Reset Timer Done Flag		

[2] 4AC Cache Operating Status Flags: Bit 27 = Force down all
Bit 26 = Force Bypass all
Bit 25 = XRB down
Bit 24 = Seek only

for ILDs except ILD B

THUMBWHEEL DISPLAY LOCATIONS 480: ILD Sense Bytes

```
|          |          |          |          |          |          |          |          |          |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 00 ----------|---------- Sense Byte 01 ----------|----- Sense Byte 02 -----|
```

Bit	Bit	Bit
31 · Command Reject	19 · Permanent Error	06 · Correctable ECC
30 · Intervention Required	18 · Invalid Track Format	04 · Env. Data Present
29 · Bus Out Parity	17 · End of Pack	
28 · Equipment Check	15 · No Record Found	
27 · Data Check	13 · Write Inhibited	
25 · Track Condition Check		
24 · Seek Check		

THUMBWHEEL DISPLAY LOCATION 481: ILD Sense Bytes

```
|          |          |          |          |          |          |          |          |          |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 03 ----------|---------- Sense Byte 04 ----------|----- Sense Byte 05------|
          Recovery Action                    Physical Drive ID                Emulated Cylinder LSBs
```

Recovery Action
0 · No Error
1 · Write Inhibited
2 · Data Check (Correctable)
3 · Bad Track Pointer
4 · Command Reject
5 · Read Label Required
6 · Intervention Required
7 · Bus Out Parity
8 · Equipment Check
9 · Permanent Data Check
A · No Record Found
B · Env. Data Present
C · Only Valid Copy First
D · Only Valid Copy Last

Bits 19	Bits 18:	Drive Group
0	0	Drives 0-7
0	1	Drives 8-15
1	0	Drives 16-23
1	1	Drives 24-31

Drive Number

	Complemented			Actual		
Bit:	17	16	15	14	13	12
Unit						
0	1	1	1	0	0	0
1	1	1	0	0	0	1
2	1	0	1	0	1	0
3	1	0	0	0	1	1
4	0	1	1	1	0	0
5	0	1	0	1	0	1
6	0	0	1	1	1	0
7	0	0	0	1	1	1

THUMBWHEEL DISPLAY LOCATION 482: ILD Sense Bytes (if ILD Error)

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---------- Sense Byte 06 ----------|---------- Sense Byte 07 ----------|----- Sense Byte 08 -----|
            |           |           |  Format   |  Message  |           Format 1
            Emulated    Emulated Head  Decode      Decode
            Cyl.MSBs    Number      (Format/Message Decode - See Figure 8-2)
```

Bit	Bit
05 - Seek Incomplete	02 - Pack Change
04 - Seek Complete	01 - Busy
03 - Online	

THUMBWHEEL DISPLAY LOCATION 483: ILD Sense Bytes (if ILD Error)

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 09, Format 1 -----|----- Sense Byte 10, Format 1 -----|-Sense Byte 11, Format 1-|
                                                                          Drive Status at Error Time
```

Bit	Bit	Bit
30 - HSSM Test Failure	17 - Access Ready	07 - Permanent Seek Error/Fault
	12 - Head Load	

THUMBWHEEL DISPLAY LOCATION 484: ILD Sense Bytes (if ILD Error)

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----- Sense Byte 12, Format 1 -----|----- Sense Byte 13, Format 1 -----|Sense Byte 14, Format 1,2|
                                                Physical Drive #
```

Bit	Bit	Bit
29 - Read Only	07 - Seek End	03 - Fault
26 - No Drive Clocks	06 - Busy	02 - Seek Error
	05 - Selected	01 - On Cylinder
	04 - Write Protected	00 - Ready

THUMBWHEEL DISPLAY LOCATION 485: ILD Sense Bytes (if ILD Error)

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|---- Sense Byte 15, Format 1,2 ----|---- Sense Byte 21, Format 1,2 ----|Sense Byte 8, Format 4,5 |
                                                                          Actual Cyl. MSBs
```

Bit	Bit	Bit
31 - Mod. Select	27 - Tag 8	17 - Drive Fault
30 - Tag Gate	26 - Tag 4	13 - Write Inhibit
29 - Valid Check	25 - Tag 2	
28 - Enable Tag	24 - Tag 1	

THUMBWHEEL DISPLAY LOCATIONS 486 through 489: ILD Sense Bytes (if ILD Error)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0

Display Location			
486	Sense Byte 9, Format 4,5 Actual Cyl. LSBs	Sense Byte 10, Format 4,5	Sense Byte 11, Format 4,5 Actual Head #
487	Sense Byte 12, Format 4,5 Actual Record	Sense Byte 13, Format 4,5	Sense Byte 14, Format 4,5
488	Sense Byte 15, Format 4 SM Error Retry Count	Sense Byte 16, Format 4 See Sense Byte 4 breakdown	Sense Byte 15, Format 5
489	Sense Byte 16, Format 5 Record Length MSB	Sense Byte 17, Format 5 Record Length LSB	Sense Byte 21, Format 5 ECC Correction MSB

THUMBWHEEL DISPLAY LOCATION 48A: ILD Sense Bytes (if ILD Error)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 22, Frmt 5 ECC Correction LSBs			Sense Byte 21, Format 6			Sense Byte 8, Format 2		

Bit		Bit	
07	HAIO Parity Error 1	03	U Bus -- HAIO Parity
06	HAIO Parity Error 2	02	WMA Test Failure (See Display Location 48B)
05	HAIO Parity Error 3	01	MDB U-DMA Check
04	HAIO Parity Error 4	00	Unable to Select HAIO

THUMBWHEEL DISPLAY LOCATION 48B: ILD Sense Bytes (if ILD Error)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 9, Format 2			Sense Byte 10, Format 2			Sense Byte 11, Format 2		

Bit		Bit		Bit	
31	ALU Failure	19	XMCP Detected U Bus PE (0-17)	07	XRB Memory PE
30	HSSM Test Failure	18	XMCP Detected U Bus PE (18-35)	06	XRB Detected CT Bus PE
29	HAIO Sequencer Error	17	XMCP Detected CT Bus PE	05	XRB Inst. PE
28	DIFP FIFO Check	16	XRB No Find	04	XRB Not Available
27	MDBP SM-DMA Check	15	HSSM Detected U Bus PE	03	HSSM Busy Timeout
26		14	SMB to XMCP PE	02	HSSM Detected CT Bus PE
25	WMA/HSSM Test	13	HSSM/WMA Inst. PE	01	HSSM Internal PE
24	Failure Code*	12	DIFP PE	00	HSSM Buffer Memory PE

* If Display Location 48A bit 2=1, use WMA Test Failure Codes;
if Display Location 48B bit 30=1, use HSSM Test Failure Codes.

HSSM Test Failure Code

0 - See other bytes
1 - Word-to-byte miscompare
2 - Byte-to-word miscompare
3 - DMA failure (early complete)
4 - U-side DMA failure (no complete)
5 - Header flag miscompare
6 - ODR or IDR tag missing
7 - Undefined error

UMA Test Failure Code

0 - See other bytes
1 - No ECC uncorrectable status on write
2 - Data miscompare (good data is always 0)
3 - Early write complete (all words not written)
4 - Complete interrupt not received
5 - No ECC correctable status on read
6 - ODR or IDR tag missing
7 - Undefined error

THUMBWHEEL DISPLAY LOCATION 48C: ILD Sense Bytes (if ILD Error)

35 34 33 32	31 30 29 28	27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
Sense Byte 12, Format 2			Sense Byte 16, Format 2			Next Cylinder		

Bit		Bit		Bit	
31	XRB Invalid Cache Address	27	WMAP PE	18	Read Data Transfer
30	OCP PE	26	WMCM PE	15	Write Data Transfer
29	OCP Not Available	25	WMAP CT-Bus PE	13	Read Header
28	WMC Select Error	24	WMAP U-Bus PE	12	Read Verify

THUMBWHEEL DISPLAY LOCATIONS 48D - 48F

35 34 33 32 31 30 29 28	27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0

Display Locations			
48D	Pushed-Off Track Upper Address	Pushed-Off Track Lower Address	Seek-Only Flag
48E	ILD Next Record Save	ILD Return 4 MSB	ILD Return 4 LSB
48F	---------- R5 Save If ILD Error ----------		ILD Error Retry Count

THUMBWHEEL DISPLAY LOCATIONS 4C0 through 4CF

Display Locations	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
4C0	---------- READ1TRK & WRIT1TRK Main Return Location ----------			Caching Status[1]
4C1	---------- Caching Read/Write Return Location ----------			ILD Max Drive Cylinder
4C2	Save Cylinder Before Caching	Save Head Before Caching		Save Starting Word Before Caching
4C3	R15 Save RD & WR 1TRK	---------- Save Transfer Length Before Caching ----------		
4C4	Seek Started Flag	Save Record Before Caching		Caching Retry Counter
4C5	---------- R14 Save Before Caching ----------			Not Used
4C6	Save Cache Cylinder Before Caching	Save Cache Unit/Head Before Caching		Save Cache Track Number Before Caching
4C7	WMA ECC Status[2]	Save Cylinder for Track to Cache		Save Unit/Head for Track to Cache
4C8	Emulated Cylinder Save LSB	Emulated Cylinder (MSB) and Head Save		Emulated Record Save
4C9	WAITSEEK Return Location MSBs	---------- Initial Cache/SSS Address ----------		
4CA	Saved Emulated Record Number	RIO Temporary Save		OCP Command[3]
4CB	Requested Unit (State Change)	Requested State (State Change)		Present State
4CC	1/8 Cache Disk Lowest Address(MSB)	---------- Command Relative Address ----------		
4CD	Not Used	---------- Saved Next U-Start Address ----------		
4CE	---------- Format & Cache Prep Date ----------			
→ 4CF	---------- Data Miscompare Bad Data ----------			

[1] 4C0 Caching Status
- Bit 6 Caching Error
- Bit 5 WMA ECC Error
- Bit 4 Push Off Track
- Bit 3 Intermediate Bypass Track
- Bit 2 Write-Through
- Bit 1 Cache to/from HAIO
- Bit 0 Caching Mode

[2] 4C7 WMA ECC Status
- Bit 1: ECC Uncorrectable
- Bit 0: ECC Two-bit Correctable

[3] 4CA OCP Command: See breakdown for Display Location 4A7

THUMBWHEEL DISPLAY LOCATION 4D0 - 4D6: External Functions

	35	34 33 32 31 30 29	28 27 26 25	24 23 22 21 20 19 18	17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
	1	0 ---------- 0	--Disk Unit--	- Command Code ---	0 0	-------- Word Transfer Length -------- OR Backing Factor

see p 6.11F

Command Chart

Command Type	Command	Octal Code	Hex Code Bits (18-23)	Command Function Word	Address Function Word
CONTROL	Sector Position Relative Seek	53	2B	X	X
	Track Position Relative Seek	13	0B	X	X
	Seek	07	07	X	X
	Seek and Set Sector	47	27	X	X
	Recalibrate	23	13	X	
	No Operation	03	03	X	
WRITE	Write Home Address and RO Special	65	35	X	X
	Write Home Address and Record Zero	25	15	X	X
	Prep Track	01	01	X	X
	Prep Cylinder	41	21	X	X
	Write Data	15	0D	X	X
	Write Data and Pad Zeros	11	09	X	X
	Alternate Defective Track	31	19	X	X
READ	Read Initial Program Load	00	00	X	
	Read Full Track	26	16	X	X
	Read Home Address Special	66	36	X	X
	Read Count	22	12	X	
	Space Count and Read Data	46	26	X	X
	Read Data	16	0E	X	X
	Read Data Special	76	3E	X	X
	Read Verify	12	0A	X	X
	Read Label	62	32	X	
SENSE	Sense I/O	04	04	X	
	Read and Reset Buffered Log	44	24	X	
	Read Configuration	64	34	X	
	Read Buffered Record	24	14	X	
	Read and Reset Drive Error Counters	54	2C	X	

THUMBWHEEL DISPLAY LOCATION 4D7: Total E.F. Count (Reset by sub-system clear)

```
|           |           |           |           |           |           |           |           |
|35 34 33 32|31 30 29 28|27 26 25 24|23 22 21 20|19 18 17 16|15 14 13 12|11 10 9 8|7 6 5 4|3 2 1 0|

|----------------------------- Count of External Function Commands -----------------------------|
```

THUMBWHEEL DISPLAY LOCATION 4D8 - 4DE: Relative Word Address

```
|                       |                       |                       |                       |
|35 34 33 32 31 30 29 28|27 26 25 24|23 22 21 20|19 18|17 16 15 14 13 12 11 10 9 8|7 6 5 4 3 2 1 0|

|0 ------------------0|------------------------ Relative Word Address ----------------------|
                                                        OR
                      |---------- Cylinder ----------|0 --------- 0|--- Head ---|  (See Note)  |
                              (Absolute Address)
```

Note: Normally zero except: Seek and Set Sector = Sector Number
Space Count and Read Data = Record Number

THUMBWHEEL DISPLAY LOCATION 4E0 - 4E6: Last External Interrupt Words

```
|           | | |           |           |           |     |                       |     |           |
|35 34 33 32|31|30|29 28 27 26|25 24 23 22|21 20 19 18|17 16|15 14 13 12 11 10 9 8|7 6 5|4 3 2 1 0|

|0 ------- 0|CT| 0|---Status--|0 ------- 0|--Recovery-|0 - 0|---Device Status-----|0 0 0|Drive No.|
|If all ones| *       Action                Action                (see below)
|= EI Time  |        (see below)        (see Display Location
|  Out      |                            401, bits 24-35)
```

*CT = Channel Truncation

Status Action Codes		Status Action Codes		Device Status	
0	Invalid Code	7	Sense Completed	15	Attention
1	Pack Change	8	Sense I/O Completed	14	Status Modifier
2	Read Label Command	9	C.T. on Sense Command	13	Control Unit End
3	EF/EI Collision	A	Channel Truncation	12	Busy
4	Seek Initiated	B	Acquire Sense Bytes for Unit Check	11	Channel End
5	Seek Completed	D	Bus Out Parity Error	10	Device End
6	Read or Write Completed	E	Correctable Data Check	9	Unit Check
		F	Forced EF Termination	8	Unit Exception
					(Not Used)

THUMBWHEEL DISPLAY LOCATION 4E7

```
|  |                       |  |                       |  |                       |  |           |
|35|34 33 32 31 30 29 28 27|26|25 24 23 22 21 20 19 18|17|16 15 14 13 12 11 10 9|8|7 6 5 4 3 2 1 0|

|0 ------- 0|31---------------------------- Drives on Cylinder ---------------------------- 0|
                        Bit Position Equals Logical Drive Number
```

THUMBWHEEL DISPLAY LOCATION 4E8: Last Channel Sense Bytes

```
|  |                          |  |                          |  |                          |  |                |
|35|34 33 32 31 30 29 28 27|26|25 24 23 22 21 20 19 18|17|16 15 14 13 12 11 10 9|8|7 6 5 4 3 2 1 0|

|0 |---- Sense Byte 0 -----| 0|---- Sense Byte 1 -----| 0|--- Sense Byte 2 -----|0|  Sense Byte 3 |
```

Bit	Bit	Bit
34 - Command Reject	28 - Track Cond. Check	21 - No Record Found
33 - Intervention Required	27 - Seek Check	19 - Write Inhibited
32 - Bus Out Parity	25 - Permanent Error	15 - Correctable Data Check
31 - Equipment Check	24 - Invalid Track Format	13 - Environ. Data Present
30 - Data Check	23 - End of Pack	3-0- Recovery Action[1]

[1]Same as Display Location 401, bits 24-35.

THUMBWHEEL DISPLAY LOCATION 4E9: Last Channel Sense Bytes

```
|  |                          |  |                          |  |                          |  |                |
|35|34 33 32 31 30 29 28 27|26|25 24 23 22 21 20 19 18|17|16 15 14 13 12 11 10 9|8|7 6 5 4 3 2 1 0|

|0 |---- Sense Byte 4 -----| 0|---- Sense Byte 5 -----| 0|--- Sense Byte 6 -----|0|  Sense Byte 7 |
                              Emulated Cyl. LSB
```

Bit	Bit	Bit
34-33 - String Number	32-30 Drive # (Complemented)	7-4 Format Decode[2]
00 = Drives 0-7	29-27 Drive #	3-0 Message Decode
01 = Drives 8-15	16-14 Emulated Cyl. 3 MSB	
10 = Drives 16-23	13-9 Emulated Head	[2] The format decode determines
11 = Drives 24-31		the meaning of sense bytes 18-23.

THUMBWHEEL DISPLAY LOCATIONS 4EA, B, C, and D: Last Channel Sense Bytes

```
|  |                          |  |                          |  |                          |  |                |
|35|34 33 32 31 30 29 28 27|26|25 24 23 22 21 20 19 18|17|16 15 14 13 12 11 10 9|8|7 6 5 4 3 2 1 0|

|0 |---- Sense Byte -------|0 |----- Sense Byte -----|0 |------ Sense Byte ----|0|--Sense Byte --|
|       (see # below)              (see # below)              (see # below)        (see below)
```

Display Location				
4EA	8	9	10	11
4EB	12	13	14	15
4EC	16	17	18	19
4ED	20	21	22	23

CACHE

THUMBWHEEL DISPLAY LOCATIONS 4EE through 4FF

Display Locations	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
4EE	Max Emulated Cylinder	Max Emulated Head	Max Emulated Record	
4EF	Record Length	1/4 Emulated Head Multiplier	1/4 HSSM Buffer Capacity	
4F0	Max Record Number in MDB	1/4 Emulated Cylinder Divisor		
4F1	Max Actual Usable Cylinder	Max Actual Cylinder	Max Actual Head	
4F2	Max Actual Record	1/4 Actual Cylinder Divisor		
4F3	1/4 Words Per Track	1/4 Max Words Per Track	Records Read/Written	
4F4	SM-Timer LSBs	U-Timer LSBs	Emulated Record Number	
4F5	---------- Max Relative Word Number ----------			
4F6	SM-Timer MSBs	U-Timer LSBs	SM Done Interrupt Prcsng. Return Location (MSB)	
4F7	SM Done Interrupt Processing Return Location LSBs	Advance to Next Record Jump Location	Saved Next XMCI Jump Location	
4F8	---------- R1 Temporary Save ----------		R2 Temporary Save	
4F9	R3 Temporary Save	---------- R5 Temporary Save ----------		
4FA	---------- Q Register Temporary Save ----------		INITSEEK Return MSB	
4FB	WAITSEEK Return LSB	R6 Temporary Save	Track-Hold Counter	
4FC	2-Drives-Per-Unit Flag	WMA ECC Test Flags	INITSEEK Return LSB	
4FD	Initial Emulated Cylinder LSB	Initial Emulated Cylinder (MSB) & Head Initial Word Number		
4FE	---------- Initial Actual Cylinder ----------		Initial Actual Head	
4FF	Initial Actual Record	---------- ILD Return 5 ----------		

THUMBWHEEL DISPLAY LOCATIONS 500 THROUGH 50F (except 502,503,504, and 507 which follow)

Display Location	35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
500	XRB Cache Address	SSS Format Transfer Length	XRB Scan Pointer
501	XRB Search Unit	XRB File Max Switch Setting	XRB Address
505	Cache Prep Return Location-MSB	Initial WMA Device #	WMA Function Word
506	WMA Starting Device #	WMA Starting Address - MSB	WMA Starting Addr.-LSB
508	Cache Prep Return Loc.-LSB	Cache Transfer Length - MSB	Cache Trans. Length-LSB
509	Lamp Test - all bits lit	Lamp Test - all bits lit	Lamp Test-all bits lit
50A	XRB Write Error Retry Count	XRB Read Error Status	XRB Read Error Count
50B	WMA Error Device #	WMA Error Address - MSB	WMA Error Address - LSB
50C	WMC Error Device #	WMC Error Address - MSB	WMC Error Address - LSB
50D	XRB Bad Data (Track #)	XRB Bad Data (Cylinder #)	XRB Bad Data(unit/head)
50E	XRB Bad Data (Flags)	XRB Read Error Retry Count	XRB Write Data (Flags)
50F	XRB Write Data (Track #)	XRB Write Data (Cylinder)	XRB Write Data (Unit/Head)

CACHE

THUMBWHEEL DISPLAY LOCATION 502

```
|                                   |                           |                           |
|35 34 33 32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17 16 15 14 13|12 11 10 9 8 7 6 5 4 3 2 1 0|

|---------- XRB Function ----------|-----XRB Write Error History----|---XRB Write Error Count----|
```

Bits 27-24 Decode:

Hex Value	Description	Hex Value	Description
0	Initialize Track	5	Get Filemax
1	Search	6	Invalidate Tracks
2	Read Entry	7	Search Write Op
3	Write Entry	8	Search for Preseek Track
4	Find Oldest Write (Backscan)	9	Invalidate all Tracks
		A	Search for a Cache Address

THUMBWHEEL DISPLAY LOCATION 503

```
|       |                           |                           |                           |
|35 34 33|32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17 16 15|14 13 12 11 10 9 8 7 6 5 4|3 2 1 0|

|------------ XRB Status ----------|---------------- XRB Handler Return Location --------------|
```

Bit		Bit	
32	· XRB data miscompare	28	· No Valid Bit Set[1]
31	· No writes in cache	27	· XRB memory parity error
30	· No-find	26	· CT bus parity error
29	· XMC CT-Bus Parity	25	· Instruction bus error
		24	· XRB not available

[1] Bit 35 missing; see Display 800-BFF.

THUMBWHEEL DISPLAY LOCATION 504

```
|       |                           |                                   |                     |
|35 34 33|32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17 16 15 14 13 12 11|10 9 8 7 6 5 4 3 2 1 0|

|----------- WMA Status -----------|------WMA Return Location · MSB-------|-WMA Return Loc.· LSB-|
```

WMA Status

32	No history flag (not displayable; used as an internal flag)	28	2-bit correctable ECC
31	Prep. error	27	Uncorrectable ECC
30	ECC error	26	Cache select error
29	WMA fault (usually parity)	25	Invalid address
		24	Cache select timeout

CACHE

THUMBWHEEL DISPLAY LOCATION 507

35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

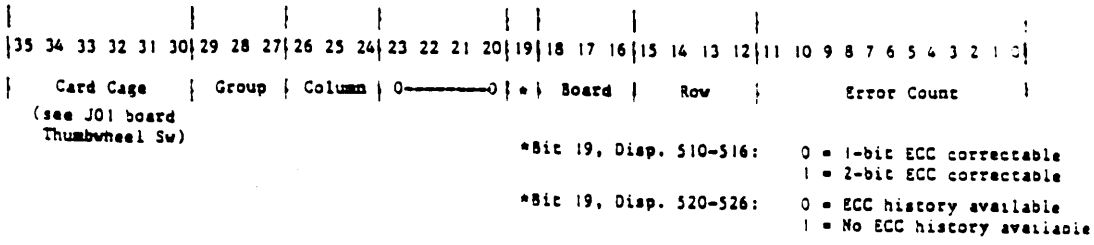
Bit	
34	Parity error detected by WMC (see bits 24-31)
33	No acknowledge (sets bit 17)
32	WMA parity error detected on bus from WMC
31	Memory board 4 parity
30	Memory board 3 parity
29	Memory board 2 parity
28	Memory board 1 parity
27	Memory board 0 parity
26	WMC data parity ("or" of bits 27-31)
25	WMC tag parity (sets bit 20)
24	WMC control bus parity (sets bit 20)
23	Write memory parity detected by memory (see bit 26)
22	ECC correctable
21	ECC uncorrectable
20	Parity detected by WMC during tags (see bits 24,25)
19	CT-bus parity

Bit	
18	No selection (no response to select tag)
17	No response to tag gate
16	No compare
15	Parity error detected by WMA during tags
14	History parity error
13	Read memory parity error (unload)
12	U-bus parity error (load)
7	Selection error (see bits 15-18, 20)
6	Tag completion
5	Data loaded into memory output register to memory (load)*
4	Data loaded into n-register (load)*
3	Data loaded into input register from u-bus (load)*
2	Data loaded into memory input register from memory (unload)*
1	Data loaded into f-register (unload)*
0	Data loaded into output register to u-bus (unload)*

* These bits are internal flags and do not indicate errors conditions.

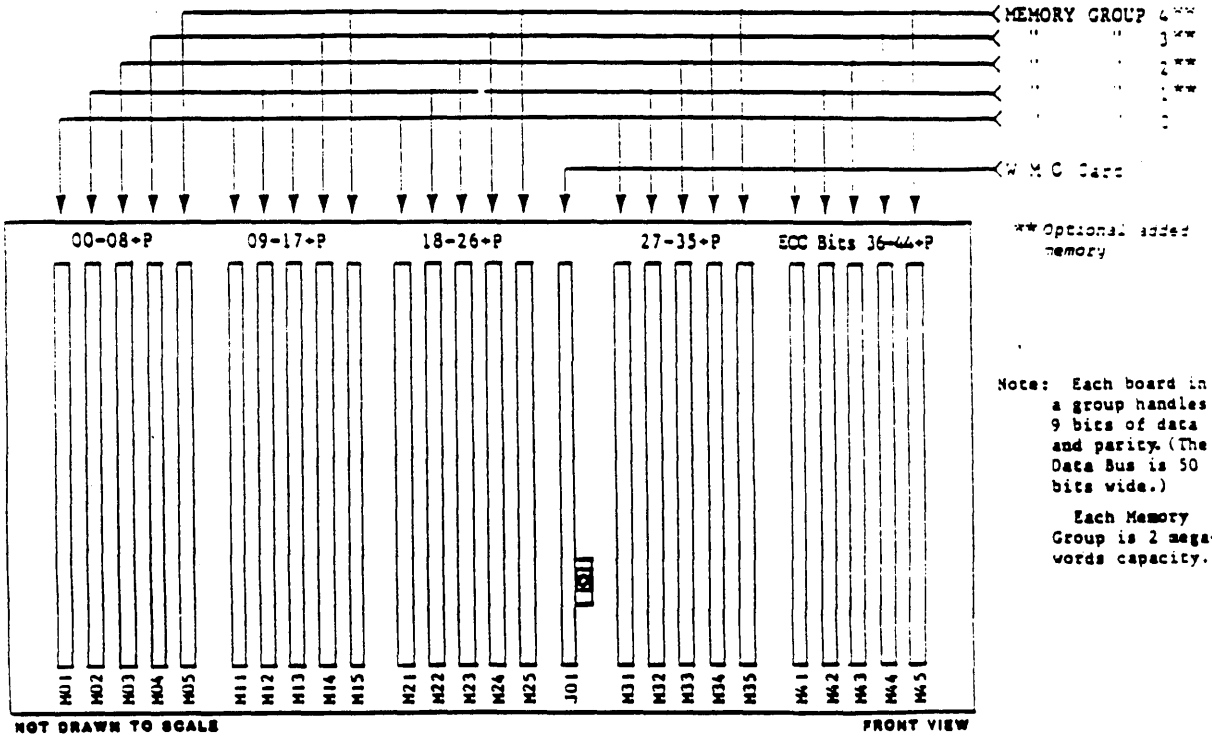
THUMBWHEEL DISPLAY LOCATION 510-516
MEMORY MODULE CORRECTABLE ECC DISPLACEMENT

THUMBWHEEL DISPLAY LOCATION 520-526
MEMORY MODULE UNCORRECTABLE ECC DISPLACEMENT



*Bit 19, Disp. 510-516: 0 = 1-bit ECC correctable
1 = 2-bit ECC correctable

*Bit 19, Disp. 520-526: 0 = ECC history available
1 = No ECC history available



** Optional added memory

Note: Each board in a group handles 9 bits of data and parity. (The Data Bus is 50 bits wide.)

Each Memory Group is 2 mega-words capacity.

CACHE/SOLID STATE STORAGE CARD CAGE

FAILING BOARD/CHIP LOCATION

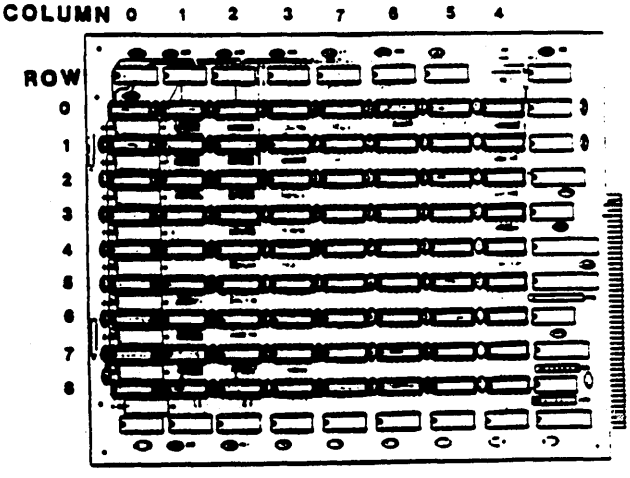
Using Group and Board numbers from Disp 510-516 or 520-526, find failing board location in matrix below. The chart above shows physical location within the failing card cage (bits 30-35).

Use Column and Row from Disp. 510-516 and the Memory Card chart (right) to locate failing chip. Fixing all ECC correctables will sometimes change an ECC uncorrectable to a correctable ECC error. (Column and Row are not valid in Disp. 520-526)

Group Number

Board #	0	1	2	3	4
0	M01	M02	M03	M04	M05
1	M11	M12	M13	M14	M15
2	M21	M22	M23	M24	M25
3	M31	M32	M33	M34	M35
4	M41	M42	M43	M44	M45

MEMORY BOARD LOCATION MATRIX



MEMORY CARD

CHIP LOCATION CHART

THUMBWHEEL DISPLAY LOCATION 517: Count of Memory Module Correctable ECCs

```
|                                                                                 |
|35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0|
|·····------------------- Total Count of Correctable Memory Module ECC Errors ------------------·····|
```

THUMBWHEEL DISPLAY LOCATION 518

```
|                                                                                 |
|35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0|
|·····------------------------------- ECC Error Assembly Word -------------------------------·····|
```

THUMBWHEEL DISPLAY LOCATION 519

```
|                                 |                                 |                 |
|35 34 33 32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17 16 15 14 13|12 11 10 9 8 7 6 5 4 3 2 1 0|
|·····------------Not Used------------|---------Last ECC Address-------|----Last ECC Displacement---|
```

THUMBWHEEL DISPLAY LOCATION 51A

```
|                                 |                                 |                 |
|35 34 33 32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17 16 15 14 13|12 11 10 9 8 7 6 5 4 3 2 1 0|
|0 ------- 0|---------------- Sector Polling Mask; bit Position = Logical Drive # ----------------|
```

Data Buffer Address Calculation

THUMBWHEEL DISPLAY LOCATIONS 51B THROUGH 51F

```
|                                 |                                 |           |       |
|35 34 33 32 31 30 29 28 27 26 25 24|23 22 21 20 19 18 17 16 15 14 13 12|11 10 9 8 7 6 5 4|3 2 1 0|
|                                 |                                 |           |       |
```

Display Location			
51B	Next SM DMA Address MSB	Next SM DMA Address LSB	Not Used
51C	Bad SM DMA Address MSB	Bad SM DMA Address LSB	Not Used
51D	Expected U DMA Address MSB	Expected U DMA Address LSB	Only Valid Copy Flag
51E	Bad U DMA Address MSB	Bad U DMA Address LSB	End U DMA MSBs (Read)
51F	Good U DMA Address MSB	Good U DMA Address LSB	End U DMA LSBs (Read)

THUMBWHEEL DISPLAY LOCATIONS 520 through 526 (See Display Locations 510-516)

THUMBWHEEL DISPLAY LOCATION 527: Count of Memory Module Uncorrectable ECCs

```
|                                                                                 |
|35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0|
|·····-------------------- Total Count of Uncorrectable Memory Module ECC Errors --------------------·····|
```

THUMBWHEEL DISPLAY LOCATIONS 528 THROUGH 532

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4 3 2 1 0
Drive Flags Unit (see # below)	Drive Flags Unit (see # below)	Drive Flags Unit (see # below)

Display Location			
528	0	1	2
529	3	4	5
52A	6	7	8
52B	9	10	11
52C	12	13	14
52D	15	16	17
52E	18	19	20
52F	21	22	23
530	24	25	26
531	27	28	29
532	30	31	Data Copy Unit

For each display there are 12 bits which describe the characteristics of the drive. They are broken down as follows:

Bits 1-3 comprise an octal digit which indicates drive type:

0 = Undefined
1 = Fujitsu Eagle
2 = CDC513
3 = M2333
4 = M2382 (Swallow 5)
5 = M2344 (Swallow 4)
6 = MPI9720
7 = MPI 9720 with Defect Tracks

BIT 7 = ?

Bits 4 and 5 comprise an octal digit which indicates record length:

0 = Undefined
1 = 112-word prep-116
2 = 448-word prep
3 = 1792-word prep

Bit 10: if bit 10 = 0, there is one physical drive per logical unit;
if bit 10 = 1, there are two physical drives per logical unit.

SOLID STATE STORAGE

THUMBWHEEL DISPLAY LOCATION 533

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
SSS Unit Size (megawords)	Not Used	Not Used	

THUMBWHEEL DISPLAY LOCATIONS 534 and 535

Reserved for Future Use

THUMBWHEEL DISPLAY LOCATIONS 536 THROUGH 540

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
Saved Unit/Head per drive # (see # below)	Saved Unit/Head per drive # (see # below)	Saved Unit/Head per dr.# (see # below)	

Display Location			
536	0	1	2
537	3	4	5
538	6	7	8
539	9	10	11
53A	12	13	14
53B	15	16	17
53C	18	19	20
53D	21	22	23
53E	24	25	26
53F	27	28	29
540	30	31	(Not Used)

*Bit 35,23, or 11 = Do not cache this track.

CACHE

THUMBWHEEL DISPLAY LOCATIONS 541 THROUGH 548

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0
Saved Track # per Drive[1] OR Saved Sector # per Drive[2]	Saved Track # per Drive[1] OR Saved Sector # per Drive[2]	Saved Tr.# per Drive[1] OR Saved Sector # per Drive[2]	

Display Location			
541	0	1	2
542	3	4	5
543	6	7	8
544	9	10	11
545	12	13	14
546	15	16	17
547	18	19	20
548	21	22	23
549	24	25	26
54A	27	28	29
54B	30	31	(Not Used)

[1] This definition applies to these display locations only when the system is in CACHE mode.
[2] This definition applies to these display locations only when the system is in BYPASS mode. (Bit 34, 22, or 10 set indicates a sector number instead of a track number.)

THUMBWHEEL DISPLAY LOCATIONS 54C THROUGH 54F

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0

Display Location			
54C	Device End Delay Timer	Last Drive Flag Byte	Saved Record for Write-Thru
54D	Saved Head for Write-Thru	Transfer Length MSBs for Write-Thru	Transfer Length LSBs for Write-Thru
54E	Starting Word # for Write-Thru	R12 Temporary Save	R9 Temporary Save
54F	First Record # after Index	Backscan Holdoff Counter (Secondary)	Minimum Read Backing Factor

THUMBWHEEL DISPLAY LOCATIONS 550 - 553: HSSM Confidence Test

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0

Display Location	
550	Reference Word 0
551	Reference Word 1
552	Reference Word 2
553	Reference Word 3

THUMBWHEEL DISPLAY LOCATION 554

Reserved for Future Use

~ DOES NOT ALWAYS DISPLAY CORRECTLY !

THUMBWHEEL DISPLAY LOCATION 555: Confidence Test Error Display

35 34 33 32 31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12	11 10 9 8 7 6 5 4	3 2 1 0

Bit	
28	XRBP Failure
27	XMCP/XM16KP Failure
26	OCP Failure
25	HSSM Failure
24	WMAP Failure

THUMBWHEEL DISPLAY 800-BFF: XRBP Entry Format bits 35-00

35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Cache Track Address											Cylinder												Unit					*	Head					

* If bit 05 = 1, Valid XRB Entry; if bit 05 = 0, Not Valid XRB Entry.

OCP PROGRAM D (MSG) THUMBWHEELS at 800-BFF: XRB Entry Format Bits 43-36
(Read Off of OCP Display Panel)

Bits	
43	Preseek in Progress
41	Uncorrectable ECC Error on Data Copy
40	Cache Track Suspended; two-bit Correctable Error
39	Track Hold Flag
37	Interval Timer Flag
36	Write Operation; Cache is only current copy

XmCP
EXX — microcode address

8.7 CDC General Status

GENERAL STATUS

Bit	Definition
11	Abnormal termination. Preceding function terminated abnormally. General status bits 8 and 9 indicate whether recovery is possible. Detailed status shows cause of abnormal termination.
10	Multiple-access controller reserved. Controller is reserved to another PP channel. All other status bits are meaningless.
9	Nonrecoverable error. Controller detected error from which no recovery is possible. Detailed status identifies error.
8	Recovery in process. Controller is ready to attempt error recovery in response to 0014 (continue) function.
7	Checkword error. Controller detected checkword error in address field or data field of sector. Detailed status word 2, bits 8 through 11, provides error analysis.
6	Correctable address error. Controller detected correctable read address checkword error. 0014 (continue) function enables data to be processed on subsequent disk revolution.
5	Unused.
4	Drive malfunction. Drive-related error occurred. Detailed status reflects drive status at time of malfunction.
3	Drive reserved. Requested drive is reserved by other controller.
2	Autoload error. Controlware loaded is not compatible with controller.
1	Busy. Controller and/or requested drive are busy.
LSB 0	Unused.

11 10 9 8 7 6 5 4 3 2 1 0

8.8 CDC Detailed Status

OCTAL

C D C EXTENDED STATUS REPORT

WORD	11	10	9	8	7	6	5	4	3	2	1	0
CDC	STROBE/OFFSET RETRY COUNT								ADDRESS ERROR	CYLINDER # ERROR	TRACK # ERROR	SECTOR # ERROR
									SB[1:2]	MSG[1:A] MSG[1:6]	SB[0:6] SB[1:1]	SB[1:4]
CDC -2 AMP	ADDRESS CKWD ERR	BAD ADDR CKWD ERR	DATA CKWD ERR	BAD DATA CKWD ERR	HDA SEQ. COMPLETE	SEQUENCE LATCH 4	SEQUENCE LATCH 2	SEQUENCE LATCH 1	SEQUENCE CHECK LA	STOP HDA CYCLE	AIR SWCH LATCH	MOTOR @ SPEED SW
	F[1,2,OR 4]	F[1,2,OR 4]		//////////	//////////	//////////	//////////	//////////	//////////	//////////	//////////	//////////
CDC -3 AMP	CURRENT FUNCTION BITS 7-0								ILLEGAL PARAMTR	ILLEG. # OF PARMS	ERR RATE EXCEEDED	//////////
									//////////	//////////	//////////	INTERVEN REQUIRED
CDC -4 AMP	////////// //////////	7155 SUBSYS..	CONTROLWARE REVISION NUMBER 1 0 1 1						DRIVE NUMBER BITS 5-0			
	////////// //////////	//////////	//////////						//////////			
CDC -5 AMP	TRACK FLAW	FACTORY FLAW MAP	//////////						CYLINDER NUMBER BITS 9-4 (HIGH)			
		////////// //////////	RECOVERY ACTION						//////////			
CDC -6 AMP	CYLINDER NUMBER BITS 3-0 (LOW)								TRACK NUMBER BITS 7 - 0			
									//////////			
CDC -7 AMP	LOGICAL SECTOR NUMBER 7 - 0								READY & SAFE	SYSTEM MNT MODE	DRIVE NUMBER BITS 7 - 6	
									*SB[0:1] NO INTER REQ	////////// //////////	//////////	
CDC -8 AMP	DRIVE NUMBER BITS 5 - 0								////////// //////////	WRITE ENABLE	ONLINE	AIR SWITCH
									////////// //////////	*SB[1:6] NOT WRITE INHIBITED	*SB[0:1] NO INTER REQ	////////// //////////
CDC -9 AMP	INDEX	SCTR MRK ON SECTR	ON CYLINDER	SELECTED & RSERVD	READY AND SAFE	ON SECTOR	STATUS VALID	STATUS PRTY ERR	SEEK T.O. ERR	SEEK OVR ERROR	SERVO OFF TRAK	REZERO MODE LCH
	////////// //////////	DEVICE END	DEVICE END		*SB[0:1] NO INTER REQ	DEVICE END		////////// //////////	////////// //////////	////////// //////////	////////// //////////	////////// //////////
CDC -10 AMP	SERVO LATCH	LIN MODE LATCH	CONTROL LATCH	WAIT LATCH	LAST SEEK FWD	GUARD PTRN X	TARGET VELOCITY	TARGET CROSSING	////////// //////////		ODD TRACK	ON CYLINDER
	////////// //////////	////////// //////////	////////// //////////	FORMAT NUMBER DECODE				MESSAGE NUMBER DECODE				DEVICE END

IF THE HP/A DETECTS A CYLINDER ERROR, IT SETS BIT 1
IF HP/A DETECTS A SECT/TK ERROR, IT SETS BITS, 0, 1, AND 3

IF HP/A DETECTS A CHECKSUM ERROR IT SETS BITS 10 AND 9
IF HP/A HAS A WRITE ERROR BIT 11 WILL SE

IF HP/A DETECTS THE CYLINDER OUT OF RANGE IT SETS BIT 3

IF HP/A READS A FLAWED OR PROTECTED SECTOR BIT 11 IS SET

////// = INDICATES FLD. NOT CHANGED

NUMBERS INDICATE INTRNCT VAL.

AMPLIF SENSE BYTE 7

C D C EXTENDED STATUS REPORT

WORD	11	10	9	8	7	6	5	4	3	2	1	0
CDC 11	CAPABLE ENAB ERR	WRITE OVERRUN	MULTIPLE HEAD ERR	WRITE CRNT ERR	WRITE TRANSIT	CONTROL ERROR	INDEX CHECK	HEAD SHORT	I/O NO CONTROL	WRITE IN OFFSET	////	////
AMP	EQUIP CHECK	////	////	////	////	////	////	////	////	////	////	////
CDC 12	EARLY STROBE	LATE STROBE	FORWARD OFFSET	////	////	SECTOR CMPR ERR	DRIVE ERROR	////	READ/WRI ERROR	////	////	ACCESS CHECK
AMP	////	////	////	////	////	////	////	////	DATA CHECK	UNIT CHECK	////	////
CDC 13	BUFFR TO DISK ERR	ACC CONN B4 GEN'L	DRIVE B4 CONNECT	////	SENSE BYTE 8							
AMP		?	?	ERR HP/A DETECTED								
CDC 14	SENSE BYTE 9								SENSE BYTE 10 a UPPER NIBBLE			
CDC j	SENSE BYTE 10 4 LOWER NIBBLE				SENSE BYTE 11							
CDC 16	LOST DRV CLOCK	UNUSED BUT RESERVED			ECC RES. NONZERO	CHAN DAT PRTY ERR	PROCESS. INST T-O	LOST CNTRL WD	UP/DOWN CNT <> 0	PAK UNSF NOT REDY	BUFF OUT PRTY ERR	WRITE VRFY ERR
AMP	////	////			////	////	////	////	////	////	////	////
CDC 17	SYNC BYT SEARCH	SECTOR LEN BAD	LOST DATA	SYNC BYT MISCOMPR	CKWD ERR CRCN TRY	BUFF OUT REG FULL	BUFF INP REG FULL	CHANNEL RESERVED	DEADMAN TIMEOUT	CHANNEL ACTIVE	DATA FLD ERR	ADDRESS FLD ERR
AMP	////	SB[1:1] INVALID TRK FORMAT	////	////	////	////	////	////	////	////	////	////
CDC 18	D ADD C	C ADD B	B ADD A	A ADD 9	////	////	////	ECHO MODE	LARGE SECTOR	////	////	////
AMP					////	////	////	////	////	////	////	////
CDC 19	SENSE BYTE 12								UPPER NIBBLE OF SENSE BYTE 14 FOR FORMAT 4, SENSE BYTE 16			
CDC 20	LOWER NIBBLE OF SENSE BYTE 14				CONTROLLER HARDWARE UNIQUE IDENTIFIER							
AMP												

not modified

HP/A SETS BITS 9 AND 10.

HP/A WILL UPDATE BITS 8,9,10,AND11 FOR THE ACCESS CONNECTED

8.44

Note: For a tilde (~) please read "NOT"
SB[x:y] means Amperif Sense Byte Number x Bit y
MSG[j:k] means Amperif Sense Byte 7 Format j Message k
FSB[n:x:y] means Amperif Format n Sense Byte Number x Bit y
WD[m:n] means CDC Extended Status Byte m Bit n

Comments:

8.9 TO CONVERT FROM CDC CYL, TRK, SECT TO ~~SWALLOW~~ 4 PHYSICAL CYL, TRK, REC

SABER 5

CDCS CYL, TRK, SECTOR, CONVERT TO DECIMAL BEFORE USING FORMULA

$$\left((\text{CDC CYL} \times 1280) + (\text{CDC TRK} \times 32) + \text{CDC SECT}\right) \times 116 = \text{RWA}$$

(116 = WORD FACTOR (WORDS/RECORD))

3682072

$$\frac{\text{RWA}}{67 \times 116 \times 15} = \text{WHOLE \#1} + \text{FRACTION \#1}$$

31.584

67 = REC/TRACK; 116 = WDS/RECORD

$= \frac{\text{RWA}}{116580}$

WHOLE #1 = PHYSICAL CYL 31

FRACTION #1 × 15 = WHOLE #2 + FRACTION #2 .76

WHOLE #2 = PHYSICAL HEAD 8

FRACTION #2 × 67 = RECORD + 1 = RECORD

REC = 1 SECTOR IS SAME IN AMDEBUG

ex CYL 30_8 24_{10}
TRK 37 31
SEC 36 30

SABER 5 HAS 15 heads

$((24 \times 1280) + (31 \times 32) + 30) \times 116 = \text{RWA} = 3682072$

$\frac{3682072}{116580} = 31.58407$ CYL (31)

$.58407 \times 15 = 8.76$ → HEAD (8)

8.10 CDC Function Codes

SUBSYSTEM FUNCTIONS

Octal Code	Function	Words Output	Words Input	General Status Required
0000	Connect (1)	1		Yes
0001	Seek, 1:1 interlace (1)	4		Yes
0002	Seek, 2:1 interlace (1)	4		Yes
0004	Read		(6)	Yes
0005	Write	(6)		Yes 2
0006	Write verify	(6)		Yes 2
0007	Read checkword			Yes
0010	Operation complete			No
0011	Disable drive reserve			No
0012	General status		1	No
0013	Detailed status		12	No
0014	Continue	(6)(3)	(6)(4)	Yes
0015	Drop seeks			No
0016	Format pack (1)	7		Yes
0017	Return drive address		3	No
0020	Drive release			No
0021	Return cylinder address		1	No
0022	Set/clear flaw (1)	1		Yes
0023	Extended detailed status		20	No
0024	Read gap sector		(6)	Yes
0025	Write gap sector	(6)		Yes (2)
0026	Write verify gap sector	(6)		Yes (2)
0027	Read checkword gap sector			Yes
0030	Read factory data		322	Yes
0031	Read utility map		322	Yes
0032	Block transfer buffer read		322	No
0033	Block transfer buffer write (1)	322		Yes
0034	Read protected sector		322	Yes
0035	Write last sector	(6)		Yes
0036	Write verify last sector	(6)		Yes
0037	Write protected sector	322		Yes
0040	Read short		319 (5)	Yes
0041	Select strobe and offset (1)	1		Yes
0042	Clear connected access			No
0043	Buffer read		322	Yes
0044	Buffer write	322		Yes
0046	Write buffer to disk			Yes
0047	Scan cylinder addresses			Yes
0050	Output on processor channel (1)	3		Yes
0051	Execute control word sequence (1)	49		Yes

NOTES

(1) When PP channel deadman timer expires during this function, controller prepares 5000 general status and sets deadman timeout bit (word 17, bit 3) in detailed status.

(2) Except when executing this function at 2:1 interlace on 844 drive, controller returns general status before transferring data from buffer to disk. If error occurs during buffer-to-disk transfer, controller responds only to 0012 (general status) function. This ensures that buffer-to-disk errors do not go undetected.

(3) Following write-type function only.

(4) Following read-type function only.

(5) 844 only; use 318 for 885; 1360 for 885 large sector.

(6) 322 words for small sector, 1376 words for large sector 885.

SUBSYSTEM FUNCTIONS (Contd)

Octal Code	Function	Words Output	General Words Input	Status Required	Octal Code	Function	Words Output	General Words Input	Status Required
0052	Input processor channel status		32	No	0063	Input display data		64	No
0053	Echo output channels		32	No	0064	Time difference counter			No
0054	Issue processor flag pulse 1	1		Yes	0066	Force Error	1		Yes
0055	Enable input channel timing 1	1		Yes	0067	Interlock Autoload	16870		Yes
					01NN	Autoload from disk			No
0056	Input timing data		2	No	03NN	Disk deadstart			No
0057	Echo one word	1	1	No	0414	Autoload from PP	16870		Yes
0061	Autodump		12288	No	0720	Echo one word	1	1	No
0062	Manipulate processor	5		No					

7777 MASTER CLEAR

LAST CHANNEL FUNCTION

8.11 ERROR LOG - DETAILED STATUS & ERROR CODES

Bits 12 - 23 = 0

Bits 0 - 11 defined as:

X001	Parity Error
X002	Address Error
X003	Device Status Error
X004	Controller Function (Reject or Timeout)
X005	Device Reserved
X006	Device Not Ready
X007	Track Limit (Device Full)
0000	Other Error

NOTE: X = 1 normally
X = 0 when incorrect data read has been transferred to circular buffer

10	General Status
11	Write Error on Previous Sector
12	Function Timeout
13	Error Code Already Set
14	Status Error
15	Media Error
16	Device Not Ready

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9. DISK LABELING, UTILITY, AND TEST FUNCTIONS

This section does not pertain to the 7001. See section 5.4 for information regarding 7001 diagnostics and utilities.

UNISYS ONLY NOT CDC

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10. SUBASSEMBLY REMOVAL/REPLACEMENT PROCEDURE

This section describes the procedures required to remove and replace defective devices within the 7001 Mass Storage System.

10.1 Pluggable Logic Board/Card Removal

Removal and replacement procedures are described below.

10.1.1 Removal Procedure

1. Remove power from the power supply that powers the board/card to be removed.
2. All pluggable logic boards/cards in the controller are equipped with two camming lock-down levers. Rotating these levers simultaneously (out and up for the top, and out and down for the bottom), will disengage the logic board/card from its backplane connector.
3. Grasp board/card gently but firmly and pull out.

10.1.2 Replacement Procedure

1. Place board/card in top and bottom alignment guides.
2. Seat board/card to backplane connectors by gently but firmly engaging the camming lock-down levers on the top and the bottom of the cage until levers rest against the edge of the board/card. DO NOT FORCE.
3. If board/card will not seat, remove and inspect for bent pins on backplane or other obstructions.

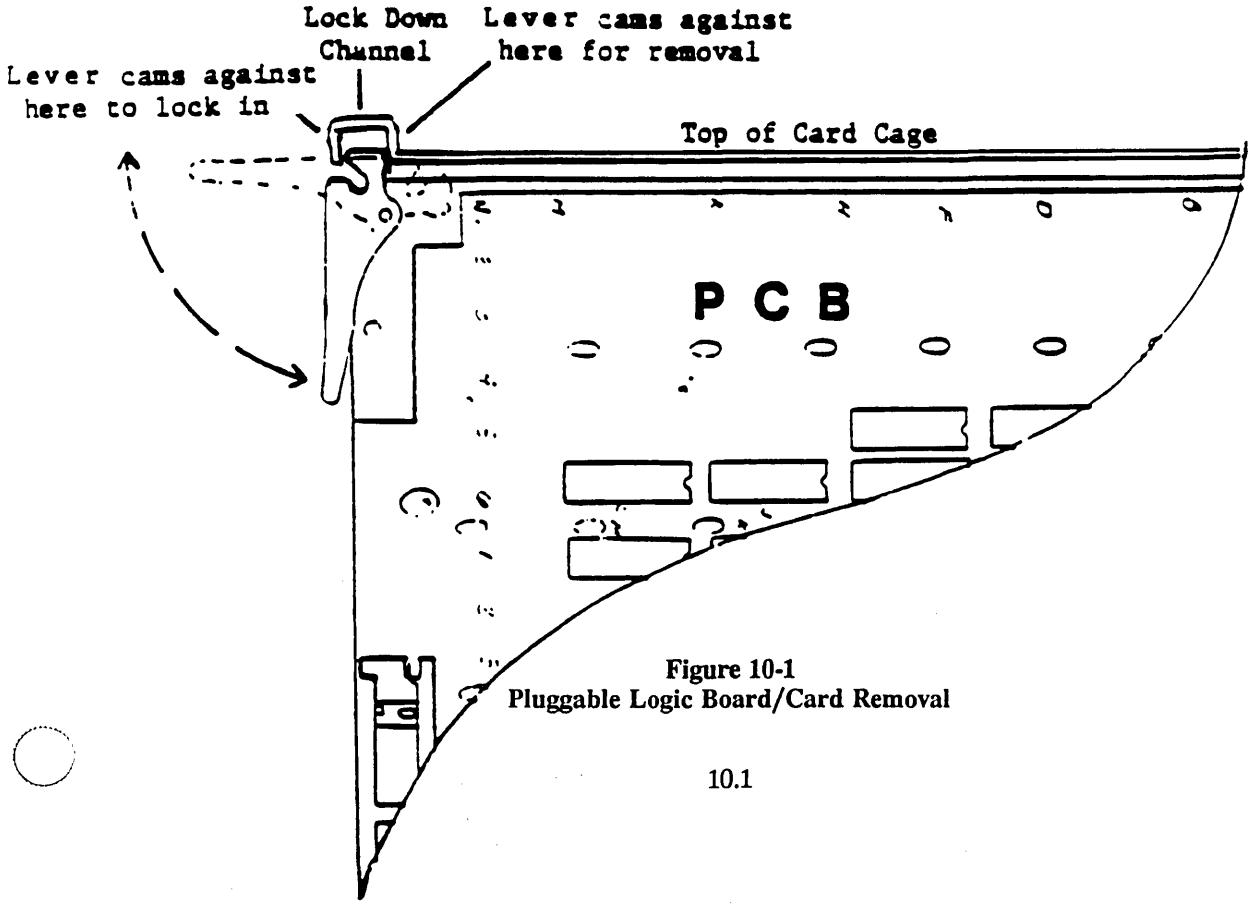


Figure 10-1
Pluggable Logic Board/Card Removal

10.2 OCP Board Removal and Replacement

1. Power on dual controller.
2. Label and remove signal cables from top and bottom rows of connectors.
3. Label and remove the four slip-on wires (+5V and ground).
4. Cut any cable ties, if present and interfering.
5. Remove four bottom screws holding board to frame. (All screws should be removed from the component side of the board.)
6. Support board with one hand and remove four top mounting screws.
7. Reinstall in reverse order.

CAUTION: When opening OCP gate B, be careful not to pull cables from the LED board (located on gate A) connectors (J1, J2, J3, and J4).

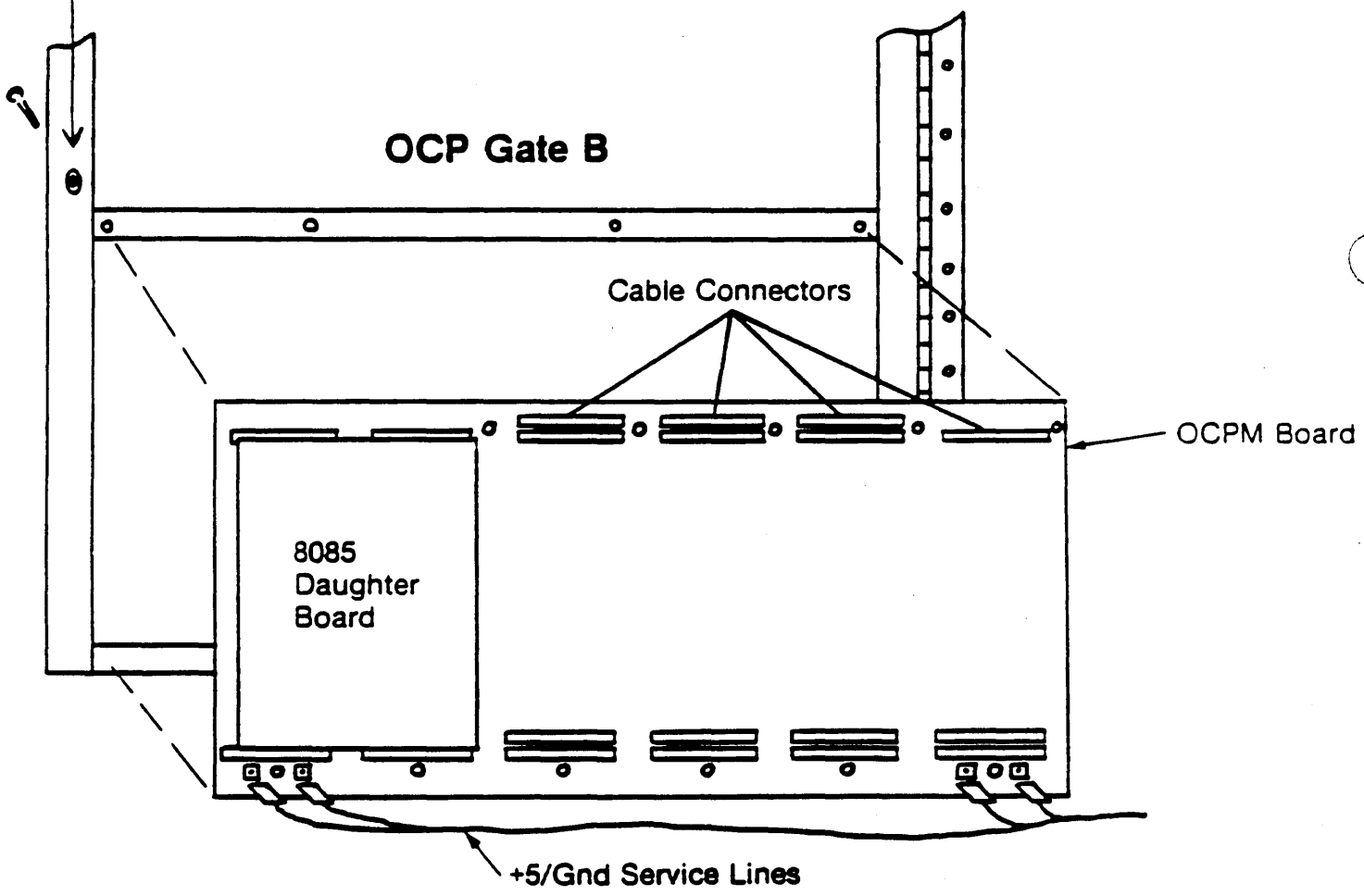


Figure 10-2
OCP Board Removal

10.3 CDCI Board Removal and Replacement

1. Power off the appropriate controller.
2. Remove two signal cables from the top of the CDCI board.
3. Remove two signal cables from the bottom of the CDCI board.
4. Remove VCC and GND wires from the bottom of the CDCI board.
5. Remove the two bottom screws holding the CDCI board to the frame.
6. Support the board with one hand while removing the two top screws holding the CDCI board to the frame.
7. Reinstall in reverse order.

NOTE: *Be sure to reinstall all four mounting screws to prevent VCC from shorting to the frame.*

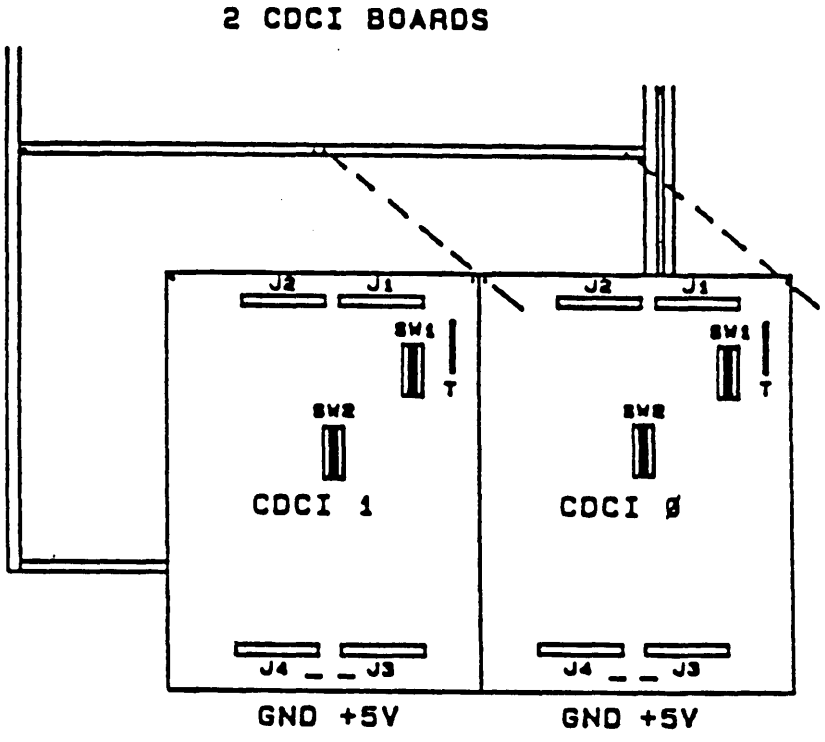


Figure 10-3
CDCI Board Removal

10.4 Driver Receiver Board Removal and Replacement [not applicable to the 7001]

Figure 10-4
Driver/Receiver Board [not applicable to the 7001]

10.5 Controller Cardcage Removal and Replacement

1. Power off dual controller.
2. Label and remove all boards from the controller cardcage.
3. Label and remove all signal cables from backplane board.
4. Label and remove the three heavy black 5V cables (and any other wires) from the 5V lugs on the backplane.
5. Label and remove the ground cables from the left end of the ground bus (mounted on the rear of the backplane).
6. Locate twisted pair (one white, one black) wires on left side of AC fan supply (outside of the cage). Label and disconnect the slip-on connectors.
7. Remove eight mounting screws at front of cage.
8. Reinstall in reverse order.

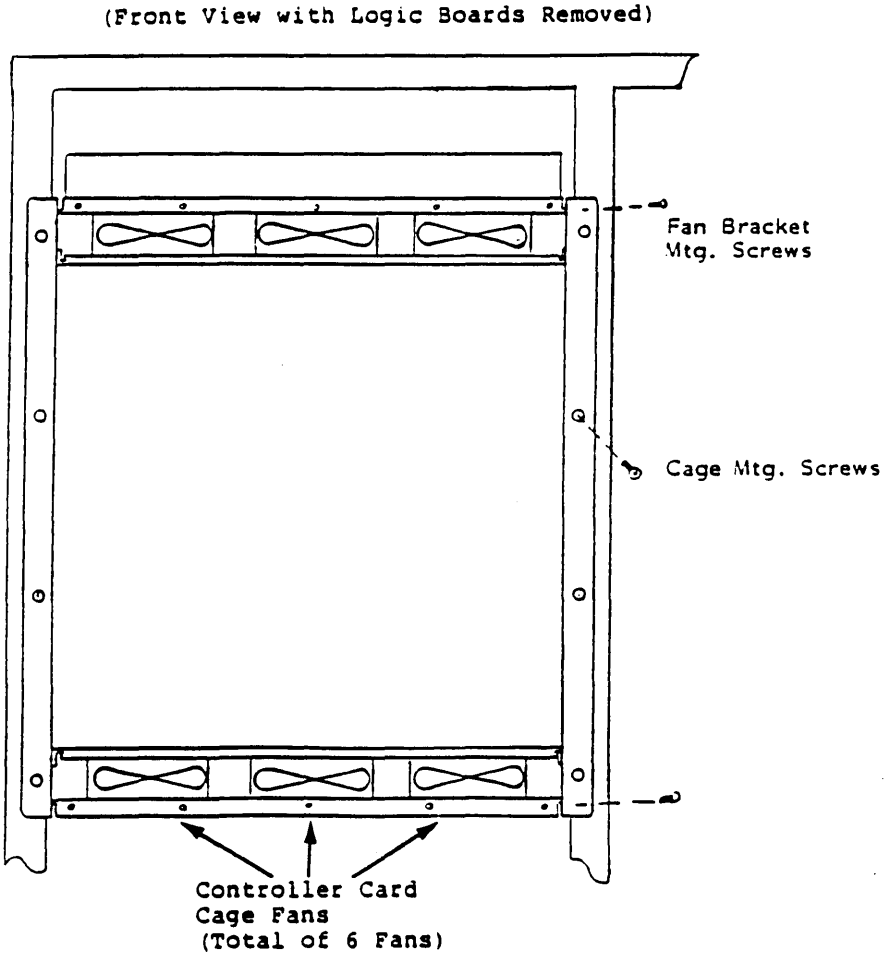


Figure 10-5
Controller Cardcage Removal

10.6 Controller Cardcage Backplane Removal and Replacement

1. Remove controller cardcage as described in section 10.5. See figure 10-5.
2. Place cardcage on flat surface with backplane up.
3. Remove ten screws holding backplane to frame.
4. Reinstall in reverse order.

10.7 Controller Cardcage Fan Removal

1. Remove controller cardcage as described in section 10.5. See figure 10-5.
2. Place cardcage on flat surface with backplane board up. (Be careful not to bend connector pins on backplane.)
3. Remove three screws from each side of controller cardcage for the three-fan assembly to be removed (upper or lower).
4. Tilt fan assembly out, taking care not to damage the two AC input wires to the assembly.
5. Remove the slip-on connectors of the fan being replaced.
6. Remove the four mounting screws holding the fan to the assembly.
7. Reinstall in reverse order.

10.8 Top Cover Removal and Replacement

1. Power off dual controller before proceeding.
2. Label and remove black fan wires from fan terminal block (A). (Do not remove black and white twisted pair wires.)
3. Remove eight top cover nuts and screws (B).
4. Carefully slide top fan assembly in whatever direction is convenient for lowering.

CAUTION: **Because the unit weighs 40 lbs., we recommend that two people lower it.**

5. Reinstall in reverse order.

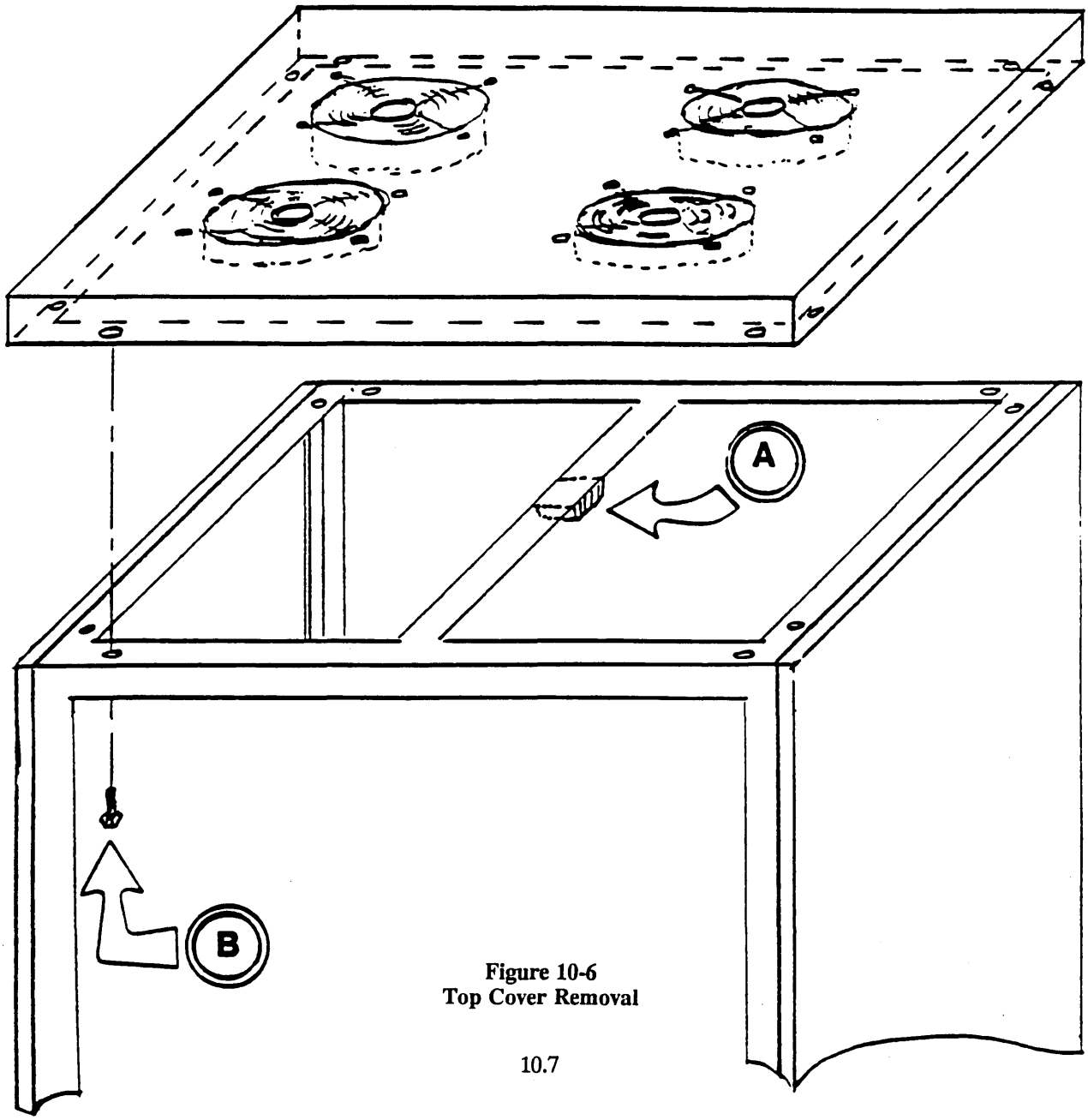


Figure 10-6
Top Cover Removal

10.9 Top Cover Fan Removal and Replacement

1. Remove top cover as described in section 10-8. See figure 10-6.
2. Remove the slip-on connectors of the fan being replaced.
3. Remove four screws holding fan to top cover assembly.
4. Reinstall in reverse order.

10.10 Disk Drive I/O Cardcage Removal

1. Power off the 7001. Be sure that all drives have been write protected.
2. Label and remove all cards from I/O cardcage.
3. Label and remove all signal cables from I/O cardcage backplane.
4. Cut cable ties on voltage and ground cables along top rear and left side of cage.
5. Label (if necessary) and remove voltage and ground wire from lugs on backplane.
6. While supporting cage with one hand, remove four mounting screws and remove assembly.

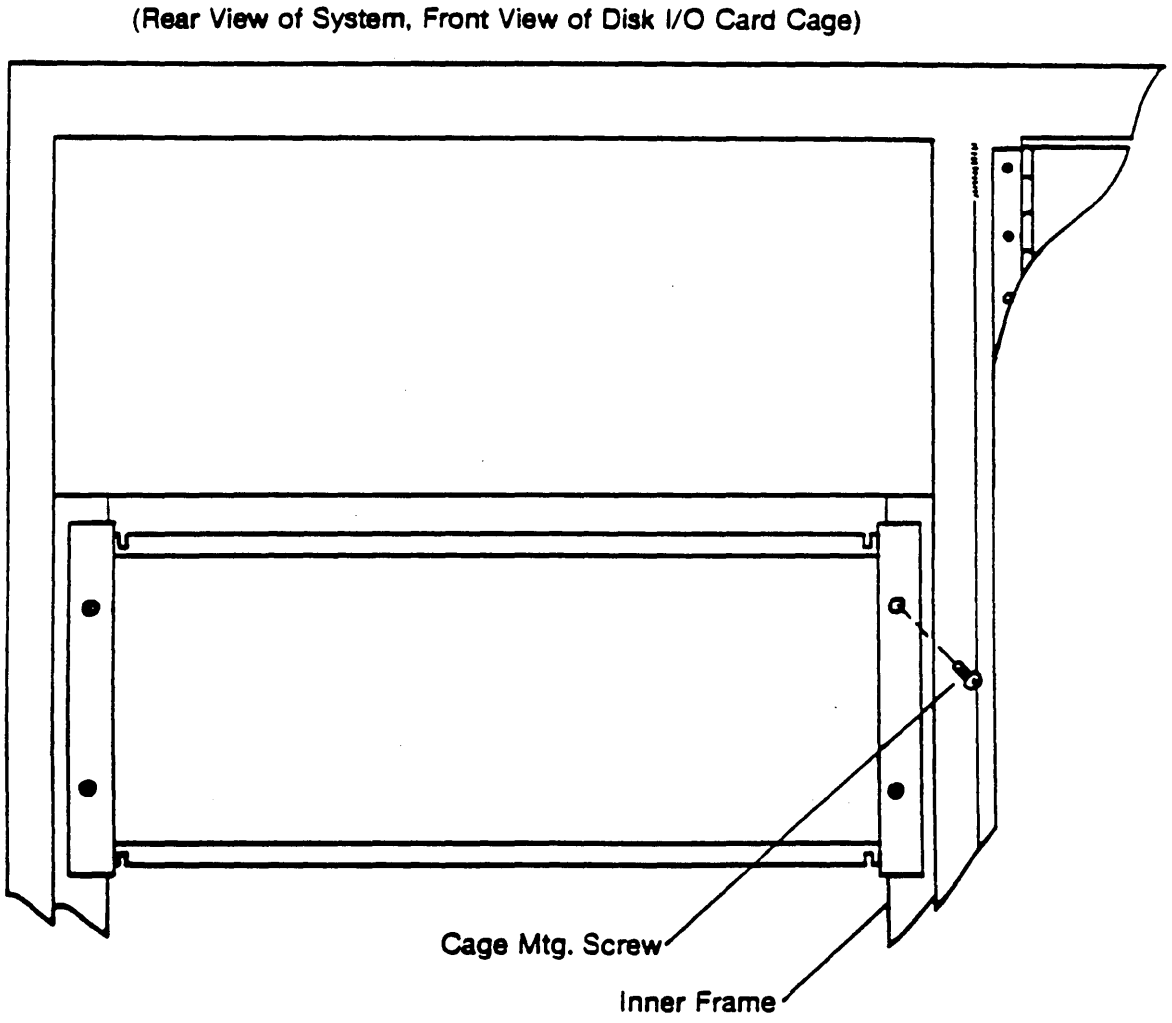


Figure 10-7
Disk Drive I/O Cardcage Removal

10.11 Disk Drive I/O Cardcage Backplane Removal and Replacement

1. Remove disk drive I/O cardcage as described in section 10.10. See figure 10-7.
2. Place cardcage on flat surface with backplane up.
3. Remove ten screws holding backplane to cage frame.
4. Reinstall in reverse order.

10.12 Expansion Cardcage Removal and Replacement

1. Power off the 7001. Be sure that all drives have been write protected.
2. Label and remove the three cards from the expansion cardcage. See figure 10-8.
3. Label and remove all signal cables from expansion cardcage backplane.
4. Cut cable ties on voltage and ground cables along top rear and left side of cage.
5. Label (if necessary) and remove voltage and ground wire from lugs on backplane.
6. While supporting cage with one hand, remove four mounting screws and remove assembly.

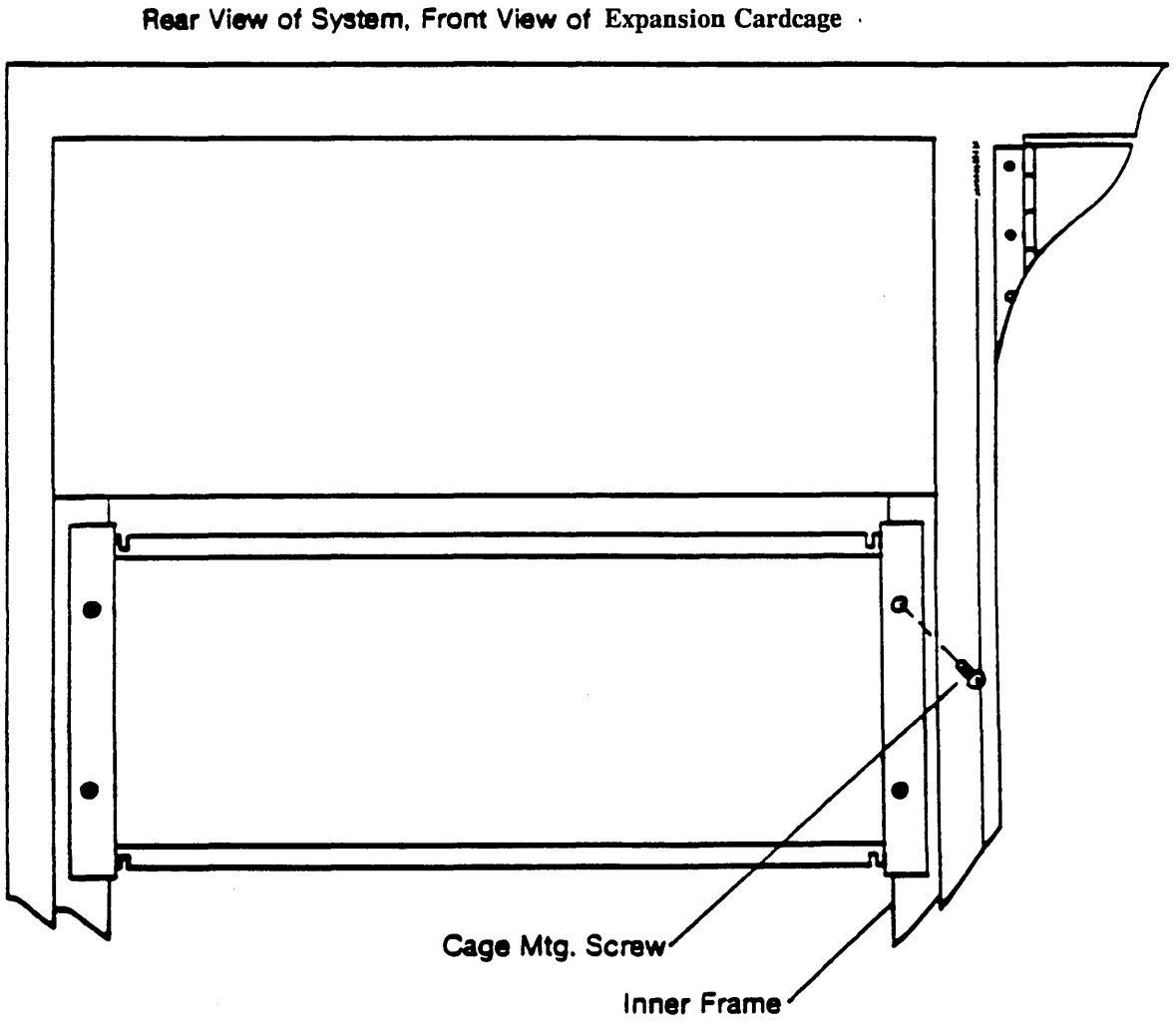


Figure 10-8
Expansion Cardcage Removal

10.13 Expansion Cardcage Backplane Removal and Replacement

1. Remove expansion cardcage as described in section 10.12. See figure 10-8.
2. Place cardcage on flat surface with backplane up.
3. Remove ten screws holding backplane to cage frame.
4. Reinstall in reverse order.

10.14 Disk Drives

The following sections describe removal and replacement procedures for the 9720 disk drives in the 7001.

10.14.1 Disk Drive Removal

1. At the system console, down the applicable disk drive via the control unit A path and the control unit B path.

2. At the 7001 OCP, place the applicable disk drive in bypass mode.

3. At the disk control panel, perform the following operations for the applicable disk drive:

   - o Deactivate the CHA and CHB switches to place the disk drive offline.
   - o Activate the WRITE PROTECT switch for the disk drive.
   - o Deactivate the PWR switch to power down the disk drive.

4. Open the rear door of the cabinet; all remaining steps can be performed at the rear of the cabinet.

5. Turn off the applicable disk drive via the on/off switch located on the power supply for that disk drive.

6. Remove the locking hold-down brackets mounted across the disk drives. This bracket is held in place with four screws, two on the left side and two on the right side front of the drive tray.

7. Carefully slide the drive tray out of the cabinet. Pull out the tray out far enough to access the cable connections.

8. Disconnect all interface cables from the rear of the applicable drive. See figure 10-9.

9. Remove the shroud covering the space between the power supply and the disk drive by removing the four screws at the top front of the disk drives and then lifting the shroud up. Then remove the drive top cover which is held in place with six screws, three on each side of the drive.

10. Disconnect the DC power harness. See figure 10-9.

11. Remove the four screws that attach the drive bracket to the drive tray. Two of these are located at the front between the drives (one upper and one lower), the third is located in the back of the tray, and the fourth is located beneath the drive. See figure 10-9.

NOTE: *From this point on you must support the drive because when you remove the next two screws the drive can fall through the tray if it is not being properly supported.*

12. Remove the two screws on the side of the tray; these go through the drive tray and into the drive itself. See figure 10-9.

13. Slide the drive forward and lift it out of the drawer.

14. Remove the drive from the bracket by removing the two mounting screws which attach it to the bracket. See figure 10-9.

10.14.2 Disk Drive Replacement

Replace a drive using the same procedures described in "Removing a Disk Drive," but perform them in reverse order. Keep in mind that if a replacement drive (or HDA) is to be installed, the following additional steps are required:

1. Uncrate the replacement drive or HDA. Check the shock watch on the unit to ensure that it has not been damaged in shipment. If damage has occurred, the unit must be returned unused. Ensure that a manufacturer's media flaw map is present and that the indicated serial number matches the replacement unit.

2. Set switches to match the settings on the drive being removed. See figures 10-10 and 10-11.

3. Install the replacement drive and turn on the AC power. (If the drive you are installing is the last one on the string, leave the terminators in place; if not, remove the terminators.) Wait for the drive to spin up and for all "normal" lights to appear. Be sure that a READY indication is provided on the drive control panel and the drive itself.

4. At the system console (host), down either control unit A or control unit B. The downed control unit will be used to run inline diagnostics (ILDs) to the replacement drive.

5. Load the OCP data switches with the worst case data pattern for the drive (6AF6DB06F).

6. For first-time formatting of a 9720 drive, follow the steps below:

   a. Load Toggle 7.
   b. Perform ILD 1.
   c. When **DRIVE X OK?** is displayed at the OCP, turn off the clock on the MPC board (top switch down) and answer **YES**.
   d. When **DO YOU WANT TO FORMAT DRIVE X?** is displayed at the OCP, turn on the clock on the MPC board (top switch up) and answer **YES**.

7. Allow the ILD 1 format operation to complete normally.

8. Create a new alternate track log for the drive by following these procedures:

   a. Record the drive number and the drive serial number on a blank alternate track log sheet.
   b. Refer to the media flaw map for the drive. In sequential order, write down the cylinder and head number for all error bursts.

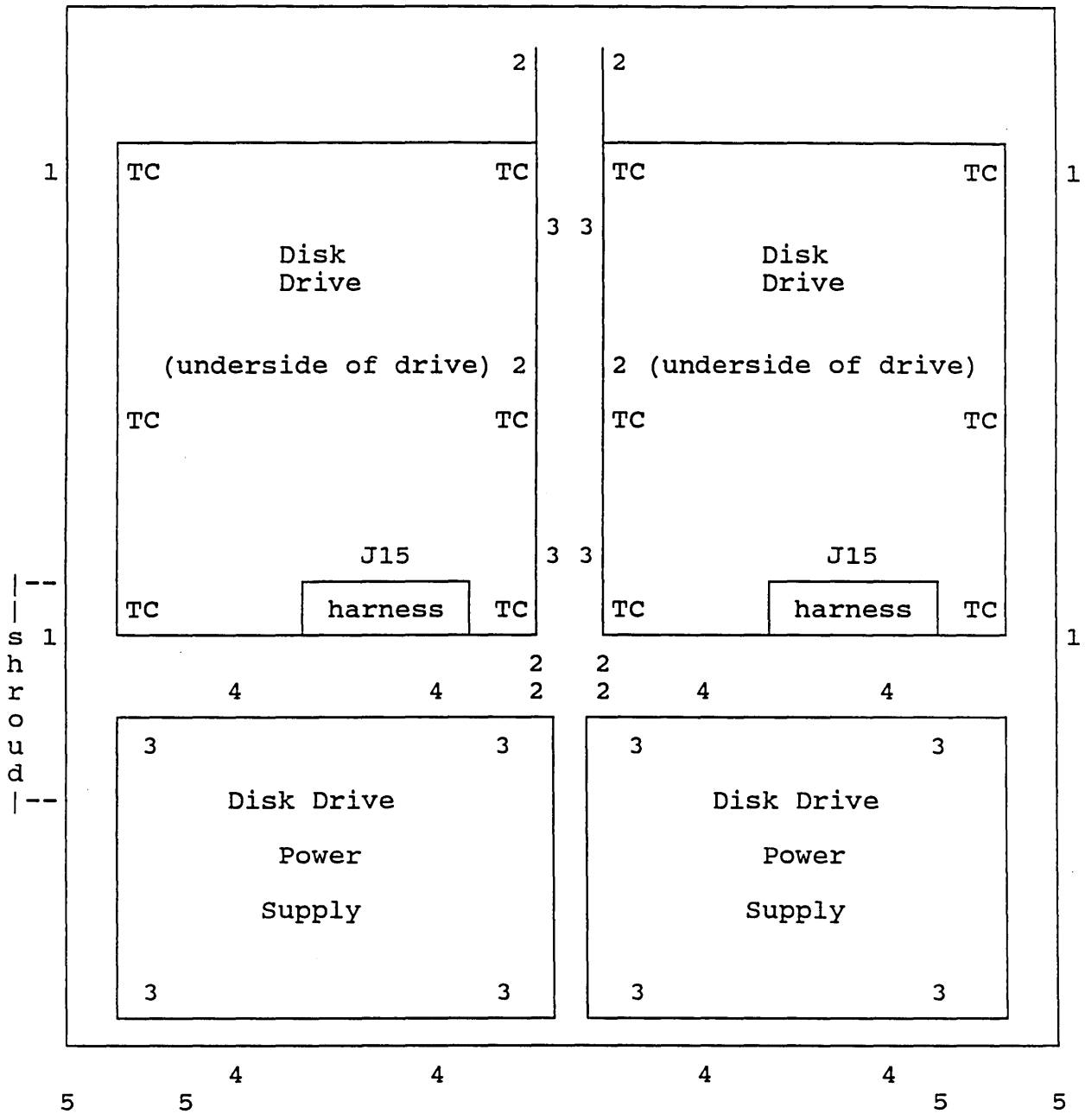
9. Use ILD 4 to flag (as defective) all alternate tracks on the drive which are indicated on the flaw map. The alternate tracks are in the range of cylinders numbered 1624 through 1633.

10. Optionally, run ILD 3 to verify the formatting of the defective tracks.

11. Run ILD 2 (Verify).

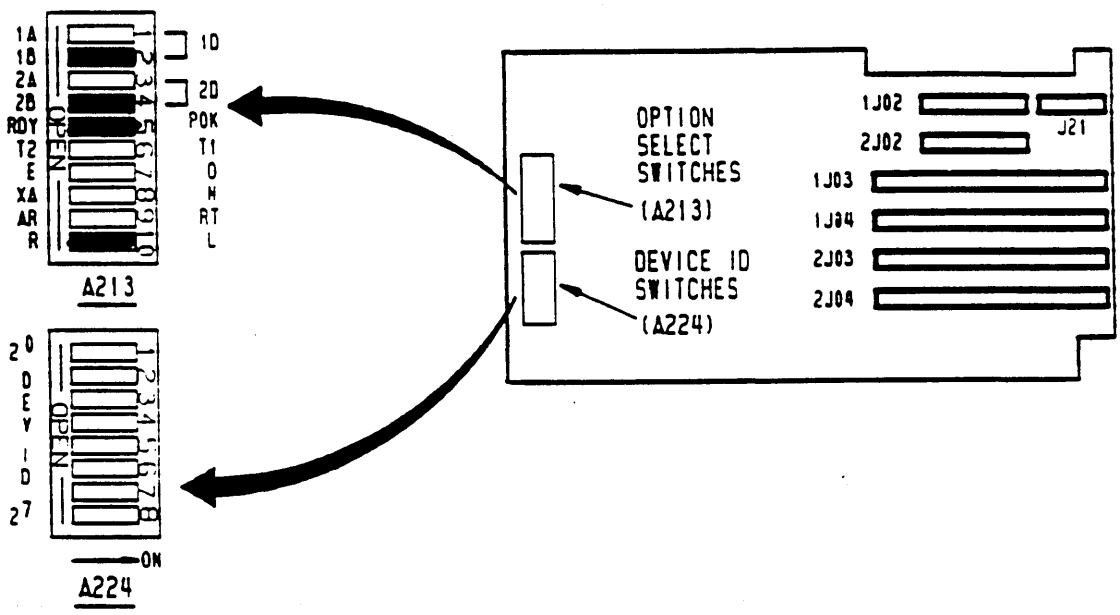
12. After formatting (ILD 1) and assigning alternates (ILD 4), run ILD B, option 50X where X equals the drive number (see section 5.4, Offline Diagnostics). Monitor the thumbwheel switch 4D8 to watch that the diagnostic sequentially writes and reads every cylinder on the drive. When the random mode has started, terminate the ILD (if desired).

13. See section 5.4 to Write Manufacturing Data (4EX). When this step is completed the system is ready for use.



NOTES: *The shroud covers the space between the bottom of the drives and the top of the power supplies.*
1 - These screws attach the drive directly to the tray.
2 - These screws attach the bracket to the tray.
3 - These screws attach the power supply (or the drive) to the power supply (or drive) bracket.
4 - These screws attach the power supply bracket to the tray.
5 - These screws attach the locking hold-down brackets mounted across the front of the drive tray.

Figure 10-9
Disk Drive Tray containing Two Disk Drives and Two Power Supplies



NOTES:
Shaded switches are ON (closed).
If the system configuration does not include a disk drive control panel, switch A213-10 to ON (local). If the configuration does include a disk drive control panel, switch A213-10 to OFF (remote).

Figure 10-10
Disk Drive I/O Board Switches

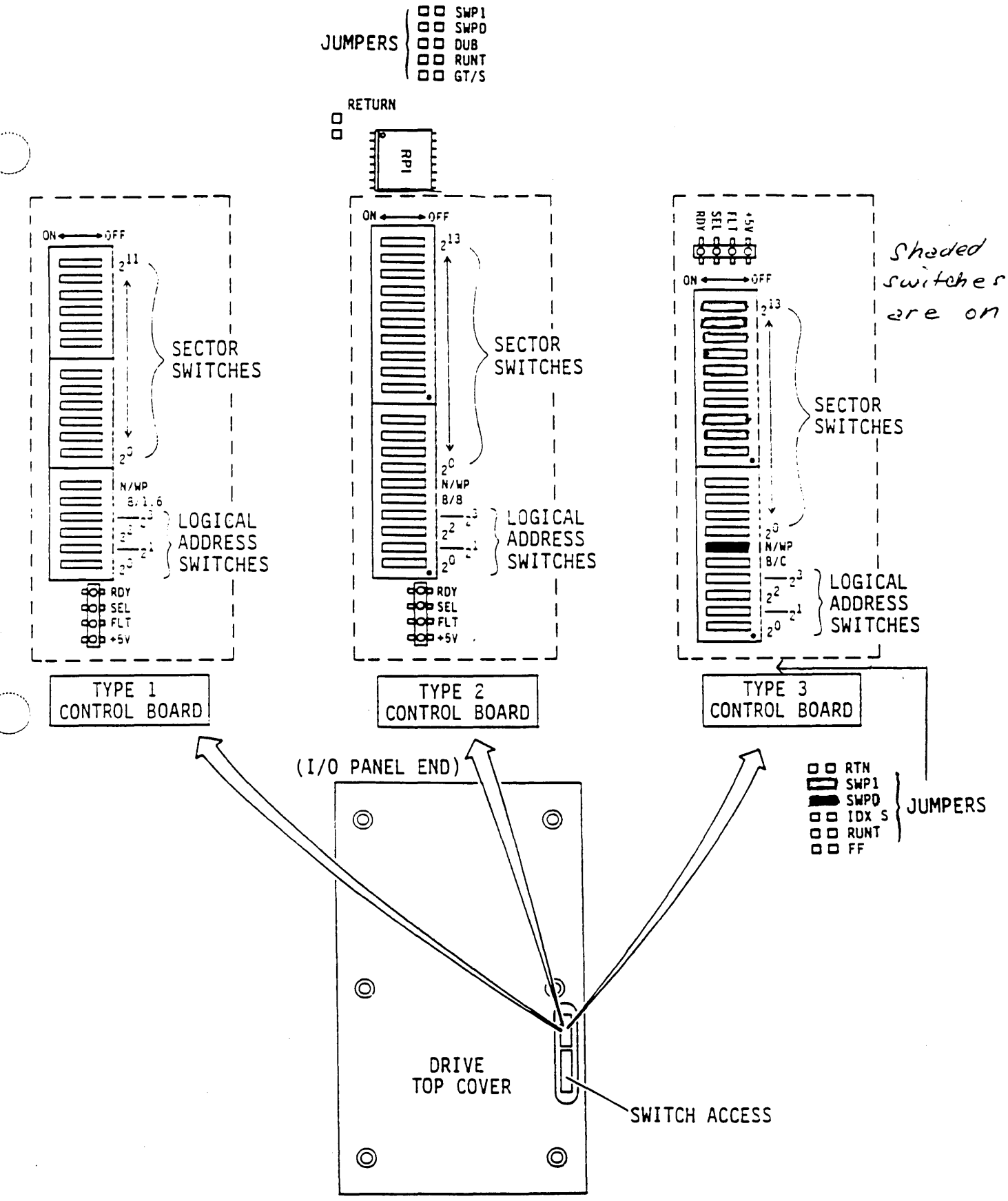


Figure 10-11
Disk Drive Control Board

Table 10-1
Switch Settings for Logical Drive Address

Drive	2^3	2^2	2^1	2^0
0	ON	ON	ON	ON
1	ON	ON	ON	OFF
2	ON	ON	OF	ON
3	ON	ON	OFF	OFF
4	ON	OFF	ON	ON
5	ON	OF	ON	OFF

10.15 Disk Drive Power Supply Removal and Replacement

1. At the system console, down the applicable disk drive.
2. At the OCP, place the applicable disk drive in bypass mode.
3. At the drive control panel, perform the following operations for the applicable disk drive:
   - o Deactivate the CHA and CHB switches to place the disk drive offline.
   - o Activate the disk drive write protect switch.
   - o Deactivate the PWR switch.
4. Open the rear door of the 7001 cabinet. All remaining steps can be performed at the rear of the cabinet.
5. Turn off the applicable disk drive power switch located at the front of the power supply.
6. Carefully slide the disk drive tray out of the cabinet. Pull the tray out far enough to access the cable connections.
7. Using a magnetic-tip Phillips screwdriver, remove the four screw/washer assemblies (two in front and two in back) which secure the power supply to the drawer, and lift the power supply out.
8. Disconnect the DC power harness from the power supply by pulling it gently but firmly. You may want to use pliers at either side to help.
9. Remove the AC plug from the back of the power supply.
10. Interface brackets must be removed from the power supply if the supply is to be replaced. (There are four screws holding the power supply to the bracket.)
11. Install in reverse order.

10.16 Display/Maintenance Panel Removal and Replacement

1. Power off dual controller.
2. Label and unplug display panel assembly signal connector.
3. Label and remove display panel assembly 5V and ground slip-on connectors.
4. Unplug key pad assembly signal cable.
5. Label and unplug four signal cable connectors from LED assembly.
6. Cut cable ties as necessary to free the thumbwheel switch cable as it is a part of the Display/Maintenance panel.
7. Label and remove the LED assembly 5V and ground slip-on connectors.
8. Supporting the panel as necessary, remove the two mounting screws at each end of the mounting frame. (Screws are through side of frame.)
9. Reinstall in reverse order.

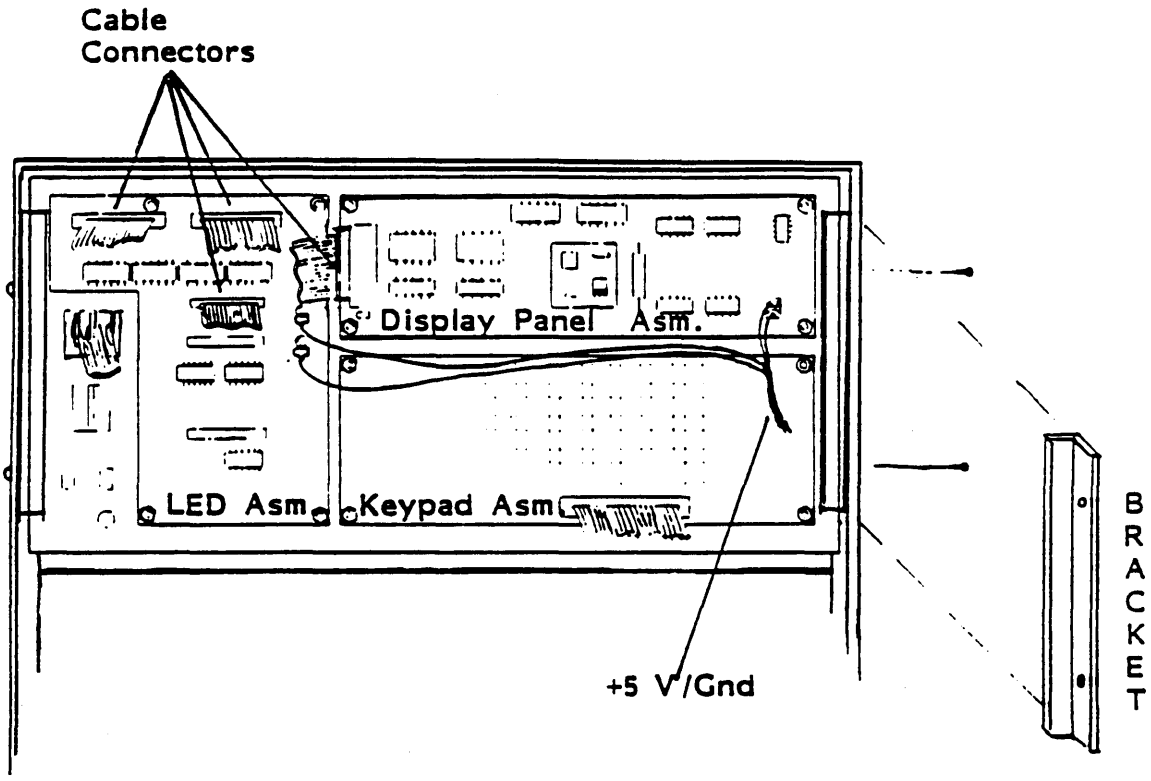


Figure 10-12
Display/Maintenance Panel Removal

10.17 Drive Control Panel Removal and Replacement

1. Power down dual controller.
2. Remove cable ties holding insulator shield on back of panel
3. Remove cable ties holding signal cables to switch modules. Be careful not to damage cables.
4. Label and unplug all switch module cable connectors.
5. Remove two mounting nuts from each side (rear) of the panel.
6. Reinstall in reverse order.

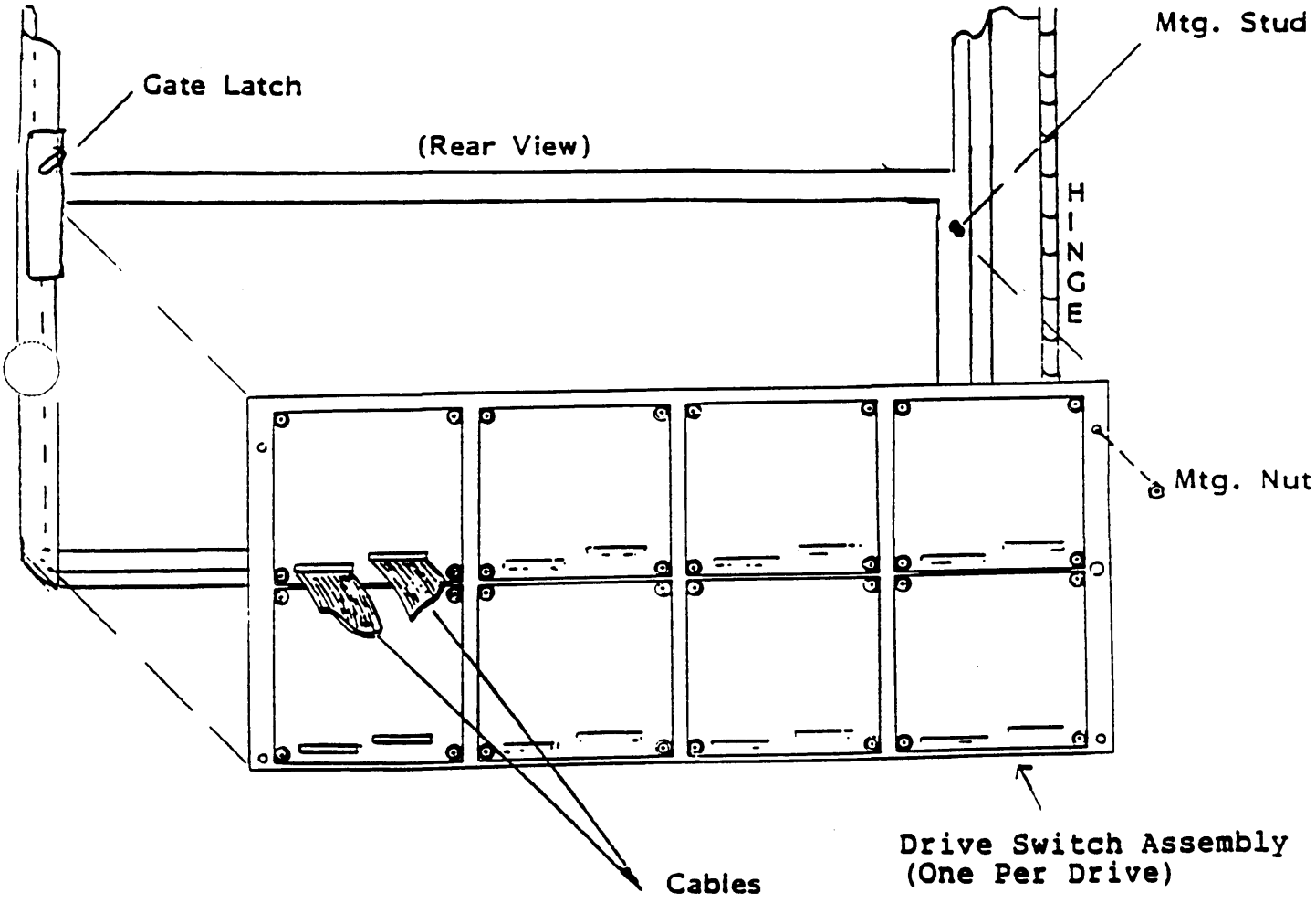
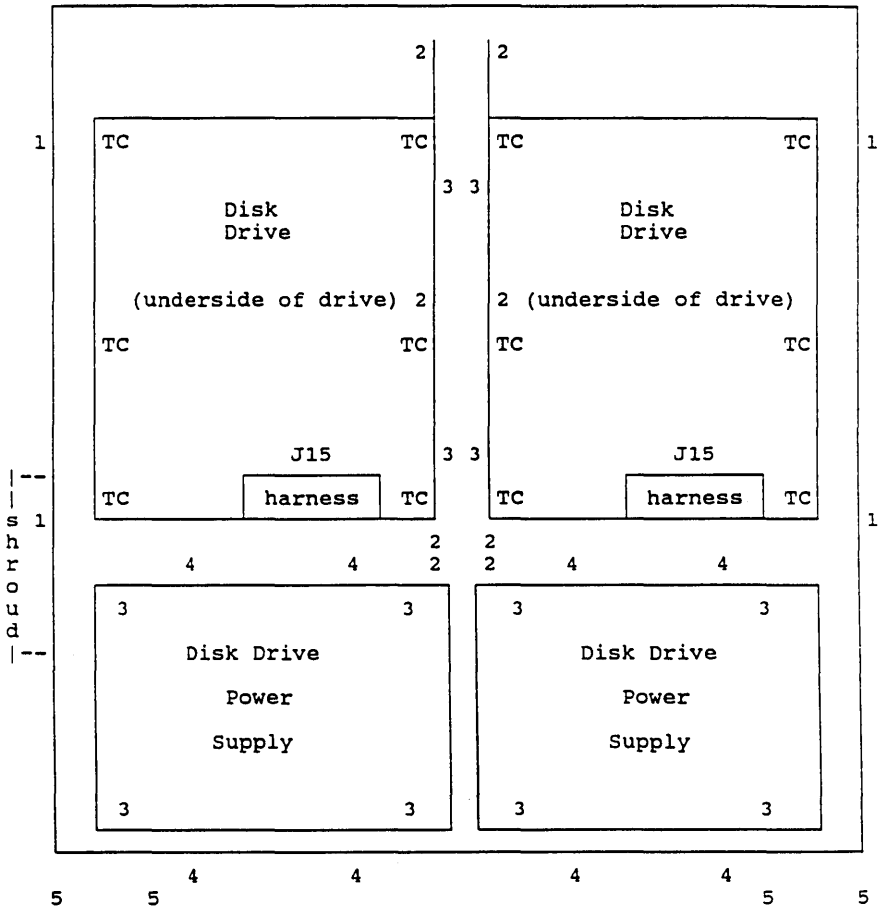


Figure 10-13
Drive Control Panel Removal and Replacement

10.18 DC Power Supply Removal and Replacement

1. Power down the 7001 system.
2. Remove the shroud covering the space between the power supply and the disk drive by removing the four screws at the top front of the disk drives and then lifting the shroud up.
3. Unplug input AC power connector to the controller.
4. Label and remove heavy cables from 5V and ground lugs on power supply.
5. Disconnect AC input wires on the power supply.
6. Remove the four mounting screws and then remove the power supply.
7. Reinstall in reverse order.



NOTES: *The shroud covers the space between the bottom of the drives and the top of the power supplies.*
1 - These screws attach the drive directly to the tray.
2 - These screws attach the bracket to the tray.
3 - These screws attach the power supply (or the drive) to the power supply (or drive) bracket.
4 - These screws attach the power supply bracket to the tray.
5 - These screws attach the locking hold-down brackets mounted across the front of the drive tray.

Figure 10-14
DC Power Supply Removal and Replacement

11. POWER SUPPLY ADJUSTMENT PROCEDURES

The following sections provide procedures for adjusting the power supplies in the 7001. There are six types of power supplies in the 7001: five of these are mounted on the back of the power supply panel; the sixth is the separate power supply for each disk drive.

Figure 11-1 shows the power supplies which are located on the power supply panel. Adjustment procedures for these power supplies are described in sections 11.1 through 11.5. Section 11.6 describes the adjustment procedures for the separate power supply for each disk drive.

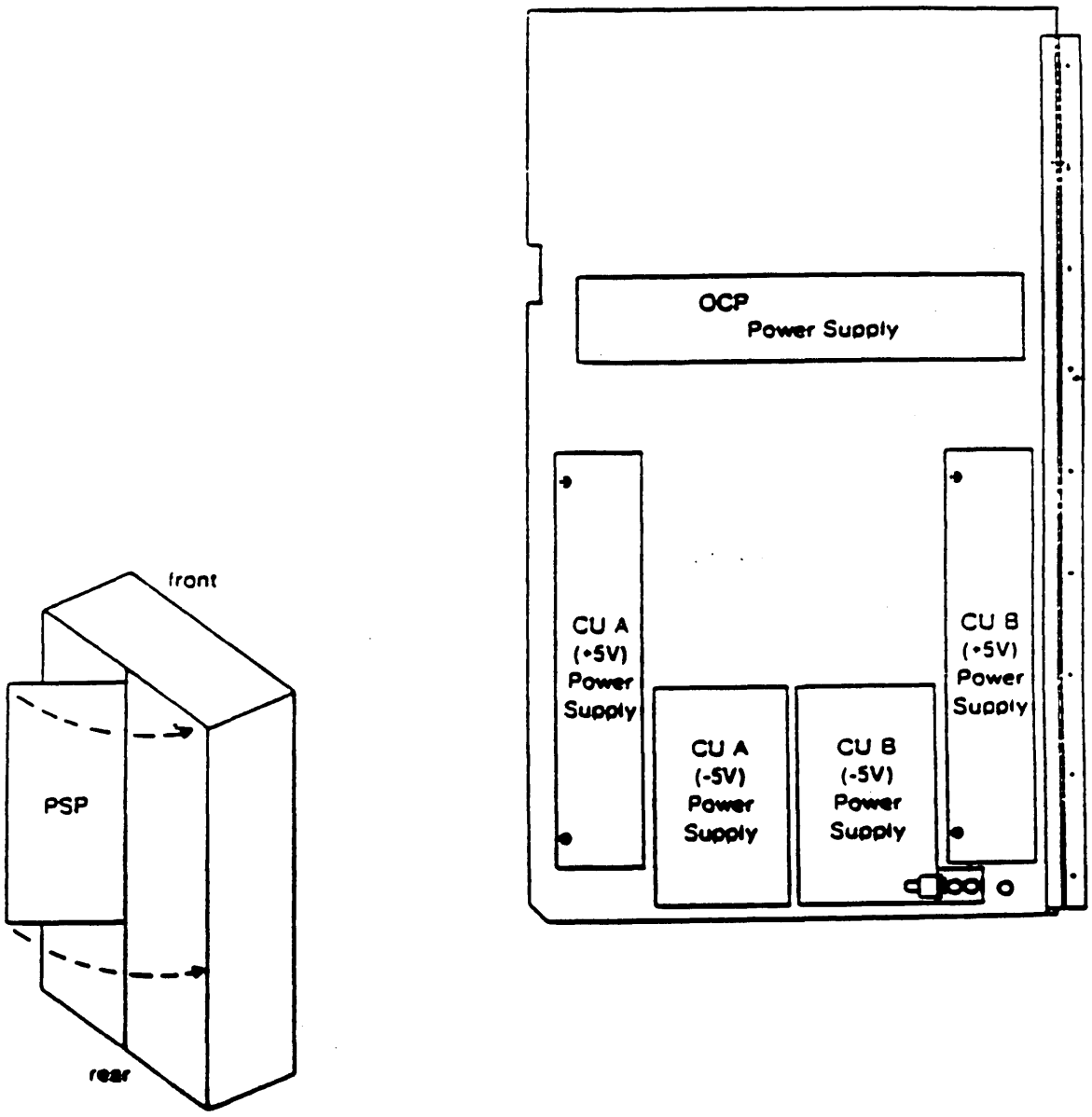


Figure 11-1
Power Supply Panel, 7001 System

11.1 Controller A (+5V) Power Supply Adjustment Procedure

1. Measure the voltage at the backplane of the controller cardcage by connecting the positive lead of a digital voltmeter to terminal TP6 (on the controller cardcage backplane) and the meter common lead to TP3 (also on the controller cardcage backplane). See figure 11-2 for the location of these terminals.

2. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot (R35) inside the power supply until the voltage measured in step 1 is +5.05V DC ± 1%. See figure 11-3 for the location of the adjust pot.

3. Differential check. Move the ground lead to the DC ground bus on the DC distribution panel. Use the positive lead to check for voltage differential at the following points:

   a. TP6 on the controller backplane (see figure 11-2)

   b. I/O cardcage +5V lug on right side (when viewing the cable side of the backplane) (see figure 11-8)

   c. +5V lug on "A" gate CDCI PCBs (see figure 11-9)

   None of these measurements should differ from +5.05V by more than 0.2V. If any of these measurements differ from +5.05V by more than 0.2V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.2 Controller A (-5V) Power Supply Adjustment Procedure

1. Connect the positive lead of a digital voltmeter to one of the controller A (-5V) lugs on the DC distribution block (see figure 11-4); connect the meter common lead to either of the ground bus bars on the DC distribution block.

2. Remove the power supply panel cover. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot (R29) inside the power supply until the voltage measured in step 1 is -5.10V DC ± 1%. See figure 11-5 for the location of the adjust pot on -5V power supplies.

3. Differential check. Leaving the ground lead in place, use the positive lead to check for voltage differential at the following points:

   a. -5V DC terminal on controller A DC terminal block (see figure 11-4)

   b. I/O cardcage -5V lug on right side (when viewing cable side of the backplane) (see figure 11-8)

   c. expansion cardcage -5V lug (see figure 11-7)

   None of these measurements should differ from -5.10V by more than 0.3V. If any of these measurements differ from -5.10V by more than 0.3V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.3 Controller B (+5V) Power Supply Adjustment Procedure

1. Measure the voltage at the backplane of the controller cardcage by connecting the positive lead of a digital voltmeter to terminal TP4 (on the controller cardcage backplane) and the meter common lead to TP1 (also on the controller cardcage backplane). See figure 11-2 for the location of these terminals.

2. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot (R35) inside the power supply until the voltage measured in step 1 is +5.05V DC $\pm$1%. See figure 11-3 for the location of the adjust pot on the +5V power supplies.

3. Differential check. Move the ground lead to the DC ground bus on the DC distribution panel. Use the positive lead to check for voltage differential at the following points:

   a. TP4 on the controller backplane (see figure 11-2)

   b. I/O cardcage +5V lug on left side (when viewing the cable side of the backplane) (see figure 11-8)

   c. +5V lug on "B" gate of CDCI PCBs (see figure 11-9)

   None of these measurements should differ from +5.05V by more than 0.2V. If any of these measurements differ from +5.05V by more than 0.2V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.4 Controller B (-5V) Power Supply Adjustment Procedure

1. Connect the positive lead of a digital voltmeter to one of the controller B (-5V) lugs on the DC distribution block (see figure 11-4); connect the meter common lead to any point on either of the ground bus bars on the DC distribution block.

2. Remove the power supply panel cover. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot inside the power supply until the voltage measured in step 1 is -5.10V DC $\pm$ 1%. See figure 11-5 for location of adjust pot on -5V power supplies.

3. Differential check. Leaving the ground lead in place, use the positive lead to check for voltage differential at the following points:

   a. -5V DC terminal on controller B DC distribution block (see figure 11-4)

   b. I/O cardcage -5V lug on left side (when viewing the cable side of the backplane) (see figure 11-8)

   c. expansion cardcage -5V lug (see figure 11-7)

   None of these measurements should differ from -5.10V by more than 0.3V. If any of these measurements differ from -5.10V by more than 0.3V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.5 OCP Power Supply Adjustment Procedure

CAUTION: **There is little space between the adjust hole of the OCP power supply and the +5V controller A power supply, which is located directly beneath the OCP power supply. Take care not to damage the controller A power supply while adjusting the OCP power supply.**

1. Measure the voltage at the backplane of the controller cardcage by connecting the positive lead of a digital voltmeter to terminal TP5 (on the controller cardcage backplane) and the meter common lead to TP2 (also on the controller cardcage backplane). See figure 11-2 for the location of these terminals.

2. Insert a screwdriver into the adjust hole of the power supply and turn the adjust pot (R35) inside the power supply until the voltage measured in step 1 is +5.05V DC $\pm$ 1%. See figure 11-6.

3. Differential check. Leaving the ground lead in place, use the positive lead to check for voltage differential at the following points:

   a. +5V lugs on OCP PCB

   b. TP5 of the controller backplane

   Neither of these measurements should differ from +5.05V by more than 0.2V. If any of these measurements differ from +5.05V by more than 0.2V, check for loose crimps or nuts, wrong wire size, bad junctions, etc.

11.6 Disk Drive Power Supply Adjustment Procedure

Under normal conditions there is no need to adjust the disk drive power supply because it is preadjusted and should arrive adjusted correctly. However, if you need to verify whether it is, use the procedure which follows.

J15 is the 13-pin connector located at the right front end of each disk drive. Using a digital voltmeter and pin 3 as the ground, verify that the following voltages are correct. (You need only check those which have entries under the "Acceptable limits" heading.)

Pin	Voltage	Acceptable limits
1	+5V high	4.75V to 5.25V
2	+5V sense	
3	ground (±5V, -12V)	
4	±5V sense return	
5	-5V high	-5.25V to -4.75V
6	-5V sense	
7	-12V high	-12.5V to -11.5V
8	+5V power OK	4V to 6V
9	key	
10	ground (+24V)	
11	ground (+24V)	
12	+24V high	23V to 25V
13	+24V high	23V to 25V

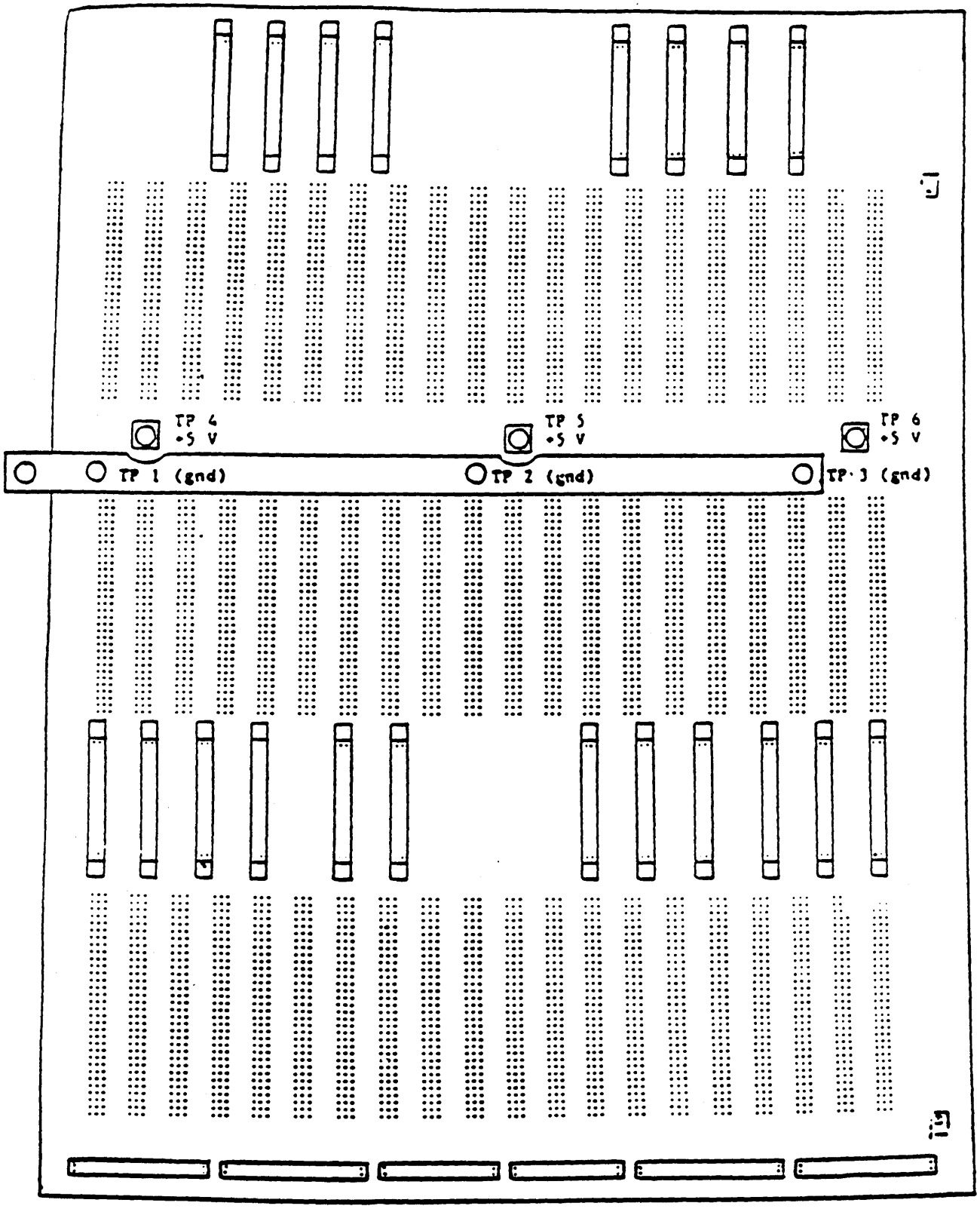


Figure 11-2
Controller Backplane

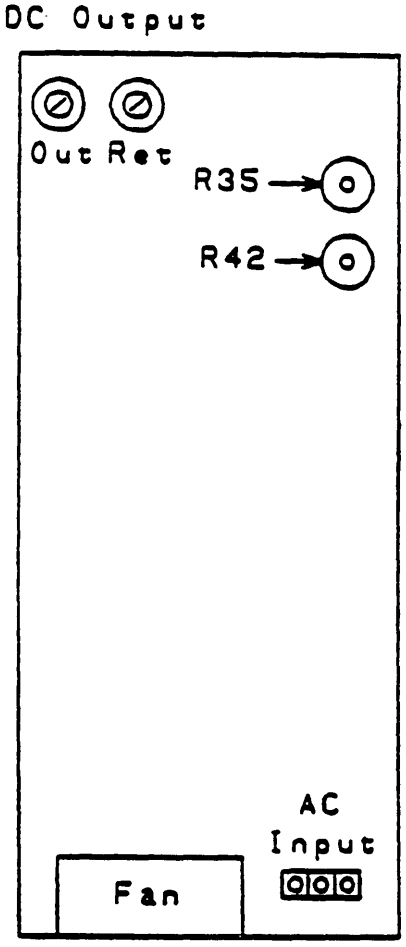


Figure 11-3
Location of Adjust Pot
on Controller A and B +5V Power Supplies

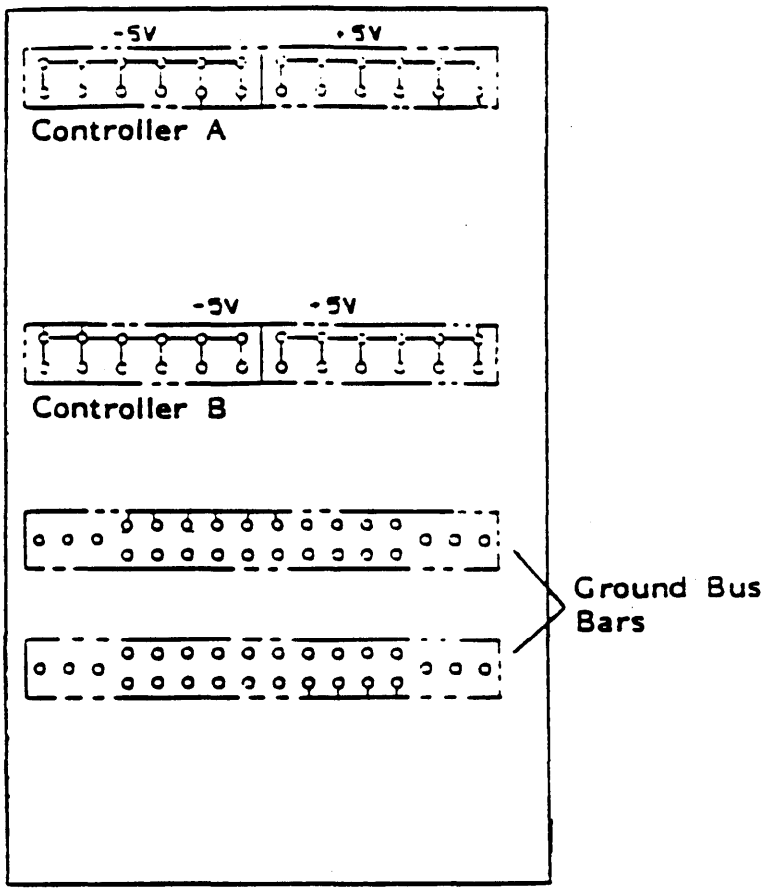


Figure 11-4
DC Distribution Block

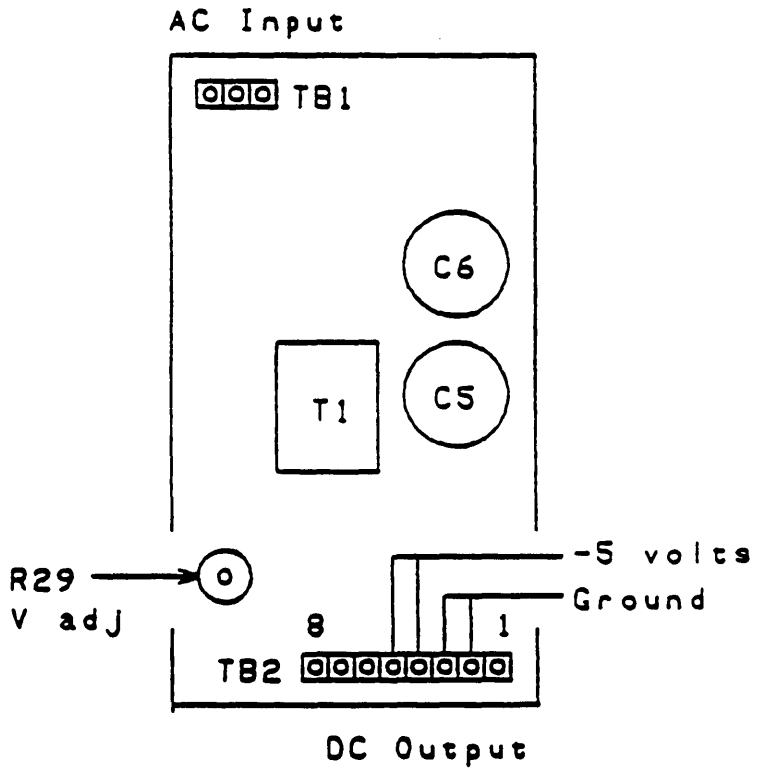


Figure 11-5
Location of Adjust Pot
on Controller A and B -5V Power Supplies

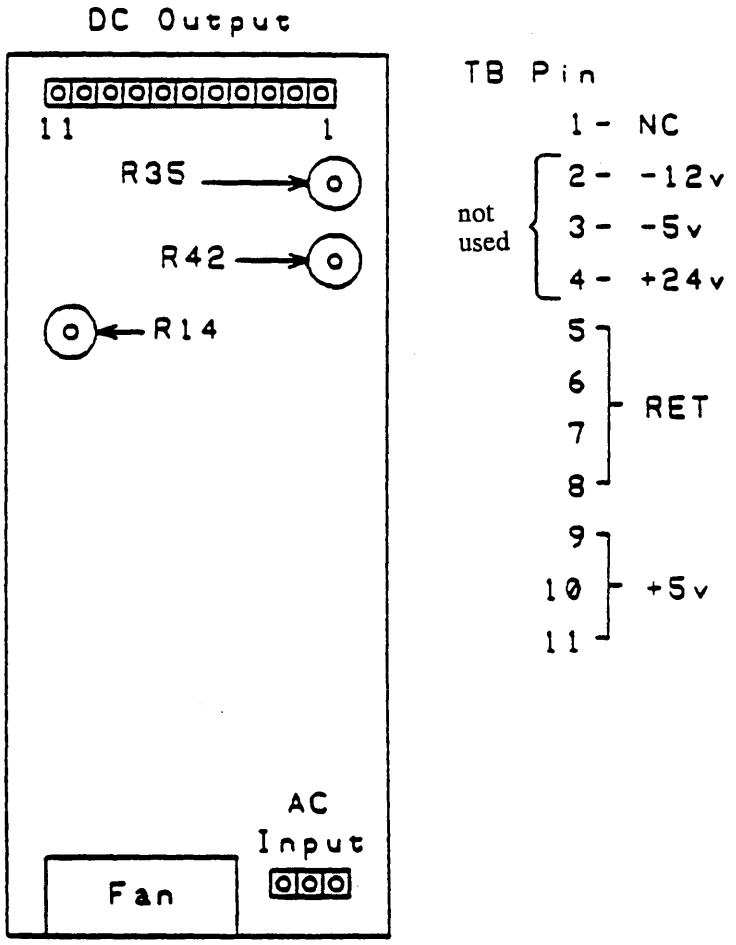


Figure 11-6
OCP Power Supply

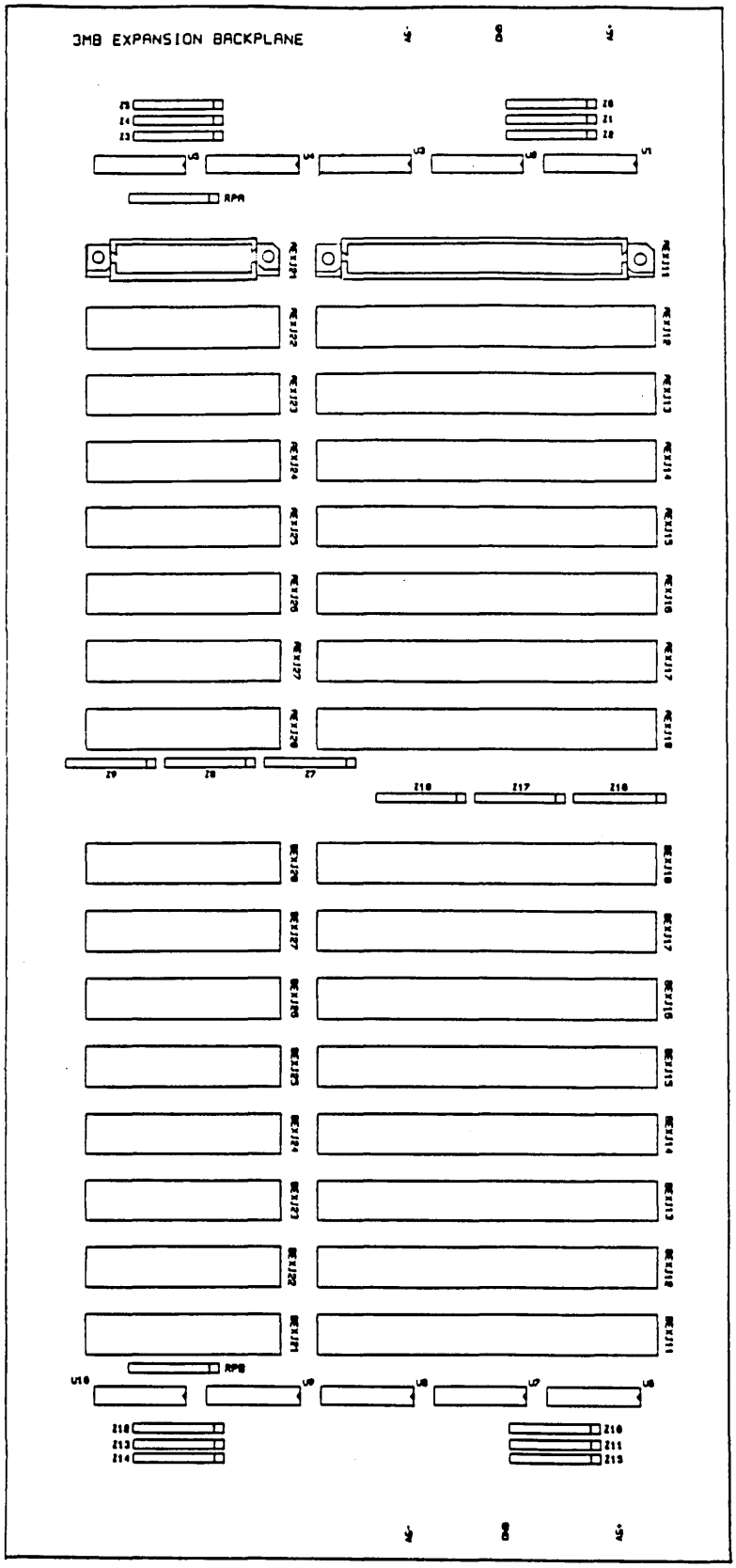


Figure 11-7
Expansion Cardcage Backplane

COMPONENT SIDE

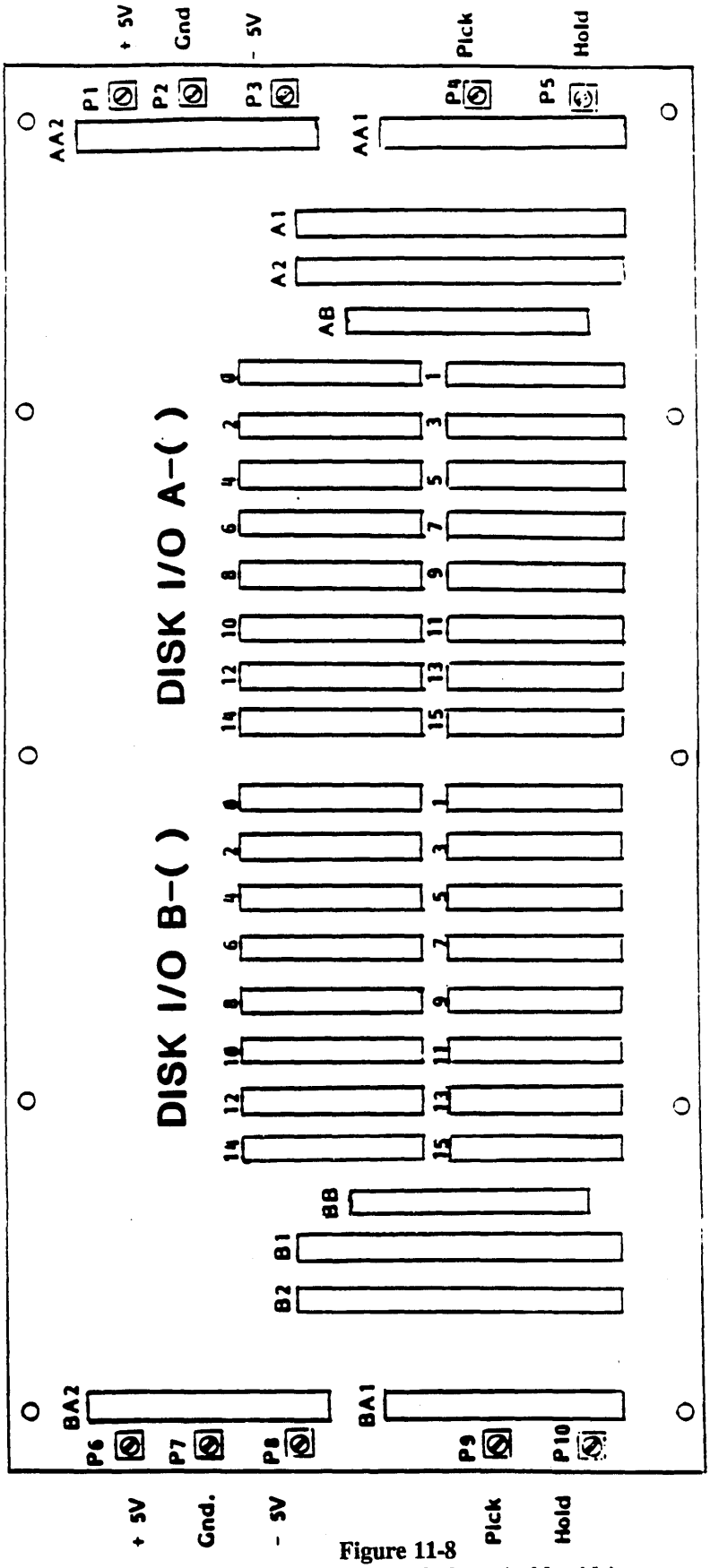


Figure 11-8
Disk I/O Cardcage Backplane (cable side)

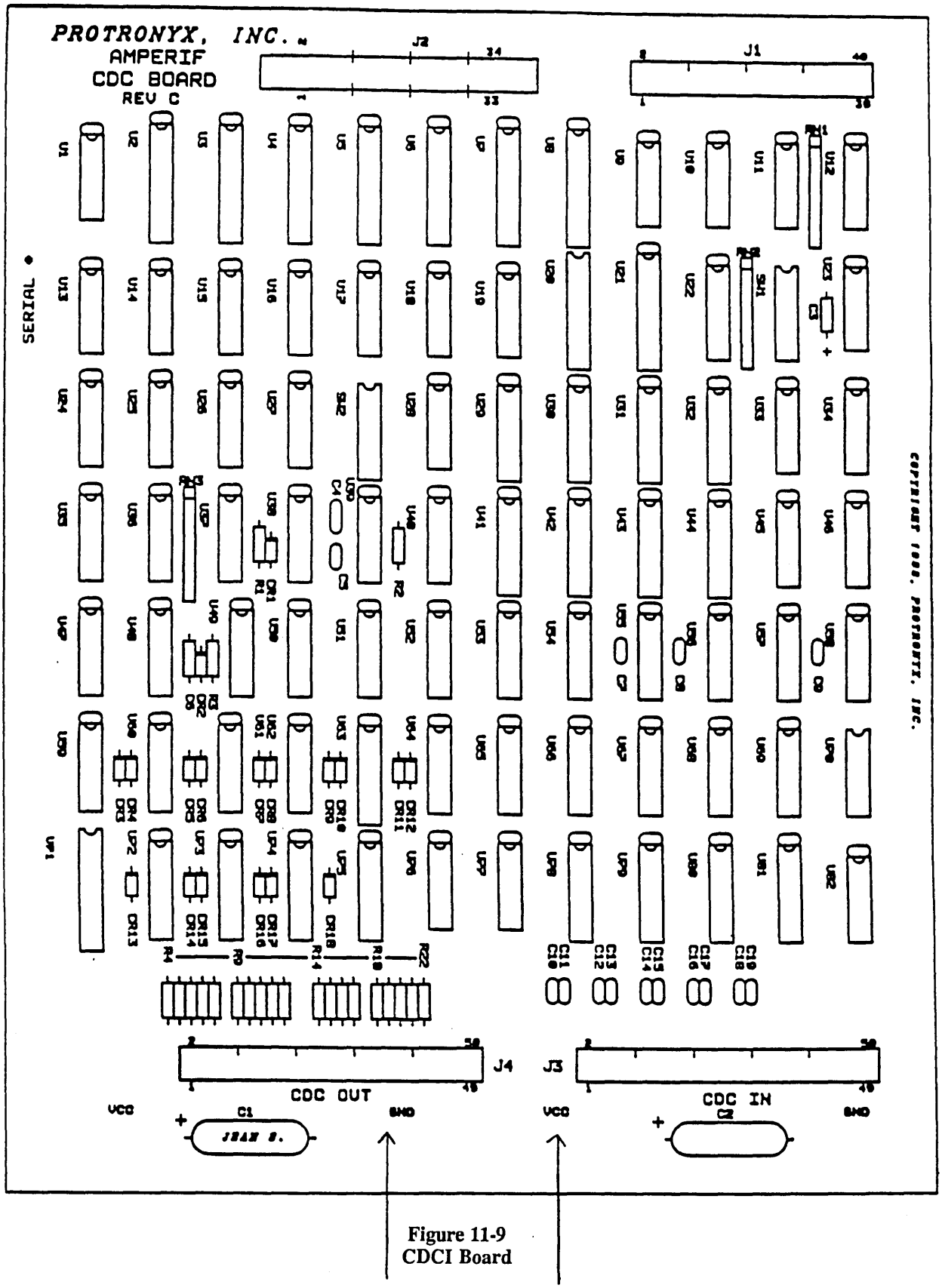


Figure 11-9
CDCI Board

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12. EQUIPMENT INSTALLATION PROCEDURES

Use the following procedures to prepare your site for an installation and to do the installation.

12.1 Preinstallation

This section provides information required to prepare a site for the installation of Amperif equipment. Equipment clearance, air conditioning, and power and grounding requirements are discussed.

12.1.1 Equipment Placement

Computer Room Installation. A false floor is required due to a large I/O cable bend radius. The area must be large enough to accommodate the equipment and to allow working room around it; about three feet in front and three feet in back of the system. Consideration must also be given to equipment cable-length restrictions and obstructions such as walls, pillars, aisles, and doors that restrict the position of equipment.

Air Conditioning. Amperif's equipment must be placed in an air-conditioned environment suitable for proper operation of computer equipment. The air conditioning should provide proper cooling during maximum seasonal conditions. A backup system may be appropriate in areas where air conditioning is not stable. To determine the approximate number of tons of air conditioning required, take the total Btu/hour value of the equipment and divide that number by 12,000. For example, assume your system uses 7 KVAs of power and generates 24,000 Btus of heat. Therefore, 24,000 Btus divided by 12,000 equals 2,000 lbs, indicating 1 ton of air conditioning is required.

Equipment Environment. Although the exact temperature and humidity requirements will vary for individual components, all of Amperif's equipment can operate satisfactorily in an environment with a temperature range of 50°F to 104°F and a humidity range of 20% to 80%. These operating limits are the conditions for the air supply where it enters the cabinet.

Input Power Requirements. The dual controller and disk drives require the following power:

208 Volts, 60 Hertz, three phase, four wire:
3 power and a ground

Variations in voltage should not exceed the following:

Long-term nominal +6%, -10%
Periods of up to 10 seconds +6%, -20%
Periods of up to 500 milliseconds +6%, -25%
Periods of up to 100 milliseconds +6%, -30%
Frequency variation must not exceed 0.5%
Harmonic content must not exceed 5%

CAUTION: **Avoid voltage variations greater than 10% from nominal. Whenever possible, equipment should be supplied from a separate, dedicated transformer.**

Power Distributions. The power for Amperif equipment is obtained from one or more transformers dedicated to this service. The transformers must have shielded primary and secondary windings in order to minimize line noise. The customer must provide one or more circuit breaker panels for the distribution of AC power and ground to the Amperif equipment.

- Input power should come from one or more input transformers which have shielded primary and secondary windings. The neutral side of the transformer must be connected to the building ground point, and the building ground point must be connected to the earth ground.
- A separate power wiring circuit and circuit breaker must be provided for each load.
- Each 208 V three-phase power wiring circuit must consist of four wires: three power lines and a ground. The ground must be connected to the building ground point.
- Power wiring must run through a metallic conduit that serves as a shield against electrical interference. Each run should be as short as possible.
- Each power run must terminate in a suitable receptacle which is located within 60 inches of the equipment or cabinet it serves. For 208 V power requirements, a NEMA L-15-20 receptacle is required. See dual controller environmental specifications in section 4 of this manual for a specification of proper power source receptacles.
- Power wiring must be routed as far as possible from the signal cables.

A dimensional illustration of the dual controller cabinet is provided in figure 12-1. For system specifications and power and voltage requirements, see section 4 of this manual.

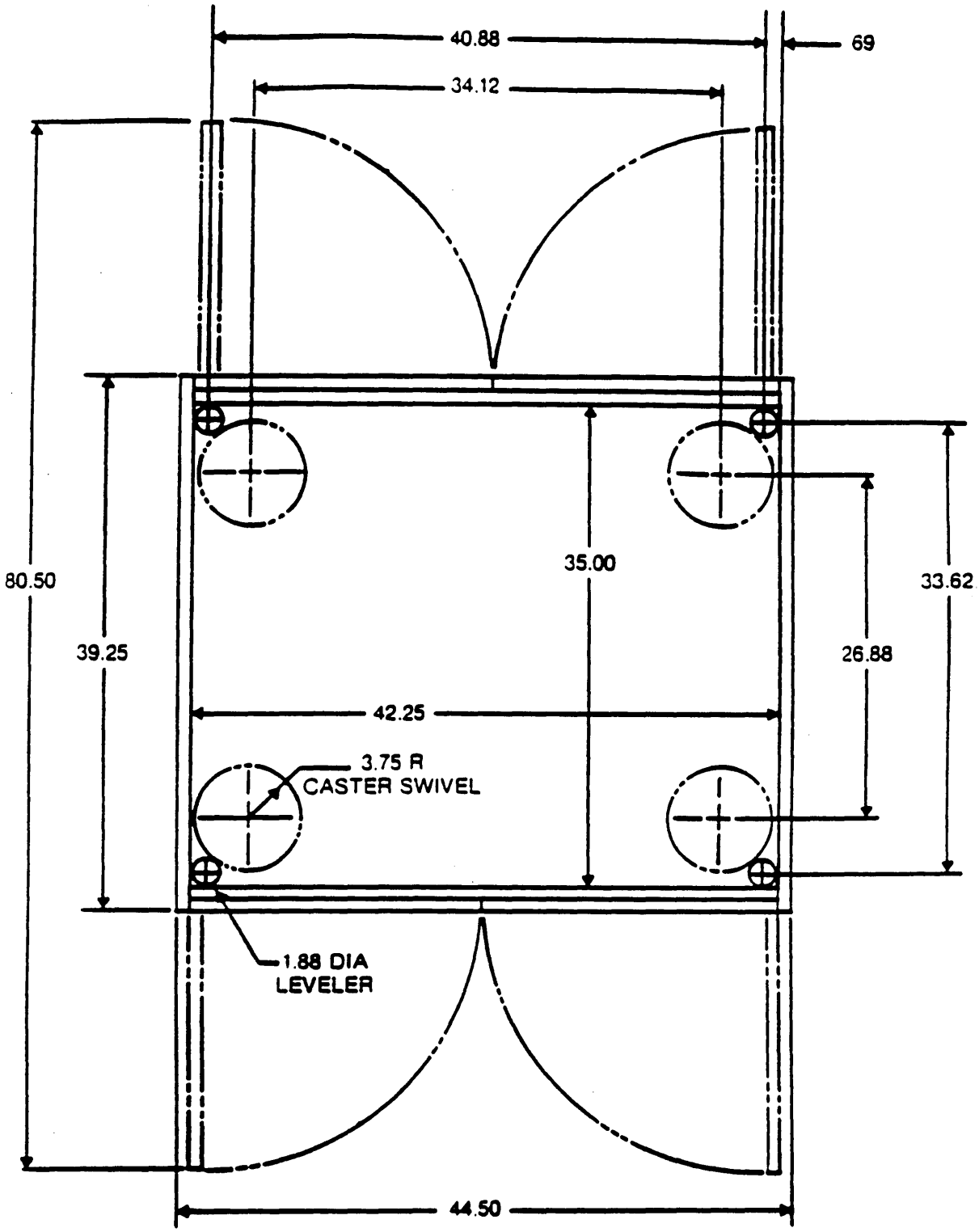


Figure 12-1
Dimensional Illustration of 7001 Mass Storage System

12.1.2 Equipment Unpacking

Unpacking and General Inspection

1. Remove all shipping containers.

   a. Undo all metal band strapping that secures the equipment and the attached ramp in place. Lower the ramp to floor level. If the pallet is a "new" style (see section 12.1.3, Field Packing Procedures, for a description of the "new" and "old" styles), remove the plastic and then attach the ramp to the pallet with the included hinge bolts.

   b. Remove all plastic or cardboard protectors that protected the equipment during shipment.

   c. Remove and retain shipping documentation.

   d. Remove the stretch wrap cellophane that held the eight cardboard corner protectors in place and retain the protectors.

   e. Locate and retain the Quality Assurance documentation package that was shipped with the equipment. Verify that the serial number of the documentation package matches the serial number of the unit.

   f. Remove the eight 9/16-inch bolts that hold the four retaining brackets in place. These brackets surround the four leveling pads which are part of the equipment; the brackets and pads secure the equipment to the pallet.

   g. Turn the leveling footpads until they are completely recessed into the equipment.

   h. Remove the four 9/16-inch bolts that secure the two wooden wheel block assemblies. Slide the block assemblies out from under the equipment.

   i. Use the attached ramp to roll the unit onto the floor and off the pallet.

2. Open all covers and doors and remove all packing material and boxes. Remove the two 7/16-inch shipping bolts on the power supply door.

3. Cut tie-wraps on cables that have been coiled and restrained within the unit for shipping purposes.

4. Check all shock watches which are affixed to the disk drives. If any disk sustained a severe shock in transit, the tube in the shock watch will be red. If the tube is red, the unit may have to be replaced.

5. Check all ribbon cable connections for secure seating and all DC wiring screw lugs for tightness. Also check major mechanical hardware for misalignment which occurred during transit. Remove cardcage cover plates and check seating of all printed circuit boards.

6. Check the equipment to be sure all FCO tags, serial number plates, and UL approval stickers are attached.

7. Inspect equipment for cosmetic shipping damage and broken or missing hardware.

8. If shipping brackets are to be removed from the disk drives, retain them for future use.

9. If the equipment is to be shipped, retain the shipping pallet along with all the hardware. If not needed, please return to Amperif for reuse.

Equipment Inventory

1. Ensure equipment configuration matches the Quality Assurance checksheet in the documentation package shipped with the system.

2. Verify that all I/O cables, grounding cables, lugs, etc., have been received. (See documentation package for cable lengths, number of cables, etc., required.)

3. Remove the covers of the controller boards in the left front of the system and ensure the serial numbers on the boards match those on the quality assurance checksheet. Similarly, check the disk I/O boards at the top left rear corner of the system.

4. Reseat all controller boards and disk I/O boards.

5. Verify that configuration options and jumpers are configured according to specifications. See section 6 of this manual for this information.

Documentation Inventory

1. Open the documentation box shipped with the system. Make sure the 7001 Maintenance Manual is included.

2. The customer engineer installing the system may also want access to the Operator's Manual, the Programmer's Reference, and the System Description for the 7001 Mass Storage System. Contact Amperif Corporation regarding the availability of these documents.

12.1.3 Field Packing Procedures

The 7001 system is transported on one of two different types of pallets. These are referred to as the new and the old style pallets. If your pallet has round, orange rubber "donuts" on it, see the directions for the new pallet immediately following this paragraph. If your pallet has white styrofoam for shock insulation, and plywood on top, see the directions for the old pallet which appear after the "New Pallets" section.

General Inspection and Repacking for New Pallets

1. Obtain equipment documentation.

   a. Collect all Quality Assurance documentation that was shipped with the equipment. Verify that the documentation serial number matches that of the equipment.

   b. Collect all log information that was maintained on the unit. (FCO cards, feature updates, and equipment enhancements, for example.)

   c. Collect all technical documentation to be sent with the equipment.

   d. Secure the documentation into a packet and affix within the equipment.

2. Secure all cable assemblies that are to ship with the equipment; coil and tie-wrap the AC power cord within the unit.

3. Secure access doors.

   a. Secure the power supply door with the two 7/16-inch shipping bolts.

   b. Secure CDCI interface rack assemblies with retaining latch.

   c. Ensure that cardcage cover plates are in place.

   d. Ensure that frame to logic ground shorting strap is installed for shipping.

   e. Ensure that disk drive shipping brackets are installed.

   f. Close and lock the front and rear doors.

4. Secure equipment to the shipping pallet.

   a. Make sure that when equipment is rolled onto the pallet, the front of the unit will face the center of gravity mark on the pallet.

   b. Rotate the leveling pads until they are recessed into the equipment.

   c. Roll the equipment onto the pallet via the attached ramp.

   CAUTION: This is a heavy unit; at least four people should be available to do this.

   d. Use the shipping hardware that was retained upon initial installation (or ordered from Amperif) to slide the wooden wheel block assemblies under the equipment until they are against the wheels and lined up with the bolt holes. Use the four 9/16-inch bolts to secure the assemblies.

5. Install protective wrapping.

   a. Attach center of gravity stickers/indicators, "cut along arrow" sticker, and "front" label at the correct locations. See figure 12-2.

   b. Attach the eight cardboard corner protectors.

   c. Put the top plastic sheet cover over the unit so there is at least six inches of overhang.

   d. Wrap the stretch plastic wrap around the unit until the entire unit has at east two full wraps. Also be sure that the stretch wrap extends at least four inches over the top. See figure 12-3.

   e. Remove the hinges that attach the loading ramp to the pallet and store the ramp up against the equipment. Use bubble wrap or cardboard protectors between the ramp and the equipment. Use the stretch wrap plastic to secure the ramp.

   f. Attach the shipping document envelope, the shipping information label, and both the large and small caution labels at the correct locations. See figure 12-2.

6. Band wrap the equipment to the pallet.

   a. Run two lengths of metal shipping band under the pallet, through the cutouts provided, and then over the equipment. The bands should cross from the front to the back of the equipment.

   b. Tighten the metal bands using the band ratchet tool. While holding the bands with this tool, use the crimping tool to crimp on the retaining brackets. The unit is now ready for pickup.

General Inspection and Repacking for Old Pallets

1. Obtain equipment documentation.

   a. Collect all Quality Assurance documentation that was shipped with the equipment. Verify that the documentation serial number matches that of the equipment.

   b. Collect all log information that was maintained on the unit. (FCO cards, feature updates, and equipment enhancements, for example.

   c. Collect all technical documentation to be sent with the equipment.

   d. Secure above documentation into a packet and affix within the equipment.

2. Secure all cable assemblies that are to ship with the equipment; coil and tie-wrap the AC power cord within the unit.

3. Secure access doors.

   a. Secure the power supply door with the two 7/16-inch shipping bolts.

   b. Secure CDCI interface rack assemblies with retaining latch.

   c. Ensure that cardcage cover plates are in place.

   d. Ensure that frame to logic ground shorting strap is installed for shipping.

   e. Ensure that disk drive shipping brackets are installed.

   f. Close and lock the front and rear doors.

4. Secure equipment to the shipping pallet.

   a. Make sure that when equipment is rolled onto the pallet, the front of the unit will face the center of gravity mark on the pallet.

   b. Rotate the leveling pads until they are recessed into the equipment.

   c. Roll the equipment onto the pallet via the attached ramp.

   CAUTION: This is a heavy unit; at least four people should be available to do this.

   d. Use the shipping hardware that was retained upon initial installation (or ordered from Amperif) to slide the wooden wheel block assemblies under the equipment until they are against the wheels and lined up with the bolt holes. Use the four 9/16-inch bolts to secure the assemblies.

   e. Rotate the leveling pads down until they allow the four retaining brackets to slide in. Use the eight 9/16-inch bolts to secure the brackets to the pallet.

   f. Rotate the leveling pads until they are snug and secure against the brackets.

5. Install protective wrapping.

   a. Attach center of gravity stickers/indicators, "cut along arrow" sticker, and "front" label at the correct locations. See figure 12-2.

b. Attach the eight cardboard corner protectors.

c. Put the top plastic sheet cover over the unit so there is at least six inches of overhang.

d. Wrap the stretch plastic around the unit until the entire unit has at least two full wraps. Also be sure that the stretch wrap extends at least four inches over the top. See figure 12-3.

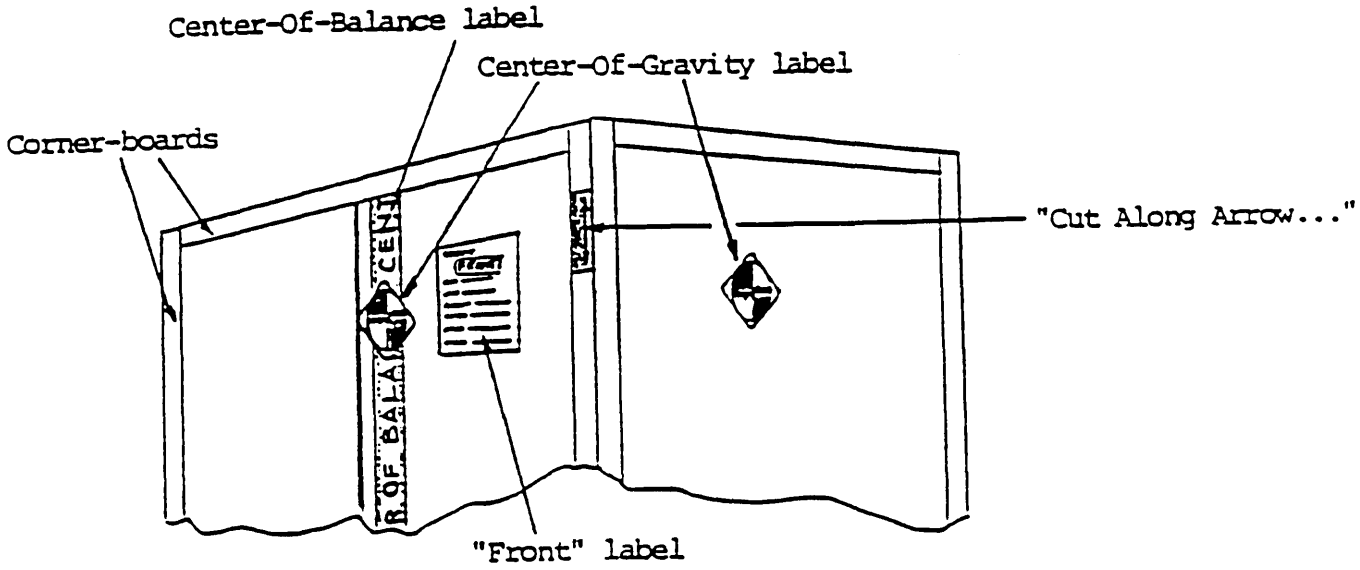
e. Attach the shipping document envelope, the shipping information label, and both the large and small caution labels at the correct locations. See figure 12-2.

6. Band wrap the equipment to the pallet.

   a. Run two lengths of metal shipping band under the pallet and over the equipment. The bands should cross from the front to the back of the equipment.

   b. Tighten the metal bands using the band ratchet tool. While holding the bands with this tool, use the crimping tool to crimp on the remaining brackets.

   c. Lift the attached loading ramp up to the equipment. Insert bubble wrap or cardboard corners between the ramp and the equipment. Secure the ramp using one wrap of the metal banding. The unit is now ready for pickup.



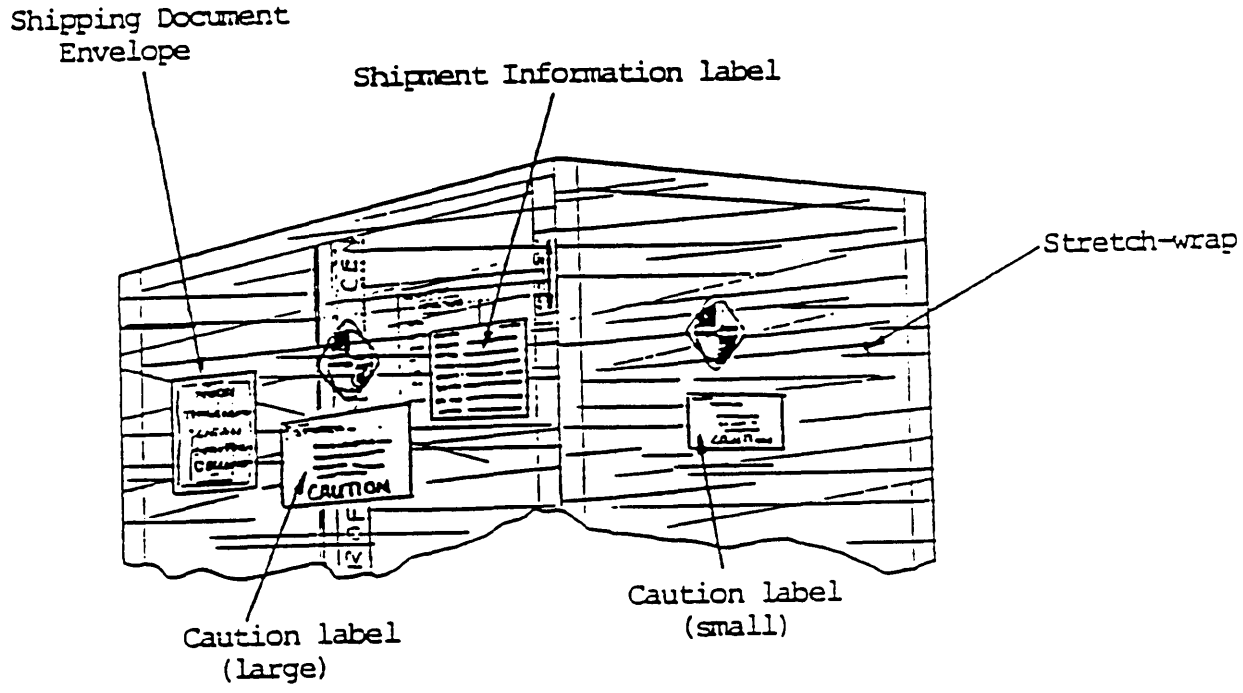
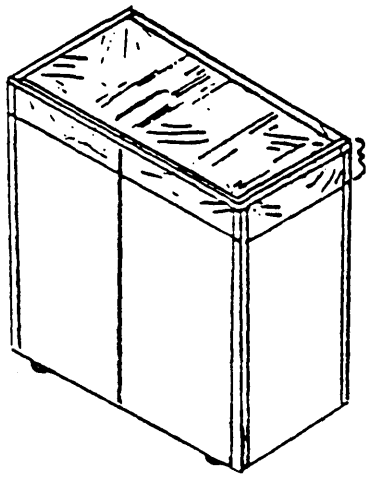
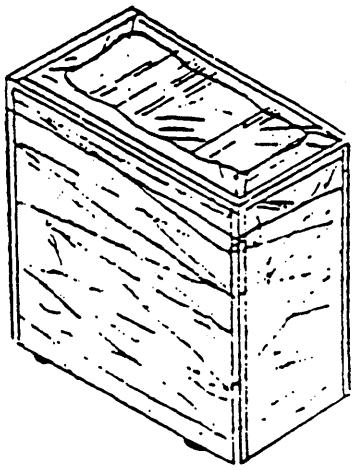
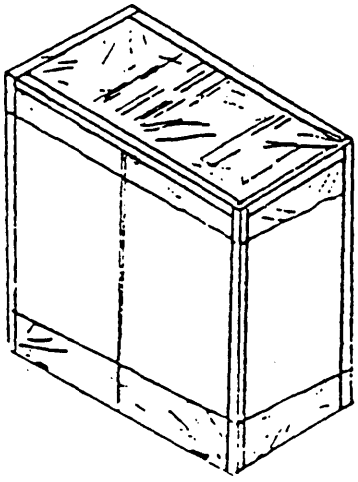


Figure 12-2
Label Location



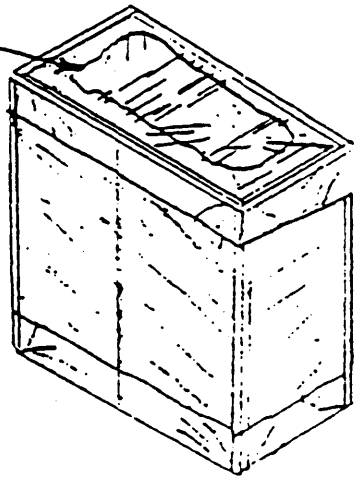
Top sheet cover.
minimum of 6" of
film overhang





Bottom sheet application
if shipping spec requires
full enclosure.
Note: Desiccant must be
included.

Minumum of 4" of film
over the top.



stretch wrap shall
cover part of skid

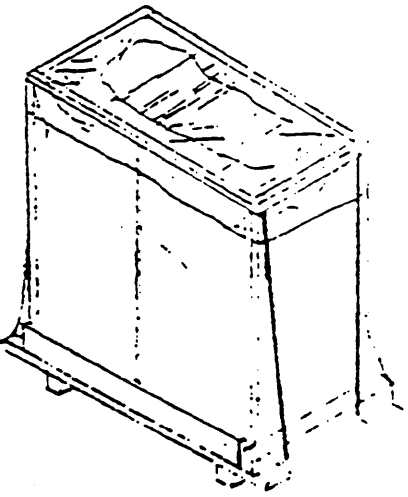


Figure 12-3
Stretch Wrap Application

12.2 Installation of 7001 Cabinet

This section describes the procedures for installing the 7001. These procedures include verifying that logic ground to frame ground is open, connecting logic ground to system ground, and making I/O connections between the 7001 and the host.

12.2.1 Logic Ground to Frame Ground Check

Remove the logic to frame ground shorting wire at the rear of the system. Using a VOM, verify that logic ground to frame ground is open. Logic ground may be referenced at the logic ground lug located on the DC voltage distribution panel in the rear middle portion of the 7001 cabinet (see figure 12-4). Frame ground may be referenced at any unpainted metallic point on the 7001 cabinet frame. A good choice would be the I/O connector mounting bracket.

12.2.2 Logic Ground Connections

Connect logic ground from controller logic ground lug to system ground.

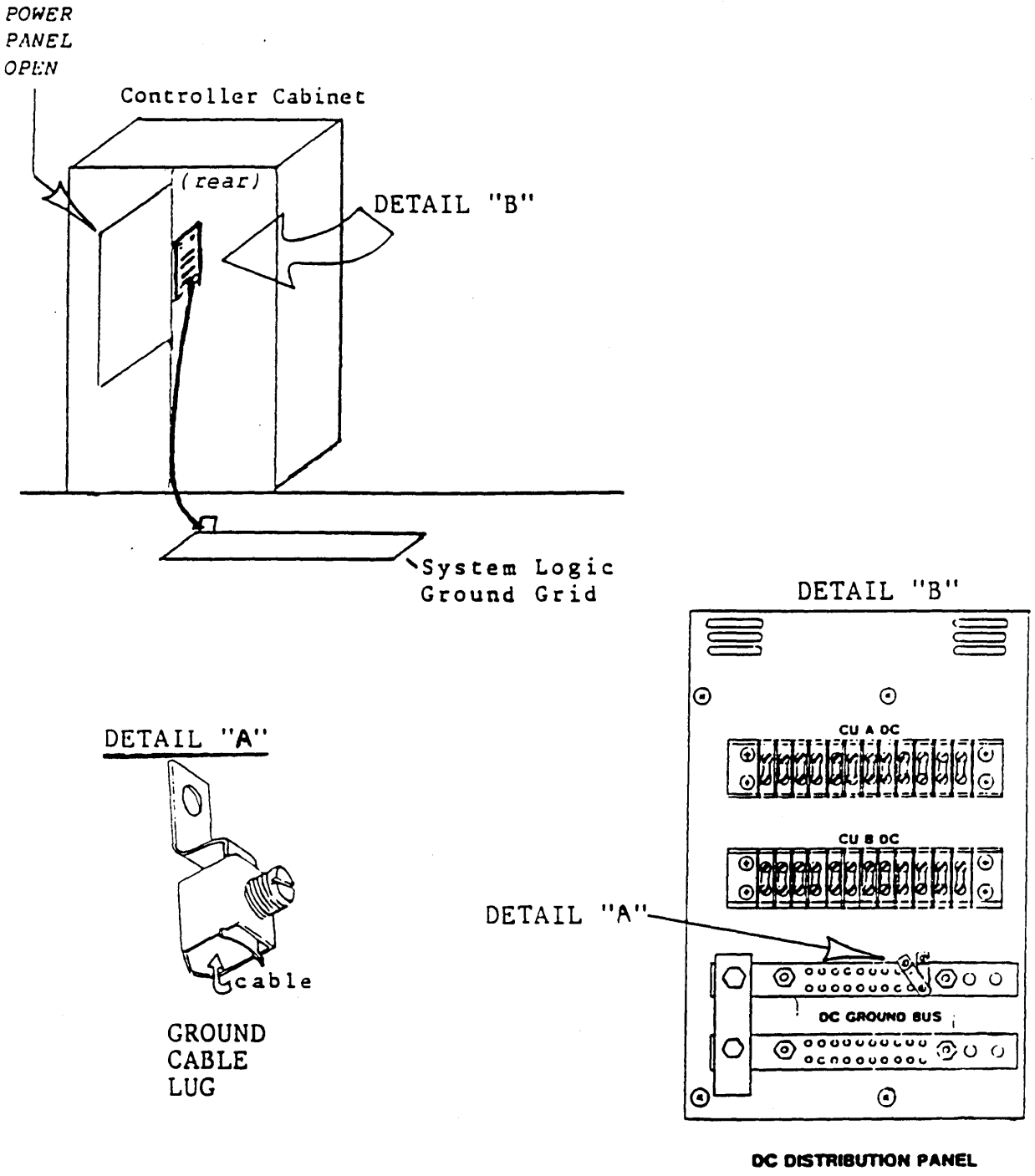


Figure 12-4
System Grounding Detail

12.2.3 I/O Connections

Verify system I/O path configuration with customer. Run I/O cables from controller cabinet to CDC I/O cabinets. Label the cables at this time to ensure proper connection and for future reference should they be disconnected for maintenance purposes. Cables should be labelled as to whether they connect through controller A or B and whether they connect through CDCI 0,1,2, or 3. Connect I/O cables to proper CDCI ports within the controller cabinet as illustrated in figure 12-5.

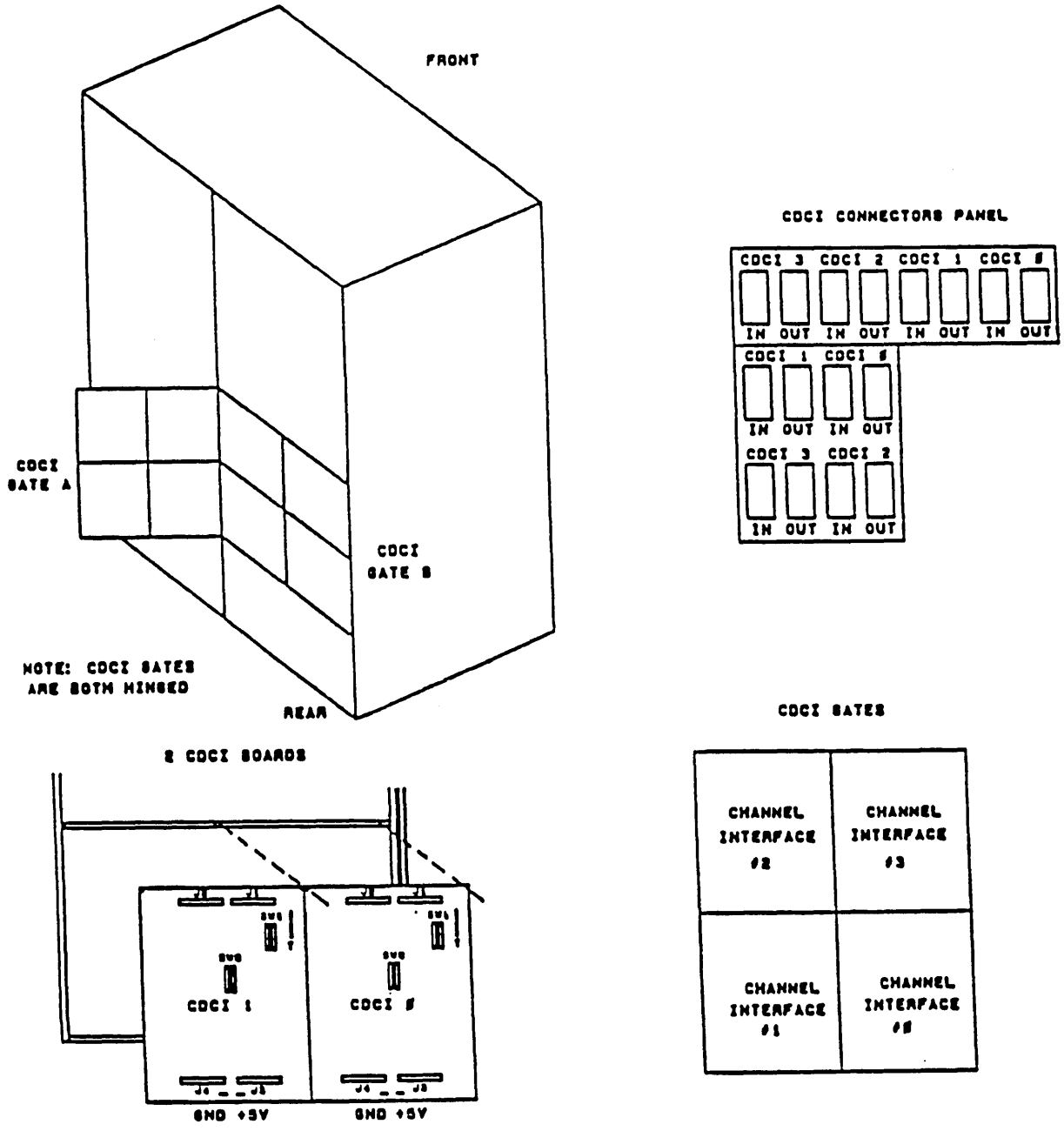


Figure 12-5
CDCI Gates

12.2.4 AC Power Connections

1. Ensure all circuit breakers on the controller cabinet.

2. Measure the voltage at the receptacle and ensure that it is as specified under "Input Power Requirements" at the beginning of this section.

3. Remove the tie wraps securing the AC power cord and route the cord through the cutout in the system floor and out to the receptacle.

4. Plug AC power cord into proper receptacle.

CAUTION: For 50 Hz systems, the plug of the AC power cord is supplied by CDC and must be grounded before the system is powered up.

12.2.5 Equipment Leveling

After all logic ground, I/O and AC power connections are completed, level the controller cabinet by lowering the leveling pads, with the understanding that most of the weight of the system must remain on the wheels. Recheck equipment leveling after a few days and adjust, if necessary, for any settling that may have occurred.

12.2.6 Power On Checks

1. Turn on the MAIN and FANS circuit breakers located in the AC power box. See figure 12-6.

2. Check that all fans inside and above the controller are operational.

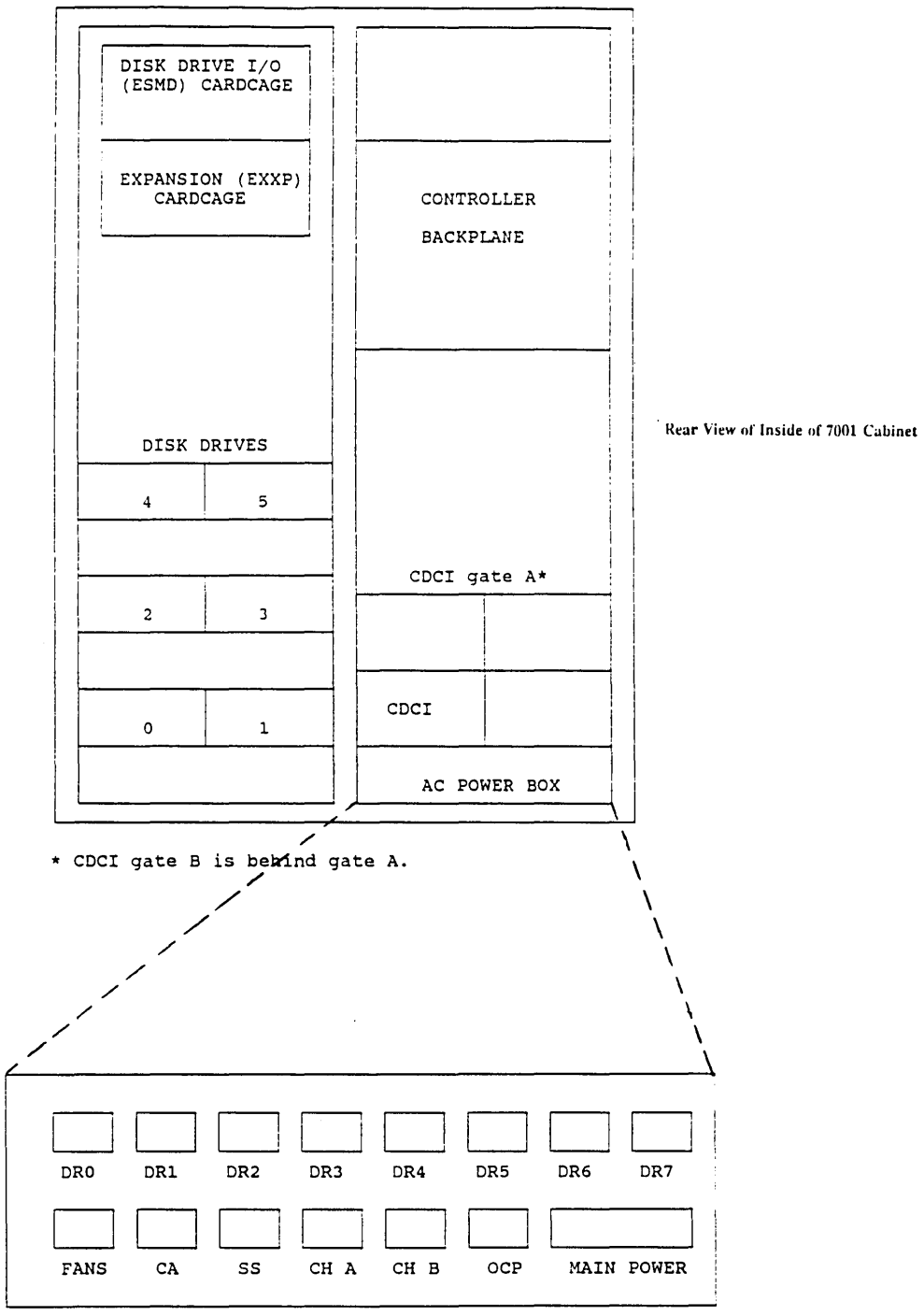
3. Turn on the OCP, CHANNEL A, and CHANNEL B circuit breakers located in the AC power box in the order listed.

4. Using a voltmeter, check the following voltage measurements and adjust if necessary. See section 11 for adjustment procedures.

   a. +5V $\pm$ 5% on the OCP power supply measured between the center terminal on the DC ground bus bar and the controller backplane terminal TP5. See section 11.2.5 for adjustment procedure.

   b. +5V $\pm$ 5% on the CHA and CHB power supplies, measured between the left (CHB) terminal on the DC ground bus bar and the TP4 terminal on the controller backplane, and between the right (CHA) terminal on the DC ground bus bar and the TP6 terminal on the controller backplane. -5V $\pm$ 5% measured at the CDCI board of the disk I/O cardcage.

   d. +5V $\pm$ 5% ripple test on OCP power supply and on CHA and CHB power supplies measured at locations in steps b and c above.



Rear View of Inside of 7001 Cabinet

NOTES: *DR1 controls drives 0 and 1; DR3 controls drives 2 and 3; DR5 controls drives 4 and 5. DR0, DR2, DR4, DR6, DR7, CA, and SS are nonfunctional in the 7001.*

Figure 12-6
AC Power Box

12.3 System Initialization

The following two sections provide procedures for initializing the controllers and disk drives. The third section provides procedures for verifying that alternate tracks have been assigned to disks.

12.3.1 Initialize Controllers

1. Turn on all circuit breakers on power distribution panel behind the cabinet.
2. At the OCP keypad press **PROGM 4** and initialize both controllers (see section 5.2.18). Make sure **CHANNEL READY** appears at the OCP display.
3. Initialize the OCP. See section 5.2.20 for instructions.

12.3.2 Initialize Disk Drives

1. Turn on all circuit breakers for drives in controller cabinet.
2. Power up disk drives at front panel by pressing START switches. Make sure each drive is ready (READY light appears on drive control panel) before proceeding to the next one. Drives should already be formatted from the factory.
3. Run a Verify (ILD 2) to all drives from both controllers, as described in section 5.2.28. Run this ILD to all cylinders and all heads.
4. To verify headers, load MODE 1 before performing any seeks.
5. Run an Oscillating Seek (ILD 5) to all drives from both controllers, as described in section 5.2.30.
6. Run a Random Seek (ILD 6) to all drives from both controllers, as described in section 5.2.31.
7. Run a Sequential Seek (ILD 7) to all drives from both controllers, as described in section 5.2.32.

12.3.3 Verify that Alternate Tracks Have Been Assigned to Disks

Verify alternate tracks by performing the ILD 3 procedure outlined in section 5.2.29.

12.4 OCP Offline Checkout/Testing

This section describes how to verify that the Operator Control Panel (OCP) is working properly. It is not necessary to go through the entire procedure when performing the functions in this section. Just perform the first two or three instructions to make sure the OCP and keypad are functioning correctly.

This section provides only a quick reference of the DISP, LOAD, PROGM and ILD functions.

12.4.1 Display/Load Functions

The DISP or LOAD key specifies a particular register, data, status or message which may be displayed at the OCP or loaded into the system. To check the following load and display functions, press the DISP or LOAD key and then press the appropriate function key number.

Function Key	Description
0/TOD	Time of day
1/BUT	Backup time
2/INT	Interval time
3/DSW	Data switch register
4/TOG	Toggle switch register
5/PB	Push button register
6/PRS	Present unit status *
7/REQ	Requested unit status *
8/PASS	Password/clearance status
9/EVC	Event counter
A/BRK	Break point address
B/MODE	Mode register
C/PGM	Program display *
D/MSG	System message

* No LOAD function.

12.4.2 Program Functions

The PROGM key specifies a certain program to be performed. To check the following Program functions, press the PROGM key and then press the appropriate function key number.

Function Key	Description
0	Introduction routine
4	Initialize channel
8	Initialize OCP
9	Initialize RAM
A	8085 editor mode
C	Repeat XMC clear
E	Slow run mode
F	Single step mode

12.4.3 Inline Diagnostic (ILD) Functions

The ILD key specifies an inline diagnostic or operating function to be performed. To check the following inline diagnostic functions, press the ILD key and then press the appropriate function key number.

Function Key	Description
0	ILD halt
1	Format and verify drive
2	Verify drive
3	Verify one track
4	Alternate defective track
5	Oscillating seek
6	Random seek
7	Sequential seek
8	Clear disk drive ECC display

12.5 Offline Installation Testing

Once you have completed the ILD tests in section 12.4.2, perform the following procedures. (Additional information about these utilities is provided in section 5.4.)

1. Perform a Write and Read using hex function 50X where X is the device address.
2. Perform a Read Data using hex function 2EX where X is the device address.
3. Perform a Write Manufacture Data using hex function 4EX where X is the device address.

13. PREVENTIVE MAINTENANCE

This section provides the recommended preventive maintenance procedures for a 7001 System. Since the 7001 is relatively maintenance-free, it requires minimal upkeep time.

13.1 Daily Checks

The following procedures tell you what checks you need to perform on a daily basis. There are separate checks for the controller and the disk drives.

13.1.1 Controller Checks

1. At the OCP keypad, press **DISP 6** to check the present drive states. Make sure all the drives are in their proper state.

2. At the OCP keypad, press **DISP 0** to check the time-of-day clock. Make sure the 7001 clock and the CDC host clock are in sync.

3. If applicable, verify that the interval timer (press **DISP 1**) and backup timer (press **DISP 2**) are set at their proper values.

13.1.2 Disk Drive Checks

Check the disk ECC error logs (at display locations 431-436) and the daily system error reports. These reports indicate that a bad spot has been found on a disk. If the same error cylinder and head appear several times during the course of a week, schedule time to assign an alternate track for that area.

13.2 Quarterly Checks

The following procedures tell you what checks you need to perform on a quarterly basis. There are separate checks for the controller, the disk drives, and the OCP power supplies.

13.2.1 Controller Checks

1. Perform a visual check of the inside of the dual controller cabinet. Look for loose cables and cable harnesses.
2. Make sure fans are turning properly and that nothing is obstructing the fans.
3. Remove the fan cage (see section 10) and wipe the blades clean. Replace the fan cage after cleaning the fan blades.
4. Check all power supply voltages and adjust if necessary. See section 11 for these procedures.

13.2.2 Disk Drive Checks

1. Check for loose cables at the I/O section of the controller and the disk drives.
2. Check all drive fans for proper operation.
3. Check all power supply voltages and adjust if necessary. See section 11 for these procedures.

13.2.3 OCP Power Supply Checks

Check all power supply voltages and adjust if necessary. See section 11 for these procedures.

JPS 11-7-89

```
MST - MASS STORAGE TEST.
G. R. MANSFIELD.  70/12/06.
MODIFIED BY W. E. GOEBEL.  74/01/21.



MST IS A CENTRAL PROCESSOR DRIVEN MASS STORAGE TEST.  IT
PERFORMS SEQUENTIAL WRITES, READS AND POSITIONS ALONG WITH
RANDOM READS AND WRITES ON A SELECTED MASS STORAGE DEVICE.

OPERATING INSTRUCTIONS.
WHEN CALLED, MST WILL REQUEST ASSIGNMENT OF THE FILE *DISK1*.

SEQUENTIAL WRITE.
RANDOM DATA IS WRITTEN SEQUENTIALLY ON THE FILE IN THIS
FORMAT -              1 WORD CONTAINING THE SECTOR NUMBER
                      1 WORD CONTAINING RANDOM DATA SEED
                      61 WORDS OF RANDOM DATA
                      1 WORD CHECKSUM OF ABOVE DATA

SEQUENTIAL READ.
FILE IS REWOUND AND DATA IS READ BACK CHECKING SECTOR NUMBER
AND CHECKSUM OF RANDOM DATA.

SEQUENTIAL POSITIONING.
FILE IS POSITIONED ALTERNATELY TO SUCCESSIVE SECTORS
FROM BEGINING TO END.

RANDOM READ.
RANDOM SECTOR NUMBERS ARE PICKED AND THE SECTORS READ.
THE SECTOR NUMBER IS CHECKED AND THE DATA CHECKSUM VERIFIED.

RANDOM WRITE.
RANDOM SECTOR NUMBERS ARE PICKED AND THE SECTORS ARE WRITTEN.
A SEQUENTIAL READ IS PERFORMED TO VERIFY THE WRITTEN DATA.

FOR BUFFERED DISKS THERE IS A THREE SECOND PAUSE FOLLOWING
EACH SECTION TO ALLOW I/O ACTIVITY TO COMPLETE ON THE
DISK BEFORE CONTINUING TO THE NEXT SECTION.



ARGUMENT PARAMETERS.

T       TEST SECTION (CAN BE EQUATED).
        T=0 OR T OR OMISSION OF THIS PARAMETER WILL RUN ALL
            SECTIONS.
        T=1 WRITE SEQUENTIAL.
        T=2 READ SEQUENTIAL.
        T=3 POSITION SEQUENTIAL.
        T=4 RANDOM READ.
```

DOES NO NEW WRITES. ASSUMES RANDOM WRITTEN

FROM SYSTEM TYPE X.MST(N=10000) PAGE 1/1

END OF TEST

XXX=FJSN ONSW,XXXX,3 — TO REQUEST ASSIGN,XXXX,YY YY = EST OF DISK TO TEST

FROM "DIS" DMS IN

MST, T = ..., N = 10000

T=5 RANDOM WRITE.

P TEST PATTERN (CAN BE EQUATED).
P=0 ALL ZEROS PATTERN.
P=1 ALL ONES PATTERN.
P=2 252525252525252525B PATTERN.
P=3 525252525252525252B PATTERN.
P=4 DO NOT GENERATE OR CHECK DATA. SECTOR NUMBERS ARE GENERATED AND CHECKED.
P=5 OR P OR OMISSION OF THIS PARAMETER WILL ENABLE RANDOM PATTERN.

N NUMBER OF SECTORS (CAN BE EQUATED).
N=0 GIVES ARGUMENT ERROR MESSAGE AND PROGRAM ABORT.
N=XXXX WILL ENABLE THE TEST TO BE RUN ON XXXX SECTORS. (BE CAREFUL THAT TRACK LIMIT IS NOT EXCEEDED)
N GIVES DEFAULT VALUE (SEE TABLE PRSA).

NW NO WRITE PERFORMED AT BEGINING OF TEST.

TL TRANSFER LENGTH IN SECTORS FOR RANDOM I/O. DEFAULT IS 108 SECTORS.

NV IF SPECIFIED, DO NOT PERFORM SEQUENTIAL READ AFTER RANDOM WRITE.

RO IF SPECIFIED, SIMULATE ROLLIN/ROLLOUT I/O ON BUFFERED DEVICES.

IO IF SPECIFIED, GIVES THE NUMBER OF I/O-S TO BE PERFORMED ON THE DEVICE. IF *IO* IS NOT SPECIFIED, THE VALUE FOR NUMBER OF I/O-S IS COMPUTED FROM THE TRANSFER LENGTH.

NOTE:

SENSE SWITCH 2 - IF SET WILL ABORT ON ERRORS.
SENSE SWITCH 3 - IF SET WILL CONTINUE AT END OF TEST.
SENSE SWITCH 4 - IF SET WILL REPEAT CURRENT SECTION.

ISSUING A CALL OF MST FROM THE CONSOLE WILL SELECT ALL SECTIONS, RANDOM PATTERN, DEFAULT SECTOR VALUE, PAUSE ON ERROR AND STOP AT END OF TEST. TO CONTINUE ON ERRORS TYPE *GO.*.

DAYFILE MESSAGES.

* ARGUMENT ERROR.* = ONE OF PARAMETERS IS IN ERROR.

* ILLEGAL EQUIPMENT.* = THE EQUIPMENT WHICH WAS ASSIGNED IN CONTROL DATA CORPORATION DOCUMENTATION.

RESPONSE TO THE DISPLAY REQUEST IS NOT
RECOGNIZED AS BEING A DEVICE UPON WHICH
THE TEST MAY BE RUN.

* SEQUENTIAL WRITE.* = THIS TEST SECTION IS BEING EXECUTED.

* SEQUENTIAL READ.* = THIS TEST SECTION IS BEING EXECUTED.

* SEQUENTIAL POSITIONING.* = THIS SECTION IS BEING EXECUTED.

* RANDOM READ.* = THIS TEST SECTION IS BEING EXECUTED.

* RANDOM WRITE.* = THIS TEST SECTION IS BEING EXECUTED.

MST TRANSFER RATE = XXXXXX.XXX KC. = THE DISK TRANSFER
RATE FOR THE PREVIOUS SECTION WAS
XXXXXX.XXX KILO-CHARACTERS PER SECOND.

* NUMBER OF I/O-S = XXXXXXXXXX.* = THE NUMBER OF IO PAIRS
SPECIFIED WITH THE *IO* PARAMETER OR
COMPUTED FROM THE *NL* PARAMETER.

* IO PER SECONDS = XXXXXX.XXX.* = NUMBER OF IO-S PERFORMED
PER SECOND.

* FILE SIZE = XXXXXXXXXX SECTORS.* = SIZE OF THE DATA
FILE IN SECTORS.*

* ILLEGAL EOF DETECTED.* = AN EOF WAS DETECTED BEFORE THE
LAST SECTOR ON THE FILE.

* NO EOF DETECTED ON LAST READ.* = NO EOF ON THE LAST SECTOR.

* JOB ABORTED.* = ABNORMAL TERMINATION OF MST.

EQXXX,DATA ERROR AT -PHYSICAL POSITION-.
EQXXX,RXXXXXXX,TYYYY,SZZZZ.
DATA ERRORS HAVE BEEN DETECTED ON A
SECTOR WHICH WAS READ.

EQXXX,POS. ERROR AT -PHYSICAL POSITION-.
EQXXX,RXXXXXXX,TYYYY,SZZZZ.
THE SECTOR WHICH WAS READ WAS NOT
THE CORRECT SECTOR. THE POSITION GIVEN
IS THE POSITION OF THE SECTOR READ.

EQXXX,DEV.-TYPE ERR--PHYSICAL POSITION-.
EQXXX,RXXXXXXX,TYYYY,SZZZZ.
CIO HAS DETECTED ONE OF THE FOLLOWING
ERRORS WHICH APPEAR IN THE -TYPE ERR-
POSITION.
-TYPE ERR- = PARITY ER. -- PARITY ERROR
ADDR. ERR. -- ADDRESS ERROR

```
                    STATUS ER.  -- DEVICE STATUS ERROR
                    81 FNC REJ  -- 6681 FUNCTION REJECT
                    RESERVED    -- DEVICE RESERVED
                    NOT READY   -- DEVICE NOT READY

*EQXXX,EXP. POSITION -PHYSICAL POSITION-.*
*EQXXX,RXXXXXXX,TYYYY,SZZZ7.*
                    WHEN A POSITION OR DEVICE ADDRESS ERROR
                    OCCURES THE EXPECTED POSITION IS GIVEN
                    BY THIS MESSAGE.

*EQXXX,DATA EXP  WWW,EEEEEEEEEEEEEEEEEEEE*
*EQXXX,DATA READ WWW,RRRRRRRRRRRRRRRRRRRR*
*EQXXX,DATA DIFF WWW,DDDDDDDDDDDDDDDDDDDD*
*DATA OK.*  (OPTIONAL - SEE BELOW)
                    WHEN A DATA ERROR OR DEVICE PARITY ERROR IS
                    DETECTED THE DATA ON THE SECTOR IS CHECKED
                    AND THE ERRORS REPORTED.  IF NO ERRORS ARE
                    FOUND THE MESSAGE *DATA OK.* IS ISSUED.
                        WWW IS THE WORD NUMBER IN THE SECTOR.
                        EE------E IS THE EXPECTED DATA.
                        RR------R IS THE DATA READ.
                        DD------D IS THE DIFFERNCE.

* MST ERROR - GO / DROP.* = *MST* HAS DETECTED AN
                    IRRECOVERABLE READ ERROR.

* END MASS STORAGE TEST.* = END OF TEST.
```

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IAB

REVISED AMPERIF 7100 TEST PROCEDURES
TEST PROCEDURES

FOR THE

AMPERIF 7100 PRODUCT

By Jim Marek
R. L. Clark

December 5, 1990

1.0 INTRODUCTION

This set of test procedures is designed to complement the Revised Test Plan for Amperif 7100 Product dated October 24, 1990, author R. L. Clark . It provides the details for the Design Verification Testing (DVT) testing and assuring test replication beyond DVT. (The Appendices of the Revision 1 of the Test Procedure Document are to be used for all the background information relative to deadstarts and usage of tools during the testing.)

The procedures are organized to follow tests as listed in the Test Plan. Appendices are included to provide details on procedures common to all the tests, such as deadstart.

2.0 HARDWARE COMPONENT PATH ACCESS TESTS

see Amperif MASS STOR. MAINT MANUAL

These tests are identified in paragraph 7.1, 7.2 and 7.3 of the Test Plan.

2.1 DRIVE CONTROL PANEL TESTS

The seven tests are to verify a subset of the switches and indicators on the disk drive control panel. The actual procedure to be followed for verification appears in reference 2.0 (h, section 2.6.) of the Test Plan.

see Amperif manual

2.1.1 POWER UP SWITCH

2.1.2 DRIVE READY LIGHT

2.1.3 PANEL DRIVE SELECT

2.1.4 PANEL DRIVE SELECT ALL

2.1.5 DRIVE A PORT ENABLE

2.1.6 DRIVE B PORT ENABLE

2.1.7 DRIVE FAULT CLEAR

2.2 IN-LINE DIAGNOSTICS

These tests are to verify the accessibility of disk drives from the Operator Control Panel (OCP). The actual procedure to be followed for verification appears in reference 2.0 (h, section 5.4) of the Test Plan.

2.2.1 ASSIGN ALTERNATE TRACKS ILD4

2.2.2 RANDOM SEEK TEST

2.2.3 SEQUENTIAL SEEK TEST

2.2.4 CLEAR DISK ECC DISPLAY LOG

2.2.5 ADAPTER OFF-LINE DIAGNOSTIC/UTILITY TEST ILD B

2.3 CYBER CHANNEL TEST

This test will verify that the CYBER channel interface and its support processor will function per design product specification. The following sequence of commands will be entered per reference 2.0 (h, section 5.2) of the Test Plan.

```
loop count
seek
write
operation complete
seek
read
operation complete
driver release
end sequence.
```

3.0 NOS IN STAND-ALONE MODE

These tests are to verify the reliability of the disk subsystem under NOS.

Test 1A - Disk Subsystem Reliability

Start the test

Deadstart the CYBER 830 using CMRDECK 20. See Appendix A of revision 1 of Test Procedure for deadstart procedure.

Enter X.BEGT(1A) from the system console to begin the test.

Verify the testing as it progresses.

To verify that the testing is proceeding normally, enter AB. on the system console. The B display, on the right side of the console, should be displaying 16 jobs with one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
SEQUENTIAL POSITIONING
RANDOM READ
RANDOM WRITE
RANDOM POSITIONING
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Each of the disk devices that has a DQ type should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.

X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST1A and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 1B - Dual Channel Test

Start the Test

If NOS is not running using CMRDECK 20, deadstart using CMRDECK 20.

Enter UNLOCK.
ENABLE,ENGR.
X.BEGT(1B) from the system console to begin the test.

Testing Dual Channel Support

Enter DOWN,CH=4. from the system console to prevent access to the disks via channel 4.

Enter W,C. and verify that channel 4 is not being assigned to PPs.

Enter WB. and verify that all the MST jobs are proceeding through their test loops and are changing their status messages on the B display. If status okay, enter UP,CH=4. and verify on the W,C display that channel 4 is now being assigned to PPs.

Enter DOWN,CH=24. and verify that channel 24 is not being assigned to PPs. Verify that all the MST jobs are proceeding through their test loops and are changing their status messages on the B display. After you are convinced that everything is okay, enter UP,CH=24. and verify on the W,C display that channel 24 is now being assigned to PPs.

Terminate the Test and Collect Results

Enter DISABLE,ENGR.
DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.

X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST1B and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

REVISED TEST PROCEDURES FOR AMPERIF 7100 PRODUCT
Revision 2 December 5, 1990

Test 1C - Deadstart Test after restoring power

Start the Test

If NOS is not running using CMRDECK 20, deadstart using CMRDECK 20.

Enter X.BEGT(1C) *(new proc)* from the system console to begin the test.

Cut power to CYBER and 7100. Then restore power.

Determine that the 7100 disks are in a state of readiness. Use CMRDECK 20 to deadstart.

Verify NOS is restored.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.
X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST1C and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 1D - Error Detection Test

Start the Test

If NOS is not running using CMRDECK 20, deadstart using CMRDECK 20.

Enter X.BEGT(1D) from the system console to begin the test.

Testing Error Detection

Enter UNLOCK.
ENABLE,ENGR.

Introduce the appropriate error conditions.

Enter DISABLE,ENGR. and retry the test with ESS running.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.

X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST1D and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 1E - Independent power down of controllers

Start the Test

If NOS is not running using CMRDECK 20, deadstart using CMRDECK 20.

Enter X.BEGT(1E) *(This proc may have to be modified since it was associated with the flawing of tracks in rev I of the Test Procedures.)* from the system console to begin the test.

Cut power to 7100 controller A.

Determine that all channels except ?? are in normal up status to NOS.

Restore power to controller A.

Cut power to 7100 controller B.

Determine that all channels except ?? are in normal up status to NOS.

Restore power to controller A.

Verify NOS is restored to the same state as prior to the power shutdown of controllers A and B.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.

X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST1E and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 1F - Empros environment test

(To be determined)

4.0 VOLTAGE MARGIN TESTS

Test 4A - 830 Voltage Margin Test

Start the Test

For the 830, enter

```
UIM
GO, VERIFY
R
```

Run test for one hour and 45 minutes.

Terminate the Test and Collect Results

Test 4B - 825 Voltage Margin Test

If NOS is not running using CMRDECK 20, deadstart using CMRDECK 20.

Enter X.BEGT(4) from the system console to begin the test.

For the 825, set voltage I/O margins on backpanel

First at -5V %

Run MST test for 30 minutes

Set at +5V %

Run MST test for 30 minutes

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.
X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST4B and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

5.0 CABINET INTERCONNECT VIA CONTROLLERS TESTS

Test 2A - Dual Channel Performance Test

Start the test

Deadstart the CYBER 830 using CMRDECK 20.

Enter X.BEGT(2A) from the system console to begin the test.

Verify the testing as it progresses

To verify that the testing is proceeding normally, enter AB. on the system console. The B display, on the right side of the console, should be displaying MST jobs. These are recognizable because they will be displaying one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
SEQUENTIAL POSITIONING
RANDOM READ
RANDOM WRITE
RANDOM POSITIONING
UCMS, 1048.576 KUNS.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Wait for an highlighted message indicating that the test is done.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.X.GETRF. on the system console and mount a scratch tape. When the job requests a tape enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST2A and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 2B - Shared Disk/Multiple Write Test

Start the test

Startup the "primary" system

Deadstart the "primary" CYBER (830) using CMRDECK 22.

Enter E,M.

```
ON,EQ=26.
NSD,26.
ON,EQ=40.
NSD,40.
```

to bring up equipments 26 and 40 in nonshared mode. Both equipments should have an NS in the NOTES column on the E,M display.

Enter X.BEGT(2B,C) to create files on equipments 26 and 40. When it is done, enter UNLOAD,26. When UA appears in the NOTES column, enter ESD,26. Enter UNLOAD,40. When UA appears in the NOTES column, enter ESD,40. to bring up equipments 26 and 40 in shared mode. Both equipments should have an ES in the NOTES column on the E,M display.

Enter X.BEGT(2B,P) to begin testing on the "primary" system.

Startup the "secondary" system

Deadstart the "secondary" CYBER (830) using CMRDECK 12.

Enter E,M.
ON,EQ=26.
ESD,26.
ON,EQ=40.
ESD,40. to bring up equipments 26 and 40 in shared mode. Both equipments should have an ES in the NOTES column on the E,M display.

Enter X.BEGT(2B,S) to begin testing on the "secondary" system.

Verify the testing as it progresses

To verify that the testing is proceeding normally, enter AB. on the 830 system console. The B display, should be displaying 2 MST jobs with one of the following status messages:

SEQUENTIAL READ
RANDOM WRITE
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Equipments 26 and 40 should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Repeat the checks on the CYBER 825.

Terminate the Test and Collect Results

Enter DROP,,EX. on the CYBER 830 system console. All the jobs at control points should terminate and disappear.

Enter MAG.X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST2B and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Repeat the termination process on the CYBER 825.

Test 2C - Disk level component failure

Start the test

Deadstart the CYBER 830 using CMRDECK 22.

Remove one controller disk port from ? data drive

Enter X.BEGT(2C) from the system console to begin the test.

Verify the drive marked down by NOS via A, ERROR LOG.

Enter E,M. on the system console. Each of the disk devices that has a DQ type should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Replace controller disk port for data disk ?.

Remove one controller disk port from ?? data drive

Follow prodedures directly above for verifying NOS marks down the disk.

Replace controller disk port for data disk ??.

Remove one controller disk port from ? system drive
Follow prodedures directly above for verifying NOS marks down the disk.

Replace controller disk port for system disk ?.

Remove one controller disk port from ?? system drive

Follow prodedures directly above for verifying NOS marks down the disk.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST2C and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 2D - Channel disable test

Start the Test

If both CYBERs are not already up in a primary/secondary configuration, start this test using the instructions for test 2B, except that the X.BEGT commands must specify test 2D instead of 2B. To verify that the CYBERs are in a primary/secondary configuration, enter E,M. on both the 830 and the 825 and verify that equipments 26 and 40 have an ES in the NOTES column on both consoles. If so, enter X.BEGT(2D,P) to begin testing on the "primary" (830) system, and enter X.BEGT(2D,S) to begin testing on the "secondary" (825) system. Verify the testing as it progresses. To verify that the testing is proceeding normally, enter AB. on the 830 system console. The B display, should be displaying 2 MST jobs with one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
RANDOM WRITE
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Equipments 26 and 40 should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Introduce a channel failure

Enter UNLOCK.
ENABLE,ENGR.

Enter DISABLE,ENGR. and retry the test with ESS running.

At least one of the disks involved should be either a system disk (equipments 10 and 11) and/or an ESHAREd disk (equipments 26 and 40.)

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points points should terminate and disappear.

Enter MAG.

X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST2D and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Repeat the channel termination process on the CYBER 825.

Test 2E - Controller power down with connections to 2 CYBERS

Start the Test

If both CYBERs are not already up in a primary/secondary configuration, start this test using the instructions for test 2B, except that the X.BEGT commands must specify test 2E instead of 2B. To verify that the CYBERs are in a primary/secondary configuration, enter E,M. on both the 830

and the 825 and verify that equipments 26 and 40 have an ES in the NOTES column on both consoles. If so, enter X.BEGT(2E,P) to begin testing on the "primary" (830) system, and enter X.BEGT(2E,S) to begin testing on the "secondary" (825) system. Verify the testing as it progresses.

To verify that the testing is proceeding normally, enter AB. on the 830 system console. The B display, should be displaying 2 MST jobs with one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
RANDOM WRITE
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Each of the disk devices that has a DQ type should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Introduce a channel failure

Enter UNLOCK.
ENABLE,ENGR.

Disconnect a cable to induce a "channel interconnect failure."

Enter DISABLE,ENGR. and retry the test with ESS running.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points points should terminate and disappear.

Enter MAG.X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST2E and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Repeat the termination process on the CYBER 825.

6.0 CABINET INTERCONNECT VIA DISKS TESTS

Test 3A - Disk String Failure Test

Start the test

Startup the "primary" system

Deadstart the "primary" CYBER (830) using CMRDECK 24.

Enter E,M.

ON,EQ=26.
NSD,26.
ON,EQ=40.
NSD,40. to bring up equipments 26 and 40 in non-shared mode. Both equipments should have an NS in the NOTES column on the E,M display.

Enter X.BEGT(3A,C) to create files on equipments 26 and 40. Enter UNLOAD,26. When UA appears in the NOTES column, enter ESD,26.

Enter UNLOAD,40. When UA appears in the NOTES column, enter ESD,40. to bring up equipments 26 and 40 in shared mode. Both equipments should have an ES in the NOTES column on the E,M display.

Enter X.BEGT(3A,P) to begin testing on the "primary" system.

Startup the "secondary" system

Deadstart the "secondary" CYBER (830) using CMRDECK 14.

Enter E,M.

ON,EQ=26.
ESD,26.
ON,EQ=40.

ESD,40. to bring up equipments 26 and 40 in shared mode. Both equipments should have an ES in the NOTES column on the E,M display.

Enter X.BEGT(3A,S) to begin testing on the "secondary" system.

Verify the testing as it progresses

To verify that the testing is proceeding normally, enter AB. on the 830 system console. The B display, should be displaying 2 MST jobs with one of the following status messages:

SEQUENTIAL READ
RANDOM WRITE
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Equipments 26 and 40 should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Repeat the checks on the CYBER 825.

Introduce a disk string outage.

Enter UNLOCK.
ENABLE,ENGR.
Do whatever is required to introduce "a disk string outage." Be sure that either the system disks (equipments 10 and 11) and/or the ESHAREd disks (equipments 26 and 40) are involved in the outage.

Enter DISABLE,ENGR. and retry the test with ESS running.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control ~~points~~ points should terminate and disappear.

Enter MAG.

X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST3A and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Repeat the termination process on the CYBER 825.

Test 3B - Controller power down with connections to disks

Start the Test

If both CYBERs are not already up in a primary/secondary configuration, start this test using the instructions for test 3A, except that the X.BEGT commands must specify test 3B instead of 3A. To verify that the CYBERs are in a primary/secondary configuration, enter E,M. on both the 830 and the 825 and verify that equipments 26 and 40 have an ES in the NOTES column on both consoles. If so, enter X.BEGT(3B,P) *(This test is new, so the previous proc used under revision 1 of the test procedure must be shifted to 3C.)* to begin testing on the "primary" (830) system, and enter X.BEGT(3B,S) to begin testing on the "secondary" (825) system. Verify the testing as it progresses.

To verify that the testing is proceeding normally, enter AB. on the 830 system console. The B display, should be displaying 2 MST jobs with one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
RANDOM WRITE
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Each of the disk devices that has a DQ type should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Introduce a powering down of controller

Enter UNLOCK.
ENABLE,ENGR.

Power down controller

Enter DISABLE,ENGR. and retry the test with ESS running.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points points should terminate and disappear.

Enter MAG.

X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST3B and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 3C - System Disk Test

Start the test

Deadstart the CYBER 830 using CMRDECK 25.

Enter X.BEGT(3C) *(This proc was 3B under revision 1 of the procedures.)* from the system console to begin the test.

Verify the testing as it progresses

To verify that the testing is proceeding normally, enter AB. on the system console. The B display, on the right side of the console, should be displaying 4 jobs with one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
SEQUENTIAL POSITIONING
RANDOM READ
RANDOM WRITE
RANDOM POSITIONING
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Equipments 10 and 11 should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG.
X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST3C and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Test 3D - Dual Write for Shared Disk/Multiple Write Test

Start the Test

If both CYBERs are not already up in a primary/secondary configuration, start this test using the instructions for test 3A, except that the X.BEGT commands must specify test 3D instead of 3A. To verify that the CYBERs are in a primary/secondary configuration, enter E,M. on both the 830 and the 825 and verify that equipments 26 and 40 have an ES in the NOTES column on both consoles. If so, enter X.BEGT(3D,P) *(This was proc 3C in revision 1.)* to begin testing on the "primary" (830) system, and enter X.BEGT(3D,S) to begin testing on the "secondary" (825) system. Verify the testing as it progresses.

To verify that the testing is proceeding normally, enter AB. on the 830 system console. The B display, should be displaying 2 MST jobs with one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
RANDOM WRITE
UCMS, 1048.576 KUNS.

Enter E,M. on the system console. Equipments 26 and 40 should have an ON status and should have a count (probably 1 or 2) displayed in the RP column most of the time. If the count field is blank constantly, MST has probably quit using that disk due to an error.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Terminate the Test and Collect Results

Enter DROP,,EX.
MAG.
X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST3D and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

Repeat the termination process on the CYBER 825.

Test 3E - Dual Cabinet Performance Test

Start the test

Deadstart the CYBER 830 using CMRDECK 23.

Enter X.BEGT(3E) *(This was proc 3D in revision 1.)* from the system console to begin the test.

Verify the testing as it progresses

To verify that the testing is proceeding normally, enter AB. on the system console. The B display, on the right side of the console, should be displaying MST jobs. These are recognizable because they will be displaying one of the following status messages:

SEQUENTIAL WRITE
SEQUENTIAL READ
SEQUENTIAL POSITIONING
RANDOM READ
RANDOM WRITE
RANDOM POSITIONING
UCMS, 1048.576 KUNS.

Enter A,ERROR LOG. on the system console. Check for any error messages that refer the any of the DQ type devices.

Enter E,E. on the system console. Check for any error messages.

Enter E,H. on the system console. Check for any values displayed in inverse video. They represent error counts that exceed threshold values.

Wait for an highlighted message indicating that the test is done.

Terminate the Test and Collect Results

Enter DROP,,EX. on the system console. All the jobs at control points should terminate and disappear.

Enter MAG

.X.GETRF. on the system console and mount a scratch tape. When the job requests a tape, enter ASSIGN,jsn,esto., where jsn is the job sequence number of the job requesting the tape and esto is the EST ordinal of the tape drive.

The tape will be labeled TEST3E and will contain copies of the system dayfile, the error log, the binary maintenance log, and an HPA report for the run.

7.0 NOS/BE IN STAND-ALONE MODE TEST

(To be supplied)

FIELD CHANGE ORDER

AUG 17 1993

FCO NUMBER 7000-021

LTR	Description	Date	Approved
A	Release via ECO 5199	1-26-93	MM

TITLE
DIFE Rework

REFERENCE ECO
4178

ASSEMBLY DESCRIPTION
DIFE pc assembly

PART NUMBER
1601716-XXX
1603120-XXX

PRODUCT TYPE / DESCRIPTION
7100-10, 7102-3X and 7100-3X Subsystems

MODEL NUMBER
7100-1X 710X-3X

CLASSIFICATION
_X_ MANDATORY
___ OPTIONAL / RETROFIT ON FAILURE

INSTALLATION TIME
1.0 Hours

PREREQUISITE None

CONCURRENT None

SUPERCEDES None

SPARES AFFECTED
YES _X_ NO __

REASON(s)

1) Prevents "No Drive Clock errors".

Note: See the following items beginning on sheet 2: 1. Effectivity 2. Identifier 3. Materials Required 4.Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9.Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

Document Release	Date
Draftsman Brian Bingham	1/14/93
Checker Donald Eric Cole	1/14/93
Tested & Verified	2-8-93
Engineering	1-14-93
Approved	1-14-93

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AMPERIF CORPORATION

DOCUMENTATION TITLE
FCO 7000-021 Installation Instructions

DRAWING NUMBER 1605328-101

1) Effectivity: 7100-1X serial numbers: 101-110
7102-3X serial numbers: 200-228
7100-3X serial numbers: 200-223

2) Identifier: If the DIFE is not p/n 1601716-952 or higher, this FCO must be installed.
or
If the DIFE is not p/n 1603120-904 or higher, this FCO must be installed.

3) Materials Required: 2) 15K ohm 1/4 watt resistors

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both controllers to be offline when installing this change.

6.2 Place all drives in bypass mode.

6.3 At the disk drive control panel press "Select All".

6.3.1 Place all drives in "Write Protect".

6.3.2 Disable both the "CHA" and "CHB" disk interfaces.

6.4 Open the controller and disk cabinet front doors.

6.5 Power off both controllers by turning off the MAIN AC breaker located in front of the control unit.

7) Installation:

7.1 Remove each DIFE and perform the following rework:

7.1.1 Remove the resistor at R1.

7.1.2 Install the supplied 15K ohm resistor into R1 location.

7.2 Install the new DIFE part number label (supplied with the FCO kit) over the old label; remarking the DIFE as:

DIFE 1601716-952 REV A	or	DIFE 1603120-904 REV A

7.3 Install DIFE(s) back into their original slots.

7.4 Power up the control unit by placing the MAIN AC breaker in the up position.

7.5 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the controllers display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX (where X = drive #) through both controllers.

9.4 Run ILD B's simultaneously from the A and B controllers:

9.4.1 Start ILD B, code 8AA, from the A-side controller. Then run ILD B, code 9AA, from the B-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.4.2 Start ILD B, code 8AA, from the B-side controller. Then run ILD B, code 9AA, from the A-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.5 Place the drives in the appropriate controller drive states (Cache, Bypass, etc.).

9.6 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 21 on the FCO tag.

10.2 Fill out and return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None

12) Parts Disposition: N/A

13) Attachments: None

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FIELD CHANGE ORDER

AUG 17 1993

FCO NUMBER 7000-022

LTR	Description	Date	Approved
A	Release via ECO 5199	1-26-93	MT

TITLE Controller Backplane Rework	**REFERENCE ECO** 4472
ASSEMBLY DESCRIPTION Controller Backplane Assembly	**PART NUMBER** 1602209-501
PRODUCT TYPE / DESCRIPTION 7100-3X Subsystems	**MODEL NUMBER** 7100-3X
CLASSIFICATION _X_ MANDATORY ___ OPTIONAL / RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0 Hours
PREREQUISITE FCO 7000-019	**SPARES AFFECTED** YES _X_ NO __
CONCURRENT None	
SUPERCEDES None	

REASON(s)

1) Change to correct diagnostic test code failures when the subsystem is a single channel controller or a dual channel controller and the HSP pcb is removed.

Note: **See the following items beginning on sheet 2: 1. Effectivity 2. Identifier 3. Materials Required 4.Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9.Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments**

Document Release	Date	CONFIDENTIAL DOCUMENT
Draftsman Brian Bingham	1/14/93	REPRODUCTION/DISCLOSURE IS PROHIBITED WITHOUT PRIOR WRITTEN AUTHORIZATION
Checker [signature]	1/14/93	AMPERIF CORPORATION
Tested & Verified [signature]	2-8-93	**DOCUMENTATION TITLE**
Engineering TK	1-14-93	FCO 7000-022 Installation Instructions
Approved [signature]	1-14-93	**DRAWING NUMBER** 1605329-101

1) Effectivity: 7100-3X serial numbers: 200-228

2) Identifier: If the controller backplane is not p/n 1602209-801 or higher, this FCO must be installed.

Note: This FCO incorporates the necessary changes to the controller backplane for both controllers.

3) Materials Required: 30 guage wire

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both controllers to be offline when installing this change.

6.2 Place all drives in bypass mode.

6.3 At the disk drive control panel press "Select All".

6.3.1 Place all drives in "Write Protect".

6.3.2 Disable both the "CHA" and "CHB" disk interfaces.

6.4 Open the controller and disk cabinet front doors.

6.5 Power off both controllers by turning off the MAIN AC breaker located in front of the control unit.

7) Installation:

7.1 Remove the four (4) receiver/driver paddle boards plugged into the controller logic backplane, locations JJ1A, JJ2A, MJ1A, and MJ2A.

7.2 Add the following two (2) wires to the backplane:

7.2.1 Add 30 gauge jumper, from JJ2A-B1 to JJ2A-B3.

7.2.2 Add 30 gauge jumper, from MJ2A-B1 to MJ2A-B3.

7.3 Installed the new backplane part number label (supplied with the FCO kit) over the old label; remarking the backplane as:

CTRL BKPNL
1602209-801
REV A

7.4 Replace the four (4) receiver/driver paddle boards in the appropriate locations.

7.5 Power up the control unit by placing the MAIN AC breaker in the up position.

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7.6 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the controllers display the message "CHANNEL READY" or "SYSTEM FULLY RECOVERED".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Run ILD B's simultaneously from the A and B controllers:

9.4.1 Start ILD B, code 8AA, from the A-side controller. Then run ILD B, code 9AA, from the B-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.4.2 Start ILD B, code 8AA, from the B-side controller. Then run ILD B, code 9AA, from the A-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.5 Place the drives in the appropriate controller drive states (Cache, Bypass, etc.).

9.6 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 22 on the FCO tag.

10.2 Fill out and return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None

12) Parts Disposition: N/A

13) Attachments: None

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FIELD CHANGE ORDER

AUG 17 1993

FCO NUMBER 7000-023

LTR	Description	Date	Approved
A	Release via ECO 5383	5-7-93	

TITLE
CDCI Board Rework

REFERENCE ECO
5207

ASSEMBLY DESCRIPTION
CDCI pc assembly

PART NUMBER
1603325-403

PRODUCT TYPE / DESCRIPTION
710X-3X Subsystems

MODEL NUMBER
710X-3X

CLASSIFICATION
_X_ MANDATORY
___ OPTIONAL / RETROFIT ON FAILURE

INSTALLATION TIME
1.0 Hours

PREREQUISITE FCO 7000-012 and FCO 7000-016

CONCURRENT FCO 7000-024 (HSP) and FCO 7000-025 (XM16KP-D)

SUPERCEDES None

SPARES AFFECTED
YES _X_ NO __

REASON(s)

1) Allows drives to be accessed after a power up without any operator action at the OCP.

2) Prevents CDCI logic from hanging after power up.

Note: **See the following items beginning on sheet 2: 1. Effectivity 2. Identifier 3. Materials Required 4.Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9.Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments**

Document Release	Date
Draftsman Brian Bingham	3/31/93
Checker TK	3-31-93
Tested & Verified	4-8-93
Engineering J. M. Cornish	4/8/93
Approved	4-7-93

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AMPERIF CORPORATION

DOCUMENTATION TITLE
FCO 7000-023 Installation Instructions

DRAWING NUMBER 1605384-101

1) Effectivity: 7100-3X serial numbers: 200-230

2) Identifier: If each CDCI board is not p/n 1603325-413 or higher, this FCO must be installed.

Note: Each FCO kit upgrades only one CDCI board. You must order one kit for every CDCI board in your subsystem.

3) Materials Required:
1 33 ohm 1/4 watt resistor ..... p/n 20198716-330
1 10 ohm 1/4 watt resistor ..... p/n 20185016-001

4) Special Tools Required: Soldering Iron - 25-30 watt, 750-800 degrees Fahrenheit
Static safeguard equipment and workstation

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both controllers to be offline when installing this change.

6.2 Place all drives in bypass mode.

6.3 At the disk drive control panel press "Select All".

6.3.1 Place all drives in "Write Protect".

6.3.2 Disable both the "CHA" and "CHB" disk interfaces.

6.4 Open the controller and disk cabinet front doors.

6.5 Power off both controllers by turning off the MAIN AC breaker located in front of the control unit.

7) Installation:

7.1 Carefully remove a CDCI board and perform the following rework:

7.1.1 Carefully unsolder and remove the resistors from locations R9 and R202.

7.1.2 Install and solder in place the 33 ohm resistor (p/n 20198716-330) into location R9.

7.1.3 Install and solder in place the 10 ohm resistor (p/n 20185016-001) into location R202.

7.2 Install the new part number label (supplied with the FCO kit) over the old label; remarking the CDCI board as:

CDCI
1603325-413
REV A

7.3 Install the reworked CDCI board into its original location.

7.4 Power up the control unit by placing the MAIN AC breaker in the up position.

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8) Verification Instructions:

8.1 At the OCP panel, wait approximately 70 seconds and verify that the controllers display the message "CHANNEL READY CODE = 000".

8.2 Verify that both "CHA" and "CHB" disk interfaces are enabled and that the drives are not write protected.

9) Operational Checkout:

9.1 Run ILD B code 2EX through both controllers.

9.2 Reset both controllers and run ILD B's simultaneously from the A and B controllers:

9.2.1 Start ILD B, code 8AA, from the A-side controller. Then run ILD B, code 9AA, from the B-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.2.2 Start ILD B, code 8AA, from the B-side controller. Then run ILD B, code 9AA, from the A-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.3 At the disk drive control panel press "Select All".

9.3.1 Place all drives in "Write Protect".

9.3.2 Disable both the "CHA" and "CHB" disk interfaces.

9.4 Cycle the MAIN AC breaker off, wait 30 seconds, then power back on. Do Not reset controllers.

9.5 Perform step 8 - Verification Instructions.

9.6 At the host, up any downed channels and/or drives and execute an MST through the channel that the reworked CDCI board is connected to. Verify that the drives can be accessed without any operator action at the OCP.

9.7 Replace all doors and covers removed during this installation.

9.8 Return the drives to their original drive state (Cache, Bypass, etc.)

9.9 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 23 on the FCO tag.

10.2 Fill out and return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None

12) Parts Disposition: Scrap

13) Attachments: None

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FIELD CHANGE ORDER

AUG 17 1993

FCO NUMBER 7000-024

LTR	Description	Date	Approved
A	Release via ECO 5383	5-7-93	M Hamm

TITLE HSP Board Microcode Update	**REFERENCE ECO** 5207
ASSEMBLY DESCRIPTION HSP pc assembly	**PART NUMBER** 1602911-701
PRODUCT TYPE / DESCRIPTION 710X-3X Subsystems	**MODEL NUMBER** 710X-3X
CLASSIFICATION _X_ MANDATORY ___ OPTIONAL / RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0 Hours
PREREQUISITE FCO 7000-018	**SPARES AFFECTED** YES _X_ NO __
CONCURRENT FCO 7000-023 (CDCI) and FCO 7000-025 (XM16KP-D)	
SUPERCEDES None	

REASON(s)

1) Allows drives to be accessed after a power up without any operator action at the OCP.

2) Prevents CDCI logic from hanging after power up.

Note: **See the following items beginning on sheet 2: 1. Effectivity 2. Identifier 3. Materials Required 4.Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9.Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments**

Document Release	Date	
Draftsman Brian Bing	3/31/93	CONFIDENTIAL DOCUMENT REPRODUCTION/DISCLOSURE IS PROHIBITED WITHOUT PRIOR WRITTEN AUTHORIZATION
Checker TK	3-31-93	AMPERIF CORPORATION
sted & Verified	4-8-93	**DOCUMENTATION TITLE**
Engineering M. Cyril	4/8/93	FCO 7000-024 Installation Instructions
Approved	4/9/93	**DRAWING NUMBER** 1605385-101 — Sheet 1 of 3

1) Effectivity: 7100-3X serial numbers: 200-230

2) Identifier: If both HSP boards are not p/n 1602911-711 or higher, this FCO must be installed.

Note: Each FCO kit upgrades only one HSP board. You must order two FCO kits for each subsystem.

3) Materials Required:

1 PROM (U105)	p/n 1605344-002
1 PROM (U106)	p/n 1605344-003
1 PROM (U107)	p/n 1605344-004
1 PROM (U108)	p/n 1605344-001

4) Special Tools Required: Static safeguard equipment and workstation

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both controllers to be offline when installing this change.

6.2 Place all drives in bypass mode.

6.3 At the disk drive control panel press "Select All".

6.3.1 Place all drives in "Write Protect".

6.3.2 Disable both the "CHA" and "CHB" disk interfaces.

6.4 Open the controller and disk cabinet front doors.

6.5 Power off both controllers by turning off the MAIN AC breaker located in front of the control unit.

7) Installation:

7.1 Remove a HSP board and perform the following rework:

7.1.1 Carefully remove the old PROMS from locations U105, U106, U107 and U108.

7.1.2 Install the supplied PROMS into locations U105 (1605344-002), U106 (1605344-003), U107 (1605344-004) and U108 (1605344-001).

7.2 Install the new part number label (supplied with the FCO kit) over the old label; remarking the HSP board as:

HSP
1602911-711
REV A

7.3 Install the reworked HSP board into its original slot.

7.4 Power up the control unit by placing the MAIN AC breaker in the up position.

8) Verification Instructions:

8.1 At the OCP panel, wait approximately 70 seconds and verify that the controllers display the message "CHANNEL READY CODE = 000".

8.2 Verify that both "CHA" and "CHB" disk interfaces are enabled and that the drives are not write protected.

9) Operational Checkout:

9.1 Run ILD B code 2EX through both controllers.

9.2 Reset both controllers and run ILD B's simultaneously from the A and B controllers:

9.2.1 Start ILD B, code 8AA, from the A-side controller. Then run ILD B, code 9AA, from the B-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.2.2 Start ILD B, code 8AA, from the B-side controller. Then run ILD B, code 9AA, from the A-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.3 At the disk drive control panel press "Select All".

9.3.1 Place all drives in "Write Protect".

9.3.2 Disable both the "CHA" and "CHB" disk interfaces.

9.4 Cycle the MAIN AC breaker off, wait 30 seconds, then power back on. Do Not reset controllers.

9.5 Perform step 8 - Verification Instructions.

9.6 At the host, up any downed channels and/or drives and execute an MST to verify that the drives can be accessed without any operator action at the OCP.

9.7 Replace all doors and covers removed during this installation.

9.8 Return the drives to their original drive state (Cache, Bypass, etc.)

9.9 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 24 on the FCO tag.

10.2 Fill out and return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None

12) Parts Disposition: Scrap

13) Attachments: None

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FIELD CHANGE ORDER

AUG 17 1993

FCO NUMBER 7000-025

LTR	Description	Date	Approved
A	Release via ECO 5383	5-7-93	

TITLE XM16KP-D Microcode Update	**REFERENCE ECO** 5207
ASSEMBLY DESCRIPTION XM16KP-D pc assembly	**PART NUMBER** 1601495-231
PRODUCT TYPE / DESCRIPTION 710X-3X Subsystems	**MODEL NUMBER** 710X-3X
CLASSIFICATION _X_ MANDATORY ___ OPTIONAL / RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0 Hours
PREREQUISITE FCO 7000-013	**SPARES AFFECTED** YES _X_ NO __
CONCURRENT FCO 7000-023 (CDCI) and FCO 7000-024 (HSP)	
SUPERCEDES None	

REASON(s)

1) Allows drives to be accessed after a power up without any operator action at the OCP.

2) Prevents CDCI logic from hanging after power up.

Note: **See the following items beginning on sheet 2: 1. Effectivity 2. Identifier 3. Materials Required 4.Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9.Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments**

Document Release	Date
Draftsman Brian Bingham	3/31/93
Checker TK	3-31-93
ed & Verified	4-8-93
Engineering J. McGinnis	4/8/93
Approved	4/9/93

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AMPERIF CORPORATION

DOCUMENTATION TITLE

FCO 7000-025 Installation Instructions

DRAWING NUMBER 1605386-101

1) Effectivity: 7100-3X serial numbers: 200-230

2) Identifier: If both XM16KP-D boards are not p/n 1601495-241 or higher, this FCO must be installed.

Note: Each FCO kit upgrades only one XM16KP-D board. You must order two FCO kits for each subsystem.

3) Materials Required: 1 PROM (U3) ..... p/n 1603542-211

4) Special Tools Required: Static safeguard equipment and workstation

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both controllers to be offline when installing this change.

6.2 Place all drives in bypass mode.

6.3 At the disk drive control panel press "Select All".

6.3.1 Place all drives in "Write Protect".

6.3.2 Disable both the "CHA" and "CHB" disk interfaces.

6.4 Open the controller and disk cabinet front doors.

6.5 Power off both controllers by turning off the MAIN AC breaker located in front of the control unit.

7) Installation:

7.1 Remove an XM16KP-D board and perform the following rework:

7.1.1 Carefully remove the old PROM from location U3.

7.1.2 Install the supplied PROM into location U3.

7.2 Install the new part number labels (supplied with the FCO kit) over the old labels; remarking the XM16KP-D board as:

XM16KP-D
1601495-241
REV A

7.3 Install the reworked XM16KP-D board into its original location.

7.4 Power up the control unit by placing the MAIN AC breaker in the up position.

8) Verification Instructions:

8.1 At the OCP panel, wait approximately 70 seconds and verify that the controllers display the message "CHANNEL READY CODE = 000".

8.2 Verify that both "CHA" and "CHB" disk interfaces are enabled and that the drives are not write protected.

9) Operational Checkout:

9.1 Run ILD B code 2EX through both controllers.

9.2 Reset both controllers and run ILD B's simultaneously from the A and B controllers:

9.2.1 Start ILD B, code 8AA, from the A-side controller. Then run ILD B, code 9AA, from the B-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.2.2 Start ILD B, code 8AA, from the B-side controller. Then run ILD B, code 9AA, from the A-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.3 At the disk drive control panel press "Select All".

9.3.1 Place all drives in "Write Protect".

9.3.2 Disable both the "CHA" and "CHB" disk interfaces.

9.4 Cycle the MAIN AC breaker off, wait 30 seconds, then power back on. Do Not reset controllers.

9.5 Perform step 8 - Verification Instructions.

9.6 At the host, up any downed channels and/or drives and execute an MST to verify that the drives can be accessed without any operator action at the OCP.

9.7 Replace all doors and covers removed during this installation.

9.8 Return the drives to their original drive state (Cache, Bypass, etc.)

9.9 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 25 on the FCO tag.

10.2 Fill out and return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None

12) Parts Disposition: Scrap

13) Attachments: None

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REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3703	12/7/90	MM
	Changes to pages 2 - 5 , PER ECO 3720	12-20-90	MM

TITLE CDCI Board Replacement	REFERENCE ECO 3671
ASSEMBLY DESCRIPTION CDCI BOARDS	PART NUMBER 1603325-303
PRODUCT TYPE/DESCRIPTION 7100-3X Subsystems	MODEL NUMBER 7100-3X
CLASSIFICATION XX MANDATORY ____ OPTIONAL/RETROFIT ON FAILURE	INSTALLATION TIME 1.0
PREREQUISITE NONE	SPARES AFFECTED YES X
CONCURRENT NONE	NO ____
SUPERCEDES FCO 7000-009	

REASON(s)

1) To correct channel timing problems.
2) To correct signal level problems.

MAR - 5 1991

Note: See sheet 3 for the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING TK	12-19-90
DRAFTSMAN	12-19-90
CKER	
OTHER	
APPROVED	12/19/90

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FCO 7000-012 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603556-101	1 OF 5

1) Effectivity: 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

CDCI board is not PN 1603325-303

3) Materials Required:

2 per subsystem CDCI PN 1603325-303

4) Special Tools Required: None

5) Test Equipment:

1 Dual trace oscilloscope (60 MHZ or better).
2 Jumper leads for clipping onto chip legs.

6) Preparation:

6.1 Both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front door.

7) Installation:

7.1 Power off both control units by turning off the main AC circuit breaker located at the front of the control unit.

7.2 Remove old CDCI boards and replace with new CDCI boards.

CAUTION: Verify terminators (Ports A0 and B0 only) and SW1 settings (port numbers) and SW2 settings (channel timing) as per this document.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

SW1 SETTINGS (After FCO 7000-014)

1	2	3	4	5	6	7	8	BRD #
0	0	0	1	1	0	1	*	0
0	0	1	0	1	0	1	*	1
0	1	0	0	1	0	1	*	2
1	0	0	0	1	0	1	*	3
PORT NUMBERS				A or B CONTROLLER				CDCI

NOTE: 0 equals ON
1 equals OFF

* This bit is used to determine A or B controller. If this position is a 0 (switch on) it denotes an A controller connection. If this position is a 1 (switch off) it denotes a B controller connection. All CDCI boards connected must indicate the controller connection (after FCO 7000-014).

SW1 SETTINGS (Before FCO 7000-014)

1	2	3	4	5	6	7	8	BRD #
1	0	0	1	0	0	0	**	0
1	0	1	0	1	0	1	0	1
1	0	1	1	1	0	1	1	2
1	1	0	0	1	1	0	0	3
PORT NUMBERS								CDCI

NOTE: 0 equals ON
1 equals OFF

** This bit is used to determine A or B controller. If this position is a 0 (switch on) it denotes an A controller connection (only 1 board per controller will define this). If this position is a 1 (switch off) it denotes a B controller connection (only 1 board per controller will define this).

7.3 Power up the control unit by placing the main "AC" breaker in the up position.

7.4 At the disk drive control panel press "Select All". Disable both the "CHA" and "CHB" disk interfaces and enable "Write Protect".

7.5 CDCI adjustment.

7.5.1 On the CDCI board jumper U42-6 to U42-7 and U71-1 to U71-11

7.5.2 At the CDC Cyber computer processor backplane;

On the cable labeled "A" put channel one of the scope on the 10MHZ signal. Put channel two of the scope on the Full signal. Put the ground leads on the opposite pin for each scope probe.

7.5.3 On the CDCI board, switch 2, positions 1 & 2 represents a hex character. Positions 3, 4, 5 & 6 represents the lower hex character. A count between 14 (hex) and 1C (hex) is expected for most mainframes. A good starting value is 18 (hex) for Cyber 65830 and Cyber 960 mainframes. Switch 2, position 7 and 8 must be off.

7.5.4 Adjust SW2 positions 1-6 so that the Full signal is active 10 to 15NS after the 10MHZ signal. Use the positive leading edge at the 50% level for measurements.

7.5.5 Signal diagram: See Attachment A

7.5.6 Remove the jumpers on U42 and U71.

7.5.7 This adjustment must be done for every port on each channel used.

7.5.8 Reset the controller when done with the above adjustments for all CDCI boards.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY" or "CHANNEL READY CODE=000" (FCO 7000-014).

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect". Enable channel "A" and channel "B" ports.

9.2 Replace all doors and covers removed during this installation. The system is now ready for use.

9.3 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 12 on the 7100-3X FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

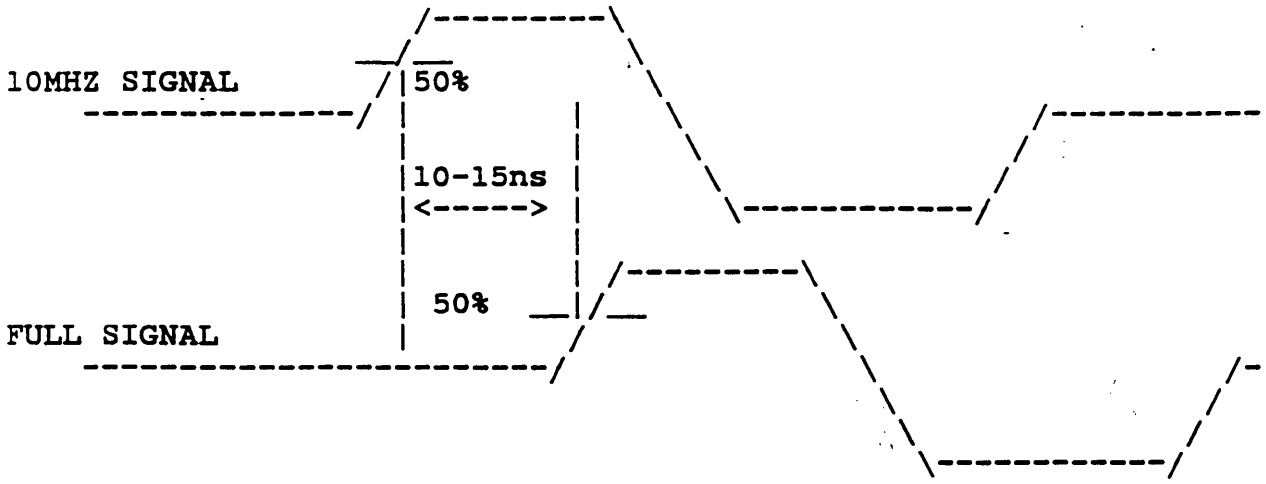
11) Documentation Updates: This information incorporated in future revision.

12) Parts Disposition:

Return parts to: EMPROS Systems International
2300 Berkshire Lane N.
Plymouth, MN 55441
ATTN: Mr. D.L. Dawkins

13) Attachments: A) Signal Diagram

Attachment A



USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV.
FCO 7000-012 Installation Instructions	B
DRAWING NO. 1603556-101	SHEET 5 OF 5

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3685		
B	Correction to cover page - ECO		

TITLE	REFERENCE ECO
XM16KPD Microcode Replacement	3685
ASSEMBLY DESCRIPTION	**PART NUMBER**
XM16KPD - Microcode	1601495-161 or -171
PRODUCT TYPE/DESCRIPTION	**MODEL NUMBER**
7100-3X Subsystems	7100-3X
CLASSIFICATION	**INSTALLATION TIME**
XX MANDATORY	1.0
___ OPTIONAL/RETROFIT ON FAILURE	
PREREQUISITE NONE	**SPARES AFFECTED**
CONCURRENT FCO 7000-014 and FCO 7000-015	YES X
SUPERCEDES NONE	NO ___

REASON(s)

1) Adds assembly flag for disabling cacheing, this reduces code down to fit in 1 prom.

2) This code increases U-bus timeout.

3) This code adds a few messages for ILD-B offline diagnostics.

4) This code fixes STR 65, a problem with HSSM resets during channel truncation.

Note: See sheet 3 for the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING	12-13-90
DRAFTSMAN	12/13/90
CHECKER	
OTHER	
APPROVED	12/13/90

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FCO 7000-013 Installation Instructions

SIZE	DRAWING NO.		SHEET
A	1603568-101	REV A	1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

1) **Effectivity:** 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

XM16KPD is not PN 1601495-~~211~~ 231 BRB REV A

3) Materials Required:

PROM PN 1603542-~~101~~ 201 BRB REV A

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front door and remove the controller cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove the XM16KPD in both controllers.

7.3 Remove the cover on both XM16KPD's.

7.4 Remove proms from locations U3 and U4.

7.5 Install PN 1603542-~~101~~ 201 BRB REV A at location U3 (U4 will remain empty).

7.6 Replace the cover on both XM16KPD's and label as PN 1601495-~~211~~ 231 BRB REV A.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

7.7 Replace the XM16KPD in both controllers.

7.8 Power up the control unit by placing the main "AC" breaker in the up position.

7.9 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Monitor the system for logged errors.

10) Installation Reporting: 1, 7 and

10.1 Mark an "X" through 13 on the 7100-30 FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: EMPROS Systems International
2300 Berkshire Lane N.
Plymouth, MN 55441
ATTN: Mr. D. L. Dawkins

13) Attachments: None.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3685 Corrections to cover and sheet 3 - ECO 3913		

TITLE HSP Board	**REFERENCE ECO** 3685
ASSEMBLY DESCRIPTION HSP BOARD	**PART NUMBER** 1602911-201 or -401
PRODUCT TYPE/DESCRIPTION 7100-3X Subsystems	**MODEL NUMBER** 7100-3X
CLASSIFICATION XX MANDATORY OPTIONAL/RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0
PREREQUISITE FCO 7000-012 and FCO 7100-016	**SPARES AFFECTED** YES X NO
CONCURRENT FCO 7000-013 and FCO 7000-015	
SUPERCEDES NONE	

REASON(s)

1) Enables toggle 07 (on power up) and manual reset of HSP board.

2) Adds logic for shared memory.

3) This release of HSP code corrects multiple product bugs.

Note: See sheet 3 for the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING	1-14-91
DRAFTSMAN	1-14-91
CHECKER	
OTHER	
APPROVED	1/14/91

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FCO 7000-014 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603569-101	1 OF 3

1) Effectivity: 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

HSP Board is not PN 1602911-501 REV A

3) Materials Required:

HSP PN 1602911-501 REV A

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open and remove the front and back doors and remove the controller cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove and replace the HSP boards located in the controller.

7.3 Power up the control unit by placing the main "AC" breaker in the up position.

7.4 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 14 on the 7100-30 FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: Empros Systems International
2300 Berksire Lane N.
Plymouth, MN 55441
ATTN: Mr. D. L. Dawkins

13) Attachments: None.

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3744 Corrections to cover and sheet 2, step 2 - ECO 3919	1-18-91	M Mooney

TITLE CDCI Board	**REFERENCE ECO** 3729
ASSEMBLY DESCRIPTION CDCI Board	**PART NUMBER** 1603325-303
PRODUCT TYPE/DESCRIPTION 7100-3X Subsystems	**MODEL NUMBER** 7100-3X
CLASSIFICATION __X__ MANDATORY _____ OPTIONAL/RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0 hours
PREREQUISITE	**SPARES AFFECTED** YES__X__
CONCURRENT FCO 7000-012	NO_____
SUPERCEDES	

REASON(s)

Corrects for wrong resistor SIP on new CDCI board

Note:
This copy is for your records only. The CDCI boards supplied 5/20/92 have this change installed.

Brian B

Note: See sheet 3 for the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING	1-17-91
DRAFTSMAN	1-17-91
CHECKER	
OTHER	
APPROVED	1/17/91

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FCO 7000-016 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603591-101	1 OF 3

1) Effectivity: 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

The resistor SIP at location RN2 on the CDCI PCB is 100 ohms. The 100 ohm resistor is identified with the markings 10X-1-101.

3) Materials Required:

Resistor SIP 330/390 ohm (part # 20101100)

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open and remove the front and back doors and remove the controller cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Inspect all CDCI boards for the presence of 100 ohm resistor SIP at location RN2 (between U10 & U11). Remove and discard all 100 ohm SIP's.

7.3 In the last board of a CDCI board string, install the 330/390 ohm resistor SIP, supplied with this FCO, at location RN2. Normally a resistor would be installed on the boards at location A0 and B0. Insure that all other boards have RN2 removed.

7.4 Place the supplied part number label (p/n 1603325-403) over the existing part number label on all CDCI boards (even if they do not have the 330/390 SIP).

7.5 Power up the control unit by placing the main "AC" breaker in the up position.

7.6 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY" or "SYSTEM FULLY RECOVERED".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 16 on the 7100-30 FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None

12) Parts Disposition: None

13) Attachments: None

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3843	3-22-91	

TITLE EXXP SIP Socket Removal	**REFERENCE ECO** 3324
ASSEMBLY DESCRIPTION EXXP Boards	**PART NUMBER** 1601909-101
PRODUCT TYPE/DESCRIPTION 710X-XX Subsystems	**MODEL NUMBER** 7100-3X
CLASSIFICATION __XX__ MANDATORY ____OPTIONAL/RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0
PREREQUISITE None	**SPARES AFFECTED** YES XX NO__
CONCURRENT None	
SUPERCEDES None	

REASON(s)

1) Improper SIP socket causing intermittent contact.

2) Causes intermittent Datachecks (43's) to random drives, random locations.

Note: See the following sheets for: 1. Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING Tony Ribrein	3-7-91
DRAFTSMAN	3/7/91
CHECKER	
OTHER	
APPROVED Brian Bond	3/7/91

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FCO 7000-017 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603623-101	1 OF 3

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9253

1) Effectivity:

7100-1X serial numbers:	101-103, 106-110
7102-3X serial numbers:	111-112
7100-3X serial numbers:	200-223

2) Identifier:

This FCO has not been installed if:

EXXP boards are PN 1601909-101.

3) Materials Required:

2 - EXXP boards PN 1601909-201

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front and back doors and remove the EXXP cardcage cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove and replace the EXXP pcbas located in the EXXP card cage with those supplied in the FCO kit.

7.3 Power up the control unit by placing the main "AC" breaker in the up position.

7.4 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD 2 to several drives from both controllers for at least 50 cylinders.

9.4 Run ILD B code 2EX through both controllers.

9.5 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 17 on the 710X-XX FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: Empros Systems International
2300 Berkshire Lane N.
Plymouth, MN 55441
Attn: D. L. Dawkins

13) Attachments: None.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
	Released via ECO 3844		

TITLE HSP Board to -601	**REFERENCE ECO** 3762
ASSEMBLY DESCRIPTION HSP BOARD	**PART NUMBER** 1602911-501 REV A
PRODUCT TYPE/DESCRIPTION 7100-1X*, 7102-3X*, & 7100-3X Subsystems	**MODEL NUMBER** 7100-1X 710X-3X
CLASSIFICATION _XX_ **MANDATORY** ___ **OPTIONAL/RETROFIT ON FAILURE**	**INSTALLATION TIME** 1.0
PREREQUISITE None	**SPARES AFFECTED** **YES** XX **NO** ___
CONCURRENT * FCO 7000-020 (SNs below 200)	
SUPERCEDES FCO 7000-014	

REASON(s)

1) New firmware release.

2) Power Up/Down Module Corrections.

3) During power down of one controller, shared memory gets a parity error.

Note: See sheet 2 for the following items: 1. Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING Tony Kilwein	3-18-91
DRAFTSMAN Dan Mena	3/18/91
CHECKER	
OTHER	
APPROVED B. Bray	3/18/91

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FCO 7000-018 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603624-101	1 OF 4

BISHOP GRAPHICS/ACCUPRESS

1) Effectivity:

7100-1X serial numbers:	101-110
7102-3X serial numbers:	111-112
7100-3X serial numbers:	200-223

2) Identifier:

This FCO has not been installed if:

HSP Boards are not PN 1602911-601 REV A or higher.

3) Materials Required:

2 - HSP PN 1602911-601 REV A

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front and back doors and remove the controller cardcage cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove and replace the HSP boards located in the controller.

7.3 Check and reset (if necessary) all CDCI board switch settings per the following chart:

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

SW1 SETTINGS (After FCO 7000-018)

1	2	3	4	5	6	7	8	BRD #
0	0	0	1	1	0	1	*	0
0	0	1	0	1	0	1	*	1
0	1	0	0	1	0	1	*	2
1	0	0	0	1	0	1	*	3
PORT NUMBERS				A or B CONTROLLER				CDCI

NOTE: 0 equals ON
1 equals OFF

* This bit is used to determine A or B controller. If this position is a 0 (switch on) it denotes an A controller connection. If this position is a 1 (switch off) it denotes a B controller connection. All CDCI boards connected must indicate the controller connection (after FCO 7000-018).

7.4 Power up the control unit by placing the main "AC" breaker in the up position.

7.5 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Run ILD B's simultaneously from the A and B controllers:

9.4.1 Start ILD B, code 8AA from the A-side controller. Then run ILD B code 9AA from the B-side controller. Allow the test to run two minutes then stop the tests by pressing the RESET button.

9.4.2 Start ILD B, code 8AA from the B-side controller. Then run ILD B code 9AA from the A-side controller. Allow the test to run two minutes then stop the tests by pressing the RESET button.

9.5 Monitor the system for logged errors.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

10) Installation Reporting:

10.1 Because this FCO supersedes FCO's 8 and 14, mark an "X" through 8 and 14 of the FCO label if not previously marked.

10.2 Mark an "X" through 18 on the 7100-30 FCO tag.

10.3 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: Empros Systems International
2300 Berksire Lane N.
Plymouth, MN 55441
ATTN: Mr. D. L. Dawkins

13) Attachments: None.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3854		

TITLE Isolated or Frame Ground Connection	**REFERENCE ECO** 3561/3416
ASSEMBLY DESCRIPTION Frame Assembly	**PART NUMBER** 1603027-101/102
PRODUCT TYPE/DESCRIPTION 7100-3X Subsystems	**MODEL NUMBER** 7100-3X
CLASSIFICATION XX MANDATORY ____ OPTIONAL/RETROFIT ON FAILURE	**INSTALLATION TIME** 0.5 Hour
PREREQUISITE NONE	**SPARES AFFECTED**
CONCURRENT NONE	YES___
SUPERCEDES NONE	NO XX

REASON(s)

1) Add lug for "Isolated ground connection system".

2) To correct manufacturing.

Done
4-24-91
JT&MAE

Note: Additional sheets include the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING J Kilwein	3-5-91
DRAFTSMAN M Maude	2/25/91
CHECKER	
OTHER	
APPROVED B Bass	3/5/91

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FCO 7000-011 Installation Instructions

SIZE	DRAWING NO.	SHEET 1 OF 6
A	1603647-101	

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-8253

1) Effectivity: 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

The ground lug is missing on BB2-12 and/or on the I/O Housing (See Attachment A,B and C)

3) Materials Required: 1/4 - 20 x 3/4 bolt PN 20119613-611
Lock Washer PN 20122113-006
Flat Washer PN 20122013-006
Ground Cable PN 1603300-101

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the back door and the power supply panel.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Locate and Remove ground wire W87 (see attachment A) and replace with the ground wire provided in the kit.

7.3 Verify the following;

7.3.1 2 lugs installed on ground bus BB1 - 20 (See Attachment A)

7.3.2 Ground wire W87 from BB2 - 11 or BB2 - 12 to Frame (See Attachment A)

7.4 If wire W87 is not connected to BB2 - 11 move the connection to BB2 - 11 (See Attachment A).

7.5 Remove the screw, associated hardware and 2 lugs connected to BB1 - 20 (See Attachment A).

7.6 Using the screw and associated hardware from step 7.4 connect 1 lug to BB2 - 12 (See Attachment B).

7.7 Using the bolt and associated hardware that came with the FCO connect 1 lug to I/O Housing (See Attachment C). If this lug is already present discard the bolt and associated hardware that came with the FCO.

7.8 The 7100-3X is designed to accommodate either a frame ground connection system or an isolated ground connection system. Review host system requirements to determine which system is suitable for your site. See Attachment C for frame ground connections or Attachment B for isolated ground connections. Late model mainframes use frame ground and is the expected configuration for most sites.

7.9 Power up the control unit by placing the main "AC" breaker in the up position.

7.10 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY" or "CHANNEL READY CODE=000" (FCO 7000-014).

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Monitor the system for logged errors.

10) Installation Reporting:

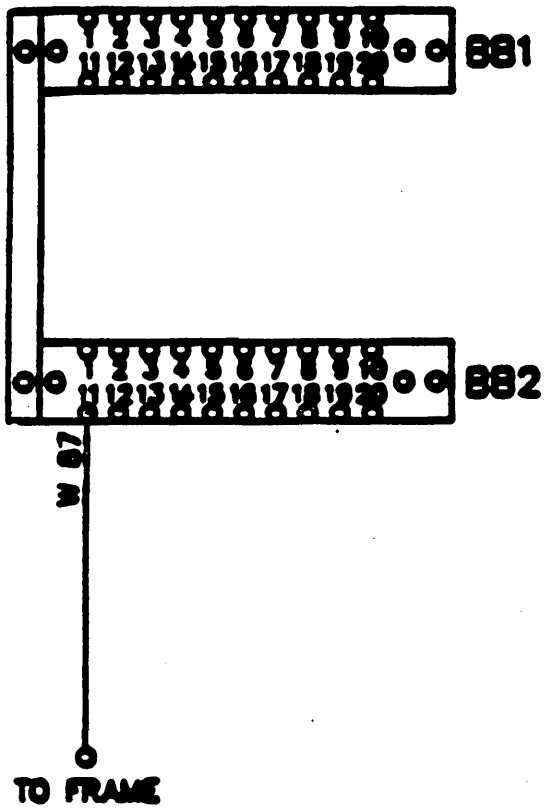
10.1 Mark an "X" through 10 and 11 on the 7100-3X FCO tag. FCO 10 was not used and is being marked out to avoid future requests for FCO 10.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: This information will be incorporated in future release.

12) Parts Disposition: None.

13) Attachments: A) Ground Bus BB1 and BB2.
B) Isolated ground connection system
C) Frame ground connection system



Attachment A

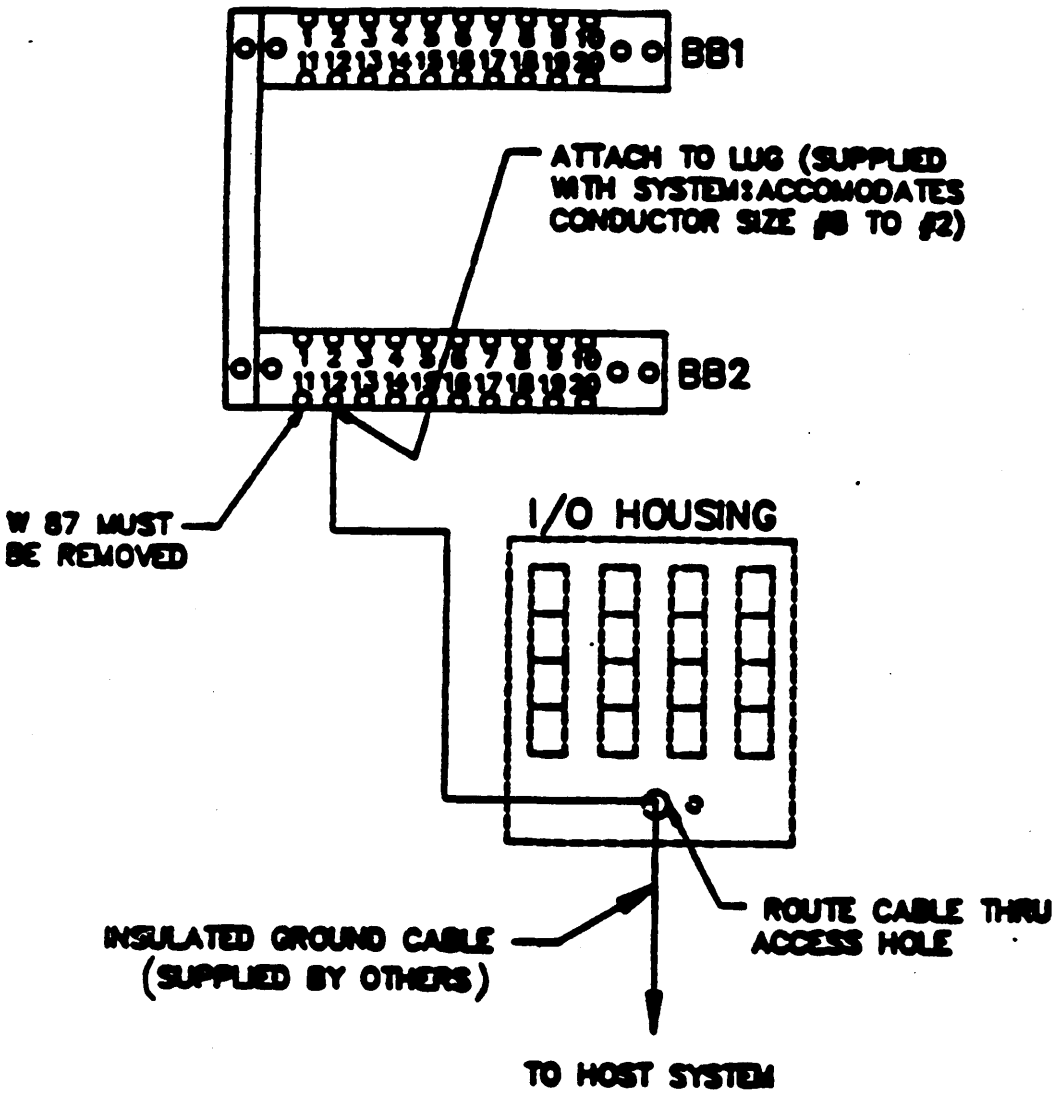

BB1
ATTACH TO LUG (SUPPLIED WITH SYSTEM: ACCOMODATES CONDUCTOR SIZE #8 TO #2)
BB2
W 87 MUST BE REMOVED
I/O HOUSING
INSULATED GROUND CABLE (SUPPLIED BY OTHERS)
ROUTE CABLE THRU ACCESS HOLE
TO HOST SYSTEM

Figure 12-6
System Grounding Detail: Isolated Ground Connection System

Attachment B

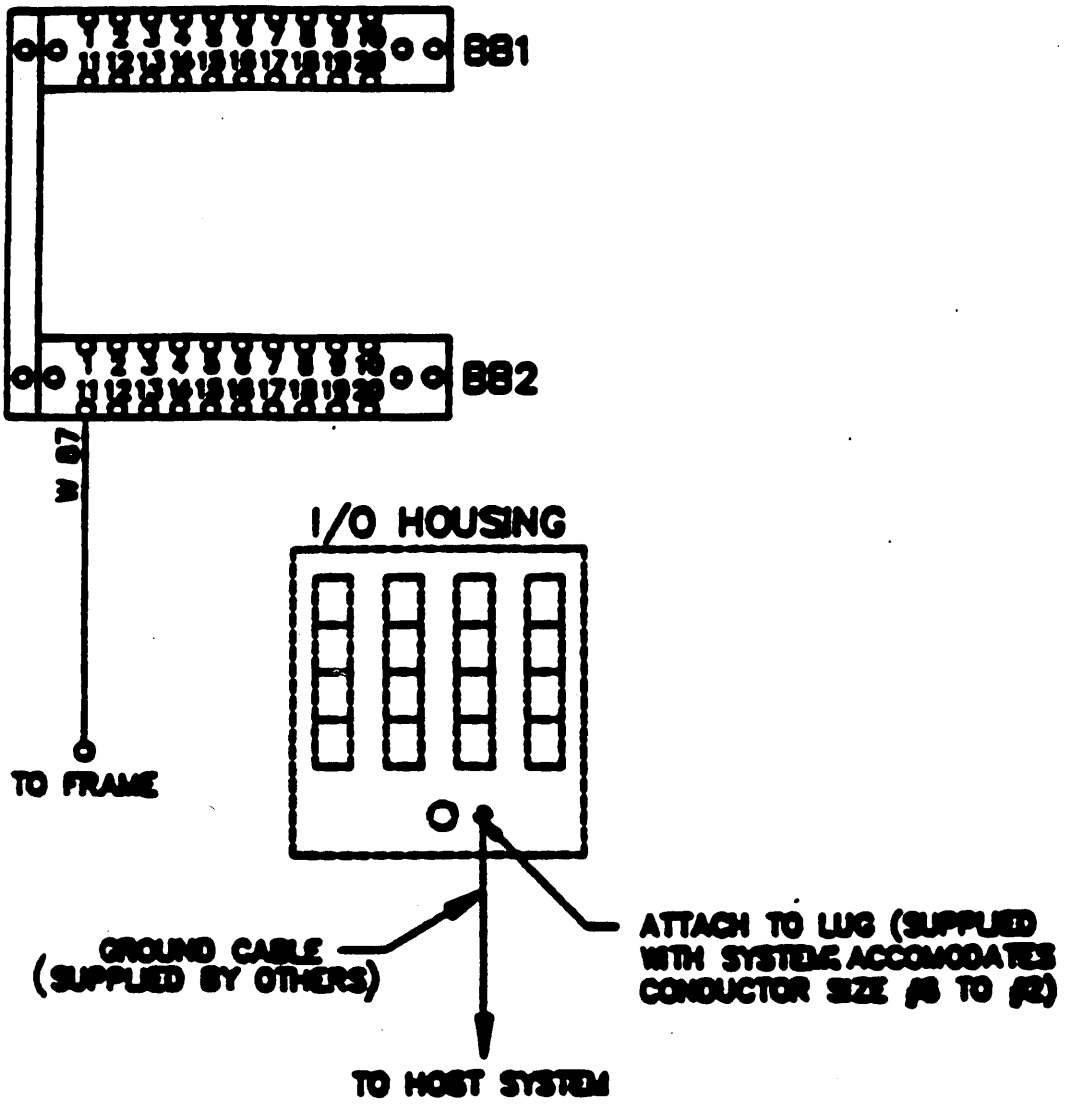


Figure 12-4
System Grounding Detail: Frame Ground Connection System

Attachment C

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	- Released via ECO 3703	12/7/90	MMacy
B	Changes to pages 2 - 5 , PER ECO 3720	12-20-90	MMacy
C	Corrections to cover and sheet 4 - ECO 3913		

TITLE CDCI Board Replacement	REFERENCE ECO 3671
ASSEMBLY DESCRIPTION CDCI BOARDS	PART NUMBER 1602912-XXX
PRODUCT TYPE/DESCRIPTION 7100-3X Subsystems	MODEL NUMBER 7100-3X
CLASSIFICATION XX MANDATORY ____ OPTIONAL/RETROFIT ON FAILURE	INSTALLATION TIME 1.0
PREREQUISITE NONE	SPARES AFFECTED YES X
CONCURRENT NONE	NO____
SUPERCEDES FCO 7000-009	

REASON(s)

Done 4/18/91 MAC & JT

1) To correct channel timing problems.
2) To correct signal level problems.

Note: See sheet 3 for the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING TR	12-19-90
DRAFTSMAN	12-19-90
CHECKER	
OTHER	
APPROVED BB	12/19/90

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FCO 7000-012 Installation Instructions

SIZE	DRAWING NO.		SHEET
A	1603556-101	REV C	1 OF 5

1) Effectivity: 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

CDCI board is not PN 1603325-303

3) Materials Required:

2 per subsystem CDCI PN 1603325-303

4) Special Tools Required: None

5) Test Equipment:

1 Dual trace oscilloscope (60 MHZ or better).
2 Jumper leads for clipping onto chip legs.

6) Preparation:

6.1 Both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front door.

7) Installation:

7.1 Power off both control units by turning off the main AC circuit breaker located at the front of the control unit.

7.2 Remove old CDCI boards and replace with new CDCI boards.

CAUTION: Verify terminators (Ports A0 and B0 only) and SW1 settings (port numbers) and SW2 settings (channel timing) as per this document.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

SW1 SETTINGS (After FCO 7000-014)

1	2	3	4	5	6	7	8	BRD #
0	0	0	1	1	0	1	*	0
0	0	1	0	1	0	1	*	1
0	1	0	0	1	0	1	*	2
1	0	0	0	1	0	1	*	3
PORT NUMBERS				A or B CONTROLLER				CDCI

NOTE: 0 equals ON
1 equals OFF

* This bit is used to determine A or B controller. If this position is a 0 (switch on) it denotes an A controller connection. If this position is a 1 (switch off) it denotes a B controller connection. All CDCI boards connected must indicate the controller connection (after FCO 7000-014).

SW1 SETTINGS (Before FCO 7000-014)

1	2	3	4	5	6	7	8	BRD #
1	0	0	1	0	0	0	**	0
1	0	1	0	1	0	1	0	1
1	0	1	1	1	0	1	1	2
1	1	0	0	1	1	0	0	3
PORT NUMBERS								CDCI

NOTE: 0 equals ON
1 equals OFF

** This bit is used to determine A or B controller. If this position is a 0 (switch on) it denotes an A controller connection (only 1 board per controller will define this). If this position is a 1 (switch off) it denotes a B controller connection (only 1 board per controller will define this).

7.3 Power up the control unit by placing the main "AC" breaker in the up position.

7.4 At the disk drive control panel press "Select All". Disable both the "CHA" and "CHB" disk interfaces and enable "Write Protect".

7.5 CDCI adjustment.

7.5.1 On the CDCI board jumper U42-6 to U42-7 and U71-1 to U71-11

DSTRBEAA

7.5.2 At the CDC Cyber computer processor backplane;

On the cable labeled "A" put channel one of the scope on the 10MHZ signal. Put channel two of the scope on the Full signal. Put the ground leads on the opposite pin for each scope probe.

7.5.3 On the CDCI board, switch 2, positions 1 & 2 represents a hex character. Positions 3, 4, 5 & 6 represents the lower hex character. A count between 14 (hex) and 1C (hex) is expected for most mainframes. A good starting value is 18 (hex) for Cyber 65830 and Cyber 960 mainframes. Switch 2, position 7 and 8 must be off.

7.5.4 Adjust SW2 positions 1-6 so that the Full signal is active 10 to 15NS after the 10MHZ signal. Use the positive leading edge at the 50% level for measurements.

7.5.5 Signal diagram: See Attachment A

7.5.6 Remove the jumpers on U42 and U71.

7.5.7 This adjustment must be done for every port on each channel used.

7.5.8 Reset the controller when done with the above adjustments for all CDCI boards.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY" or "CHANNEL READY CODE=000" (FCO 7000-014).

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect". Enable channel "A" and channel "B" ports.

9.2 Replace all doors and covers removed during this installation. The system is now ready for use.

9.3 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 12 on the 7100-3X FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

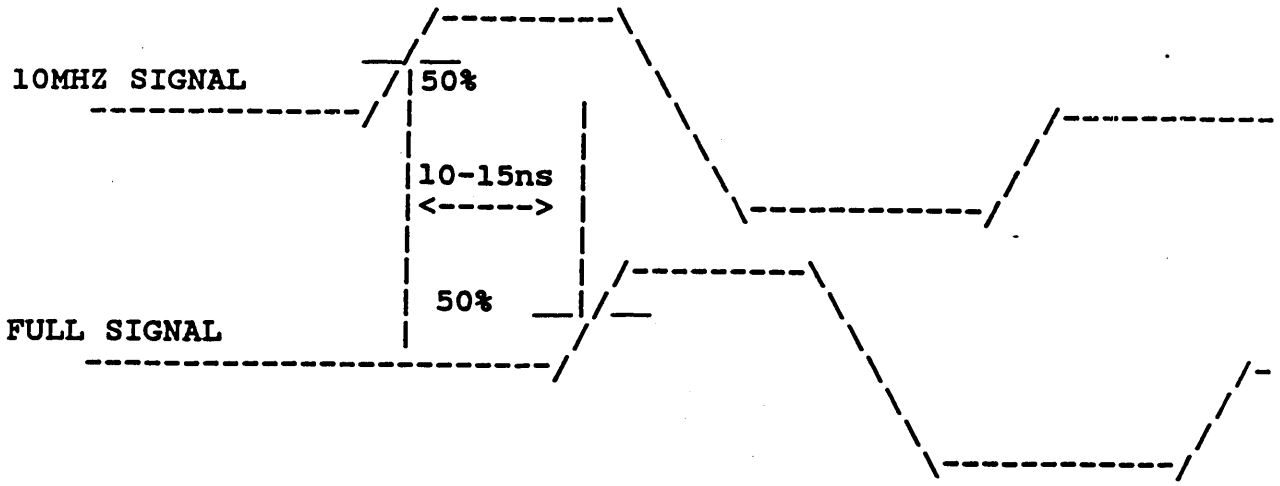
11) Documentation Updates: This information incorporated in future revision.

12) Parts Disposition:

Return parts to: Empros Systems International
2300 Berkshire Lane N.
Plymouth, MN 55441
ATTN: Mr. D.L. Dawkins

13) Attachments: A) Signal Diagram

Attachment A



COC Amp 12-3-92
SN 222
AS FOUND

CONTRL 'B'

SW1 — ADDR

Bϕ — 1, 4, 8 = OFF

B1 — 1, 3, 5, 7 = OFF

SW2 — TIMMING

2, 5, 6, 7, 8 = OFF

2, 5, 6, 7, 8 = OFF

CONTRL 'A'

SW1 — ADD

Aϕ 1, 4 = OFF

A1 1, 3, 5, 7 = OFF

SW2 TIMMING

2, 5, 6, 7, 8 = OFF

2, 5, 6, 7, 8 = OFF

REVISION			
TR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3685		
B	Correction to cover page - ECO 3913		

TITLE XM16KPD Microcode Replacement	REFERENCE ECO 3685
ASSEMBLY DESCRIPTION XM16KPD - Microcode	PART NUMBER 1601495-161 or -171
PRODUCT TYPE/DESCRIPTION 7100-3X Subsystems	MODEL NUMBER 7100-3X
CLASSIFICATION XX MANDATORY OPTIONAL/RETROFIT ON FAILURE	INSTALLATION TIME 1.0
PREREQUISITE NONE	SPARES AFFECTED YES X NO
CONCURRENT FCO 7000-014 and FCO 7000-015	
SUPERCEDES NONE	

REASON(s)

1) Adds assembly flag for disabling cacheing, this reduces code down to fit in 1 prom.

2) This code increases U-bus timeout.

3) This code adds a few messages for ILD-B offline diagnostics.

4) This code fixes STR 65, a problem with HSSM resets during channel truncation.

Note: See sheet 3 for the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING	12-13-90
WATERMAN	12/13/90
CHECKER	
OTHER	
APPROVED	

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FCO 7000-013 Installation Instructions

SIZE	DRAWING NO.		SHEET
A	1602568-101	REV A	1 OF 3

1) Effectivity: 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

XM16KPD is not PN 1601495-211 REV A

3) Materials Required:

PROM PN 1603542-101 REV A

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front door and remove the controller cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove the XM16KPD in both controllers.

7.3 Remove the cover on both XM16KPD's.

7.4 Remove proms from locations U3 and U4.

7.5 Install PN 1603542-101 REV A at location U3 (U4 will remain empty).

7.6 Replace the cover on both XM16KPD's and label as PN 1601495-211 REV A.

7.7 Replace the XM16KPD in both controllers.

7.8 Power up the control unit by placing the main "AC" breaker in the up position.

7.9 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 13 on the 7100-30 FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: EMPROS Systems International
2300 Berkshire Lane N.
Plymouth, MN 55441
ATTN: Mr. D. L. Dawkins

13) Attachments: None.

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3505		
B	Corrections to cover and sheet 3 – ECO 3913		

TITLE	REFERENCE ECO
Driver/Receiver Board Replacement	3505
ASSEMBLY DESCRIPTION	**PART NUMBER**
Driver and Receiver Boards	1602748-101 1602749-201
PRODUCT TYPE/DESCRIPTION	**MODEL NUMBER**
7100-3X Subsystems	7100-3X
CLASSIFICATION	**INSTALLATION TIME**
XX MANDATORY	1.0
____ OPTIONAL/RETROFIT ON FAILURE	
PREREQUISITE None	**SPARES AFFECTED**
CONCURRENT FCO 7000-013 and FCO 7000-014	YES X
SUPERCEDES None	NO ____

REASON(s)

1) Driver board PN 1602748-201 REV A.

2) Receiver board PN 1602749-301 REV A.

3) Adds capability to accommodate shared memory tests.

Note: See sheet 3 for the following items: 1.Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING TK	12-13-90
DRAFTSMAN	12/13/90
CHECKER	
OTHER	
APPROVED B. Bu	12/13/90

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FCO 7000-015 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603570-101 REV B	1 OF 6

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9253

1) **Effectivity:** 7100-3X serial numbers: 101-103,200-223
7102-3X serial numbers: 111-112

2) Identifier:

This FCO has not been installed if:

Driver Board is not PN 1602748-201 REV A
Receiver Board is not PN 1602749-301 REV A

3) Materials Required:

Driver Board PN 1602748-201 REV A
Receiver Board PN 1602749-301 REV A

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open and remove the front and back doors and remove the controller cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove and replace the Driver and Receiver boards located on the controller backplane.

7.3 Power up the control unit by placing the main "AC" breaker in the up position.

7.4 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 8XX and 9xx through both controllers.

9.4 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 15 on the 7100-30 FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: Empros Systems International
2300 Berkshire Lane N.
Plymouth, MN 55441
ATTN: Mr. D. L. Dawkins

13) Attachments: Shared memory offline diagnostic codes.

Changes to
7100-30 and 7100-35 Mass Storage System
Maintenance Manual
for HSP 648A0, ECO 3685

Albert Monroe, Amperif Corp.

1. Shared Memory Offline Diagnostics

Powerup diagnostics and online code check only the local copy of shared memory for errors. Testing writes to the remote (other controller's) copy of shared memory can only be done with the cooperation of the other controller. This is done by the shared memory offline diagnostics. There are read and write diagnostics, each with various options and data patterns. To fully test shared memory, you can have one controller do a shared memory write offline diagnostic, and the other do the coresponding shared memory read offline diagnostic.

Shared memory offline diagnostics are started as other offline diagnostics, ILD 8 and a three hex digit function code. The first digit is 8 for write, 9 for read. The second digit has 4 option flags, entered as a single hex digit. The last digit specifies the data pattern (it is not the drive number as on other offline diagnostics).

Shared memory offline diagnostic function codes:

8xx Writes all addresses
9xx Reads all addresses
x8x Random addresses flag (bit 7), else sequential addresses
x4x Ignore errors flag (bit 6), else stop on error
x2x Continuous flag (bit 5), else one pass
x1x Complement data pattern flag (bit 4)
xx0 Data pattern of all zeros
xx1 Data pattern of repeating 0001
xx2 Data pattern of repeating 0010
xx3 Data pattern of repeating 011 (has odd parity)
xx4 Data pattern of repeating 0100
xx5 Data pattern of repeating 01
xx6 Data pattern of repeating 110
xx7 Data pattern of repeating 000111 (has odd parity)
xx8 Data pattern of repeating 1000
xx9 Data pattern of 9999 hex
xxA Data pattern equal to address (incrementing pattern)
xxF Data pattern of 00FF hex (alternating 0 and 1 each byte)

These can be combined. Thus a function code of 8BA will do writes at random addresses continuously, writing the complement of the address as the data pattern. A function code of 9BA will run the read and compare for the other controller.

WARNING: The write tests DESTROY SHARED MEMORY DATA ON BOTH

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

CONTROLLERS! Both controllers must be offline in order to run these diagnostics.

While a shared memory diagnostic is running, it will display "ILD xxx RUNNING DR.dd" as other offline diagnostics, except the drive number will be meaningless.

If a shared memory diagnostic completes, it will display "ILD xxx COMPLETE, CYL. cccc" on the OCP, as other offline diagnostics, except that the cylinder number will be meaningless. If the continuous flag was specified, the diagnostic will not complete, but will run until error, or the reset button is pressed.

If a shared memory diagnostic gets an error, it will display "ILD xxx CODE = eee, CYL. cccc" on the OCP, as other offline diagnostics, except that the cylinder number will be meaningless, and the error number has new meanings. If the ignore error flag was specified, the diagnostic will not stop on errors or report errors.

Shared memory offline diagnostic error codes:

003 High Speed Bus parity error
004 Data miscompare
005 Local parity error
006 Open shared memory cable
007 Remote parity error

2. Exiting Offline Diagnostics

After any offline diagnostic (ILD B function) is complete, you can enter another offline diagnostic without reinitializing the HSP and going to the online code. To go online, you must enter ILD B FFF, or push the reset button.

3. New OCP Messages

After a reset or a powerup, the HSP runs powerup diagnostics. If these complete successfully, the OCP will display the message "TEST. CODE = 020". As before, if the powerup diagnostics fail, the message "TEST. CODE = 02x", where "x" is the error, will be displayed.

After powerup diagnostics or offline diagnostics are exited (by entering ILD B FFF), the HSP runs coldstart initialization. When these complete, the message "CHANNEL READY CODE = 000" is displayed.

These will also be visible on the OCP thumbwheel switch setting 4DO, the last EF received by the XMC, as a NOOP function with the lower 12 bits containing the code, i.e., 8000C0xxx hex.

4. CDC Detailed Status Bits

Word 12 bit 5, drive error: The HSP always sets this bit to 0.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV.
FCO 7000-015 Installation Instructions	B
DRAWING NO. 1603570-101	SHEET 5 OF 6

Word 16, bit 6, channel data parity error, and bit 1, buffer output register parity error: The HSP sets bit 1 if a local memory address error is detected, bit 6 if a CDCI channel parity error is detected, and both bit 1 and bit 6 if a High Speed Bus or local memory data error is detected.

5. Echo One Word Function

The HSP now supports the CDC diagnostic function of Echo One Word, octal codes 0057 and 0720.

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3843		

TITLE EXXP SIP Socket Removal	**REFERENCE ECO** 3324
ASSEMBLY DESCRIPTION EXXP Boards	**PART NUMBER** 1601909-101
PRODUCT TYPE/DESCRIPTION 710X-XX Subsystems	**MODEL NUMBER** 7100-3X
CLASSIFICATION __XX__ MANDATORY ____OPTIONAL/RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0
PREREQUISITE None	**SPARES AFFECTED** YES XX NO__
CONCURRENT None	
SUPERCEDES None	

REASON(s)

1) Improper SIP socket causing intermittent contact.

2) Causes intermittent Datachecks (43's) to random drives, random locations.

Note: See the following sheets for: 1. Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING Dana Rubrein	3-7-91
DRAFTSMAN	3/7/91
CHECKER	
OTHER	
APPROVED Brian Bank	3/7/91

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FCO 7000-017 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603623-101	1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-0333

1) Effectivity:

7100-1X serial numbers:	101-103, 106-110
7102-3X serial numbers:	111-112
7100-3X serial numbers:	200-223

2) Identifier:

This FCO has not been installed if:

EXXP boards are PN 1601909-101.

3) Materials Required:

2 - EXXP boards PN 1601909-201

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front and back doors and remove the EXXP cardcage cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove and replace the EXXP boards located in the EXXP card cage with those supplied in the FCO kit.

7.3 Power up the control unit by placing the main "AC" breaker in the up position.

7.4 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD 2 to several drives from both controllers for at least 50 cylinders.

9.4 Run ILD B code 2EX through both controllers.

9.5 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 17 on the 710X-XX FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: Empros Systems International
2300 Berkshire Lane N.
Plymouth, MN 55441
Attn: D. L. Dawkins

13) Attachments: None.

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REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3844	3-25-91	

APR 16 1991

TITLE HSP Board to -601	**REFERENCE ECO** 3762
ASSEMBLY DESCRIPTION HSP BOARD	**PART NUMBER** 1602911-501 REV A
PRODUCT TYPE/DESCRIPTION 7100-1X*, 7102-3X*, & 7100-3X Subsystems	**MODEL NUMBER** 7100-1X 710X-3X
CLASSIFICATION _XX_ MANDATORY ___ OPTIONAL/RETROFIT ON FAILURE	**INSTALLATION TIME** 1.0
PREREQUISITE None	**SPARES AFFECTED** YES XX NO___
CONCURRENT * FCO 7000-020 (SNs below 200)	
SUPERCEDES FCO 7000-014	

REASON(s)

1) New firmware release.

2) Power Up/Down Module Corrections.

3) During power down of one controller, shared memory gets a parity error.

Note: See sheet 2 for the following items: 1. Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments

DOCUMENT RELEASE	DATE
ENGINEERING Tony Kilveen	3-18-91
DRAFTSMAN Richard Mena	3/18/91
CHECKER	
OTHER	
APPROVED B. Bang	3/18/91

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FCO 7000-018 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603624-101	1 OF 4

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9253

1) Effectivity:

7100-1X serial numbers:	101-110
7102-3X serial numbers:	111-112
7100-3X serial numbers:	200-223

2) Identifier:

This FCO has not been installed if:

HSP Boards are not PN 1602911-601 REV A or higher.

3) Materials Required:

2 - HSP PN 1602911-601 REV A

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front and back doors and remove the controller cardcage cover.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove and replace the HSP boards located in the controller.

7.3 Check and reset (if necessary) all CDCI board switch settings per the following chart:

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

SW1 SETTINGS (After FCO 7000-018)

B controller
Board 0 - sw 8
OFF

1	2	3	4	5	6	7	8	BRD #
0	0	0	1	1	0	1	*	0
0	0	1	0	1	0	1	*	1
0	1	0	0	1	0	1	*	2
1	0	0	0	1	0	1	*	3
PORT NUMBERS				A or B CONTROLLER				CDCI

NOTE: 0 equals ON
1 equals OFF

* This bit is used to determine A or B controller. If this position is a 0 (switch on) it denotes an A controller connection. If this position is a 1 (switch off) it denotes a B controller connection. All CDCI boards connected must indicate the controller connection (after FCO 7000-018).

7.4 Power up the control unit by placing the main "AC" breaker in the up position.

7.5 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY CODE=000".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Run ILD B's simultaneously from the A and B controllers:

9.4.1 Start ILD B, code 8AA from the A-side controller. Then run ILD B code 9AA from the B-side controller. Allow the test to run two minutes then stop the tests by pressing the RESET button.

9.4.2 Start ILD B, code 8AA from the B-side controller. Then run ILD B code 9AA from the A-side controller. Allow the test to run two minutes then stop the tests by pressing the RESET button.

9.5 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Because this FCO supersedes FCO's 8 and 14, mark an "X" through 8 and 14 of the FCO label if not previously marked.

10.2 Mark an "X" through 18 on the 7100-30 FCO tag.

10.3 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition:

Return parts to: Empros Systems International
2300 Berksire Lane N.
Plymouth, MN 55441
ATTN: Mr. D. L. Dawkins

13) Attachments: None.

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A cont

0
3

1 — 1, 3, 5, 7 = OFF

2 — 1, 3, 4, 5, 7, 8 = OFF

3 — 1, 2, 5, 6 = OFF

0 — 1, 4 = OFF

SW 1
old SW-1 settings

TIMMING
1, 3, 4 = ON

SW 2

B cont

0 - 1, 4, 8 OFF

1 - 1, 3, 5, 7

2 - 1, 3, 4, 5, 7, 8

3 - 1, 2, 5, 6

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	Released via ECO 3845		

4/18/91 MAC & JT
Done S/N 205

TITLE	REFERENCE ECO
System Logic Backplane to -501	None
ASSEMBLY DESCRIPTION	**PART NUMBER**
System Logic Backplane	1602209-201 REV A
PRODUCT TYPE/DESCRIPTION	**MODEL NUMBER**
7100-3X Subsystems	710X-3X
CLASSIFICATION	**INSTALLATION TIME**
XX MANDATORY	1.5
___OPTIONAL/RETROFIT ON FAILURE	
PREREQUISITE None	**SPARES AFFECTED**
CONCURRENT None	YES XX
SUPERCEDES N/A	NO___

REASON(s)

1) Backplane wiring correction.

2) Causes channel hangs.

3) Causes checkword errors.

Note: **See sheet 2 for the following items: 1. Effectivity 2. Identifier 3. Materials Required 4. Tools Required 5. Test Equipment Required 6. Preparation 7. Installation Instructions 8. Verification Instructions 9. Operational Checkout 10. Installation Reporting 11. Documentation Updates 12. Parts Disposition 13. Attachments**

DOCUMENT RELEASE	DATE
ENGINEERING Tony Kilvein	3-7-91
DRAFTSMAN Carol M. Lilly	2/26/91
CHECKER	
OTHER	
APPROVED Bruce Bell	2/27/91

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FCO 7000-019 Installation Instructions

SIZE	DRAWING NO.	SHEET
A	1603625-101	1 OF 4

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-6253

1) Effectivity: 7100-3X serial numbers: 200-206, 209-223

2) Identifier: This FCO has not been installed if:

Controller Logic Backplane is not PN 1602209-501

3) Materials Required: 30 gauge wire

4) Special Tools Required: None

5) Test Equipment: None

6) Preparation:

6.1 This procedure requires both control units must be offline to the host when installing this FCO.

6.2 Bypass all drives.

6.3 At the disk drive control panel press "Select All".

6.3.1 Disable both the CH "A" and CH "B" disk interface.

6.3.2 Place the drives in "Write Protect".

6.4 Open the front and rear doors and remove the rear doors.

7) Installation:

7.1 Power off the both control units by turning off the main AC circuit breaker located in front of the control unit.

7.2 Remove the four (4) receiver/driver paddle boards plugged into the controller logic backplane, locations JJ1A, JJ2A, MJ1A, and MJ2A.

7.3 Inspect the backplane for the fifty-four (54) wires shown on the wire list included in Attachment A. If the jumpers are present, remove them.

7.4 Add the following two (2) wires to the backplane:

7.4.1 Add 30 gauge jumper, from PJ3C-25 to UJ3C-25.

7.4.2 Add 30 gauge jumper, from AJ3C-25 to FJ3C-25.

7.5 Make a new Backpanel part number label by writing on the blank label supplied with this FCO kit. Write three lines as follows:

CTRL BKPNL
1602209-501
REV A

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

Place the label below the "ASSY P/N" words as stamped on the backpanel with the old part number 1602209-201 Rev A. With a black felt tipped pen, black out the "201" tab of the old stamped part number and the old stamped revision letter "A". Also black out the tab "201" and the rev "A" of this part number on the other labels that may also be on the backpanel. An example would be a label that reads "Wired by DataCon,Inc" with the old part number.

7.6 Replace the four (4) receiver/driver paddle boards in the appropriate locations.

7.7 Power up the control unit by placing the main "AC" breaker in the up position.

7.8 At the disk drive control panel press "Select All". Enable both the "CHA" and "CHB" disk interfaces.

8) Verification Instructions:

8.1 At the OCP panel, verify that the control units display the message "CHANNEL READY" or "SYSTEM FULLY RECOVERED".

9) Operational Checkout:

9.1 At disk drive control panel disable "Write Protect".

9.2 Replace all doors and covers removed during this installation.

9.3 Run ILD B code 2EX through both controllers.

9.4 Run ILD B's simultaneously from the A and B controllers:

9.4.1 Start ILD B, code 8AA, from the A-side controller. Then run ILD B, code 9AA, from the B-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.4.2 Start ILD B, code 8AA, from the B-side controller. Then run ILD B, code 9AA, from the A-side controller. Allow the test to run two minutes, then stop the tests by pressing the RESET button.

9.5 Monitor the system for logged errors.

10) Installation Reporting:

10.1 Mark an "X" through 19 on the 7100-30 FCO tag.

10.2 Return the FCO reporting card to Amperif Technical Services.

11) Documentation Updates: None.

12) Parts Disposition: N/A

13) Attachments: A - System Logic Backplane Wiring Diagram

Attachment A.

JJ1A-B30	TPORT(3)/PORTD(3)	MJ2A-B30
JJ1A-B29	PORTACKO*/PORTACKI*	MJ2A-B29
JJ1A-B28	PDOSTB*/PAISTB*	MJ2A-B28
JJ1A-B27	GND	MJ2A-B27
JJ1A-B26	PAOSTB*/PAISTB*	MJ2A-B26
JJ1A-B25	TPA(0)/PORTPA(0)	MJ2A-B25
JJ1A-B24	GND	MJ2A-B24
JJ1A-B23	TPA(1)/PORTPA(1)	MJ2A-B23
JJ1A-B22	TPA(2)/PORTPA(2)	MJ2A-B22
JJ1A-B21	GND	MJ2A-B21
JJ1A-B20	PORTD(0)/TPORT(0)	MJ2A-B20
JJ1A-B19	PORTD(1)/TPORT(1)	MJ2A-B19
JJ1A-B18	GND	MJ2A-B18
JJ1A-B17	PORTD(2)/TPORT(2)	MJ2A-B17
JJ1A-B15	GND	MJ2A-B15
JJ1A-B14	PORTD(4)/TPORT(4)	MJ2A-B14
JJ1A-B13	PORTD(5)/TPORT(5)	MJ2A-B13
JJ1A-B12	GND	MJ2A-B12
JJ1A-B11	PORTD(6)/TPORT(6)	MJ2A-B11
JJ1A-B10	PORTD(7)/TPORT(7)	MJ2A-B10
JJ1A-B9	GND	MJ2A-B9
JJ1A-B8	PORTD(8)/TPORT(8)	MJ2A-B8
JJ1A-B7	PORTD(9)/TPORT(9)	MJ2A-B7
JJ1A-B6	GND	MJ2A-B6
JJ1A-B5	TPORT(10)/PORTD(10)	MJ2A-B5
JJ1A-B4	TPORT(11)/PORTD(11)	MJ2A-B4
JJ1A-B3	TREMOTE/REMOTER	MJ2A-B3
JJ2A-B30	PORTD(3)/TPORT(3)	MJ1A-B30
JJ2A-B29	PORTACKI*/PORTACKO*	MJ1A-B29
JJ2A-B28	PDISTB*/PDOSTB*	MJ1A-B28
JJ2A-B27	GND	MJ1A-B27
JJ2A-B26	PAISTB*/PAOSTB*	MJ1A-B26
JJ2A-B25	PORTPA(0)/TPA(0)	MJ1A-B25
JJ2A-B24	GND	MJ1A-B24
JJ2A-B23	PORTPA(1)/TPA(1)	MJ1A-B23
JJ2A-B22	PORTPA(2)/TPA(2)	MJ1A-B22
JJ2A-B21	GND	MJ1A-B21
JJ2A-B20	PORTD(0)/TPORT(0)	MJ1A-B20
JJ2A-B19	PORTD(1)/TPORT(1)	MJ1A-B19
JJ2A-B18	GND	MJ1A-B18
JJ2A-B17	PORTD(2)/TPORT(2)	MJ1A-B17
JJ2A-B15	GND	MJ1A-B15
JJ2A-B14	PORTD(4)/TPORT(4)	MJ1A-B14
JJ2A-B13	PORTD(5)/TPORT(5)	MJ1A-B13
JJ2A-B12	GND	MJ1A-B12
JJ2A-B11	PORTD(6)/TPORT(6)	MJ1A-B11
JJ2A-B10	PORTD(7)/TPORT(7)	MJ1A-B10
JJ2A-B9	GND	MJ1A-B9
JJ2A-B8	PORTD(8)/TPORT(8)	MJ1A-B8
JJ2A-B7	PORTD(9)/TPORT(9)	MJ1A-B7
JJ2A-B6	GND	MJ1A-B6
JJ2A-B5	PORTD(10)/TPORT(10)	MJ1A-B5
JJ2A-B4	PORTD(11)/TPORT(11)	MJ1A-B4
JJ2A-B3	REMOTER/TREMOTE	MJ1A-B3

" USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

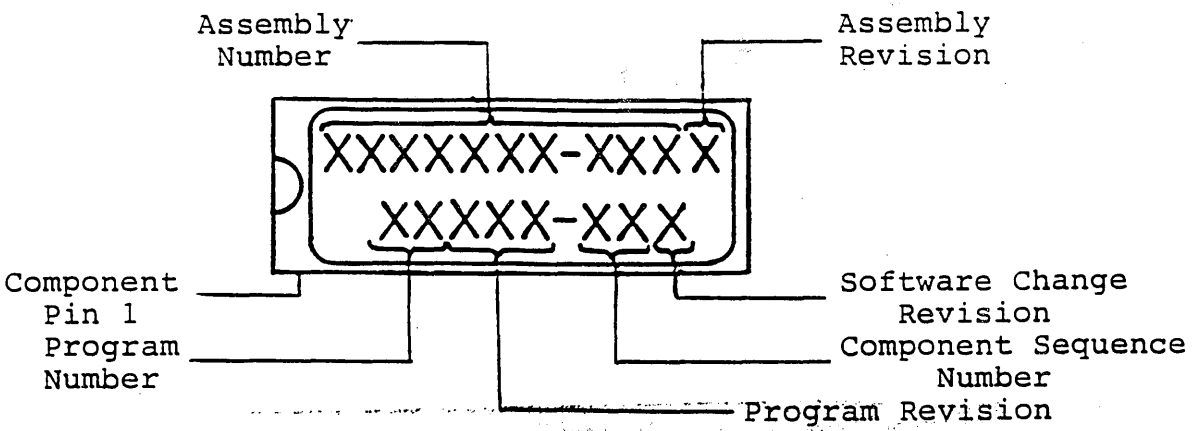
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - ECO # 2029 CR	8-4-89	MM

Procedure:

1. Program component using data filed in software no. 42BA0-01 A.

2. Make from unprogrammed part number 20156600-001.

3. Used on PCBA 1601962-101,201,202 Location U167.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 42 Revision BA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

CHECKSUM = 97E8

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN CHERYL REYNOLDS	3JUN88
CHECKER	
OTHER	
APPROVED	

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PAL ASSEMBLY,

XMCP2

REV A

SIZE	DRAWING NO.	SHEET
A	1602232-101	1 OF 3

BISHOP GRAPHICS/ACCUPRESS

```
Partno      0000-0000 ;
Date        04/APR/88 ;
Revision    01        ;
Designer    R.BUSTAMANTE;
Company     Amperif   ;
Assembly    XMC       ;
Location    U167   ;

/*****************************************************************************




 ******************************************************************************
    Allowable Target Device Types:
 ******************************************************************************/


/** Re-define operators **/

$define :+: $           /* XOR operator                                      */
$define  +  #           /* OR  operator                                      */


/**  Inputs  **/

Pin 1    = A          ;   /*                                                  */
Pin 2    =  ALUY1     ;   /*                                                  */
Pin 3    =  SMCMDLC   ;   /*                                                  */
Pin 4    =  MINST20   ;   /*                                                  */
Pin 5    =  MINST21   ;   /*                                                  */
Pin 6    =  MINST22   ;   /*                                                  */
Pin 7    =  MINST23   ;   /*                                                  */
Pin 8    =  !ALUFOUT  ;   /*                                                  */
Pin 9    =  !CLK12    ;   /*                                                  */
Pin 10   =  !CLK1     ;   /*                                                  */
Pin 11   =  !CLEAR    ;   /*                                                  */
Pin 20   =  ALUY0     ;   /*                                                  */
Pin 14   =  HIOEN     ;   /*                                                  */
Pin 16   =  HIOENA    ;   /*                                                  */


/**  Outputs  **/

Pin 23   =  SEQIR12   ;   /*                                                  */
Pin 22   =  SEQIR13   ;   /*                                                  */
Pin 21   =  SMCMDLB   ;   /*                                                  */
Pin 19   =  RSTIRU    ;   /*                                                  */
Pin 18   =  C         ;   /*                                                  */
Pin 17   = !RSHENA    ;   /*                                                  */
Pin 15   = !RSHEN     ;   /*                                                  */


/** Un-Used Pins **/
/*

*/
```

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

USE OF THIS DOCUMENT IS SUBJECT TO THE

```
/** Declarations and Intermediate Variable Definitions **/

SETIRU = MINST20 & !MINST21 & !MINST22 &  MINST23 & ALUFOUT ;
RSTIRU = !MINST20 & MINST21 & MINST22 &  MINST23 ;

/**  Logic Equations  **/

 SEQIR12.D  = ALUY0 & SETIRU + SEQIR12 & !RSTIRU & !CLEAR + SEQIR12 & !ALUFOUT
 & !CLEAR ;
 SEQIR12.CK = !CLK1  ;
 SEQIR12.AP =  CLEAR ;
 SEQIR13.D  = ALUY1 & SETIRU + SEQIR13 & !RSTIRU & !CLEAR + SEQIR13 & !ALUFOUT
 & !CLEAR ;
 SEQIR13.CK = !CLK1  ;
 SEQIR13.AP =  CLEAR ;
 SMCMDLB.D  = !SMCMDLB & SMCMDLC ;
 SMCMDLB.CK = !CLK12  ;
 RSHEN.D    =  HIOEN  ;
 RSHEN.CK   = !CLK1   ;
 RSHENA.D   =  HIOENA ;
 RSHENA.CK  = !CLK1   ;
```

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV.
PAL ASSEMBLY, XMCP2	A
DRAWING NO. 1602232-101	SHEET 3 OF 3

amperif corporation

FIELD RELEASE NOTICES

FRN #: 004 DATE: January 15, 1990

EFFECTIVITY: 920X-10/30's

This FRN releases the following technical information to the field. These documents may be ordered from Material Services.

ATLAS Diagnostic Package - Rev. 3R3 P/N 1602689-001 Rev. G
Release Tape Assy, Atlas 3R3 (tape only) P/N 1820003-001

The following changes have been incorporated into release 3R3:
- *New label program - NTT
- *Corrects Ferret erroring off in pass 0, phase 3
- *Corrects WRTEST skel error
- *Corrects MDB skel error
- *Adds FMD device (9720) to SURF10
- *Adds FMD device (9720) to RAND10
- *Incorporates ALFA, RAND6, SURF6, FERRET into Assist
- *Enhances ALFA error reporting for CDMF

The following programs have been replaced in release 3R3:
- *RANDIO replaced by RAND10
- *AMPLOG replaced by ALFA39
- *TSTDSK limited use
- *BMXADT replaced by NTT
- *LOG replaced by ALFA39

9200-10 Lowest Acceptable Level (LAL) List (Rev 1/14/91) P/N 1603531-002
* Corrects the part number for the 8085 PCB

NOTE: Addendums are based on Revision C of the maintenance manual. Each addendum requires the previous release to be installed.

9200-30 Maintenance Manual Addendum (Rev. D) P/N 1602943-20D
* Incorporates changes for subsystems without the EXXP PCB.
* Changes to CDMF

9200-30 Maintenance Manual Addendum (Rev. E) P/N 1602943-20E
* Incorporates changes for the new OCP

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

TECH SPEC: [signature] DATE: 1/21/91

APPROVAL: B. Bang [signature] DATE: 1/22/91

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

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FEILD RELEASE NOTICE TABLE OF CONTENTS

FRN001	Releases initial documentation	August 15, 1990
FRN002	FCO 9200-025/026/027/028	September 25, 1990
FRN003	Releases LAL & Updates Documentation	November 16, 1990
FRN004	Releases ATLAS 3R3	January 14, 1991

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

TECH SPEC: [signature] DATE: 1/22/91

APPROVAL: [signature] DATE: 1/22/91

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

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TECHNICAL BULLETIN TABLE OF CONTENTS

9200-001	Drives enabled before caching	September 20, 1990
9200-002	Fujitsu 2382 part numbers	September 20, 1990
9200-003	9200 MM display location correction (534 & 535)	September 20, 1990
9200-004	MCMC switch settings	September 20, 1990
9200-005	Exec level 40 & above using ADT Rev. 1R3	September 20, 1990
9200-006	Reversed DC wiring	September 20, 1990
9200-007	DC Copy Routine	September 20, 1990
9200-008	Interaction of thumbwheel & data switches	September 20, 1990
9200-009	CDMF message not presented when C.U. is "downed"	September 20, 1990
9200-010	NVMF alarm occurs on 56BA0	September 20, 1990
9200-011	AJ12 & AJ13 mislabeled on C.U. backplane	September 20, 1990
9200-012	Marginal AM2925DC chips	September 20, 1990
9200-013	Switch settings between C.U. A & C.U. B	September 20, 1990
9200-014	MCMC interchanageability	September 20, 1990
9200-015	Unrecoverable cache errors downing drives	November 27, 1990
9200-016	SIOA termination	December 11, 1990
9200-017	Processing of defective part tags	January 21, 1991
9200-018	Metal Banding Kit	January 25, 1991

8200-001	Drives enabled before caching	September 20, 1990
8200-002	Fujitsu 2382 part numbers	September 20, 1990
8200-003	MCMC switch settings	September 20, 1990
8200-004	Reversed DC wiring	September 20, 1990
8200-005	AJ12 & AJ13 mislabeled on C.U. backplane	September 20, 1990
8200-006	Marginal AM2925DC chips	September 20, 1990
8200-007	Switch settings between C.U. A & C.U. B	September 20, 1990
8200-008	MCMC interchanageability	September 20, 1990
8200-009	Unrecoverable cache errors downing drives	November 27, 1990
8200-010	Processing of defective part tags	January 22, 1991
8200-011	Meatl Banding Kit	Janaury 25, 1991

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

TECH SPEC: J. Meade DATE: 1/29/91

APPROVAL: Brian Bo L DATE: 1/29/91

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

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FIELD RELEASE NOTICES

FRN #: 003 DATE: November 16, 1990

EFFECTIVITY: 9200-10/30's, 8200-30's

This Field Release Notice releases the following technical information to the field. These documents may be ordered from Material Services.

Technical Publication List — P/N 1603402 Rev. C
* A complete list of available documentation/publication

CDMF KIT - Rev. C — P/N 1602907-701
CDMF Tape, Rev. 3R1C — P/N 1820001
* Corrects for data errors when writing back 8MW of cache when performing a "BYPASS ALL" via CDMF

ATLAS Installation Procedure — P/N 1602789-001
**Note: This is a part number correction for FRN #002*

8200-30 Maintenance Manual — P/N 1602943 Rev. D
* A complete manual, including the revision D update package

8200-30 Maintenance Manual Update Package D — P/N 1602937-20D
* Incorporates changes included in revision D Maintenance Manual. **Only** the updated package needs to be ordered if you already have Maintenance Manual revision C

8200-30 Lowest Acceptable Level (LAL) List — P/N 1603530-001
* Lists the lowest and current acceptable FRU's (Field Replaceable Units) for the 8200-30

9200-10 Lowest Acceptable Level (LAL) List — P/N 1603531-001
* Lists the lowest and current acceptable FRU's (Field Replaceable Units) for the 9200-10

9200-30 Lowest Acceptable Level (LAL) List — P/N 1603532-001
* Lists the lowest and current acceptable FRU's (Field Replaceable Units) for the 9200-30

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

TECH SPEC: [signature] DATE: 11/16/90

APPROVAL: [signature] DATE: 11/26/90

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9254

N RESPONSE TO A MEMO DATED FEBRUARY 23 TO BHEEM SAHGAL WE HAVE
REPARED A PACKAGE TO RESOLVE FINAL CONTRACT REQUIREMENTS. THE
TEMS NOW BEING SUPPLIED ARE AS FOLLOWS :

. PROM LISTINGS — NOTES - OK EXCEPT AS NOTED

A.	PN 1601397-001	rev E	SID 26EA0-01A	XMCIP PCBA	
B.	PN 1601398-001	rev E	SID 26FA0-01A	XMCIP PCBA	
C.	PN 1601399-001	rev E	SID 24-A0-03A	DIF* PCBA's	
D.	PN 1601400-201	rev A	SID 24-A0-04B	DIF* PCBA's	
E.	PN 1601401-002	rev C	SID 24AA0-02A	DIF* PCBA's	
F.	PN 1601402-002	rev C	SID 24AA0-01A	DIF* PCBA's	
G.	PN 1601403-001	rev E	SID 24-A0-01A	DIF* PCBA's	
H.	PN 1601405-201	rev A	SID 24BA0-01B	DIF* PCBA's	
I.	PN 1601407-002	rev C	SID 25-A0-01C	MDBP PCBA	
J.	PN 1601408-002	rev C	SID 25AA0-01B	MDBP PCBA	
K.	PN 1601411-001	rev F	SID 26-A0-01B	XMCIP PCBA	
L.	PN 1601412-001	rev E	SID 26AA0-01A	XMCIP PCBA	
M.	PN 1601413-001	rev E	SID 26BA0-01A	XMCIP PCBA	
N.	PN 1601414-201	rev A	SID 26CA0-01B	XMCIP PCBA	
O.	PN 1601415-001	rev (B)	SID 26DA0-01B	XMCIP PCBA	— OUR BDS HAVE PN 1601415-001 (E)
P.	PN 1601526-001	rev C	SID 06-031-A	XMC* PCBA's	
Q.	PN 1601611-001	rev D	SID 29-A0-01A	EXP MEM PCBA	— COVER SHEET SENT, BUT NO LISTING
R.	PN 1601681-001	rev C	SID 24DA0-01A	DIF* PCBA's	
S.	PN 1601688-001	rev B	SID 34-A0-02A	XMC* PCBA's	
T.	PN 1601689-001	rev B	SID 34-A0-01A	XMC* PCBA's	
U.	PN 1602963-101	rev (B)	SID 24RA0-01A	DIFE PCBA	— OUR BDS HAVE PN 1602963-101 (A)
V.	PN 1602964-101	rev (B)	SID 24SA0-01A	DIFE PCBA	— OUR BDS HAVE PN 1602964-101 (A)
(W)	PN 1106069-	rev D	SID 28-A0-01A	OCP PCB	— NOT SENT ; U38 ON OCP BD

. PAL LISTINGS

	PN 1601566-001	rev D	SID 33-A0-01A	EXP MEM PCBA	
B.	PN 1601567-001	rev E	SID 33AA0-01B	EXP MEM PCBA	
C.	PN 1601568-001	rev D	SID 33BA0-01A	EXP MEM PCBA	
D.	PN 1601569-001	rev D	SID 33CA0-01A	EXP MEM PCBA	
E.	PN 1601570-001	rev D	SID 33DA0-01A	EXP MEM PCBA	
F.	PN 1601571-001	rev D	SID 33EA0-01A	EXP MEM PCBA	
G.	PN 1601572-001	rev D	SID 33FA0-01A	EXP MEM PCBA	
H.	PN 1601573-001	rev C	SID 33GA0-01A	XM16KP PCBA	
I.	PN 1601574-001	rev C	SID 33HA0-01A	XM16KP PCBA	
J.	PN 1601662-001	rev B	SID 24CA0-01A	DIF* PCBA's	
K.	PN 1601692-001	rev B	SID 36-A0-01A	XMCIP PCBA	
L.	PN 1601693-001	rev B	SID 36AA0-01A	XMCIP PCBA	
M.	PN 1601694-001	rev B	SID 36BA0-01A	XMCIP PCBA	
	PN 1601695-001	rev B	SID 36CA0-01A	XMCIP PCBA	
O.	PN 1601696-001	rev B	SID 36DA0-01A	XMCIP PCBA	
P.	PN 1602230-101	rev A	SID 42-A0-01A	XMC* PCBA's	
Q.	PN 1602231-101	rev A	SID 42AA0-01A	XMC* PCBA's	
R.	PN 1602232-101	rev A	SID 42BA0-01A	XMC* PCBA's	
* S.	PN 1603064-101	rev A	SID 43AA0-01A	DDC PCBA	— COVER SHEET SENT, NO PAL EQNS. SENT

. MICROCODE LISTINGS

A.	PN 1601741-001 to 004	SID 17GA0-XXA	OCP OP SYS	
B.	PN 1601925-101 to 103	SID 35EA0-XXA	CDC OP SYS	
C.	PN 1602962-101 to 102	SID 22FB1-XXC	XMC OP SYS	— OUR ROMS HAVE SID L NOT F
	PN 1603101-101 to 104	SID 64-A0-XXA	HSP OP SYS	

TO:FPL JUNE 22, 1990
FROM:MELISSA MAXEY

SUBJECT:RESPONSE TO MEMO DATED 6/7/90 TO BHEEM SAHGAL

PROM LISTINGS:

1601415-001 REV F IS CORRECT FOR PART NO. REV NEW DOCUMENT ATTACHED
1601611-001 LISTING ATTACHED
1602963-101 PART NO. S/B REV B NEW DOCUMENT ATTACHED
1602964-101 PART NO. S/B REV B NEW DOCUMENT ATTACHED
1106069 NEW DOCUMENT ATTACHED

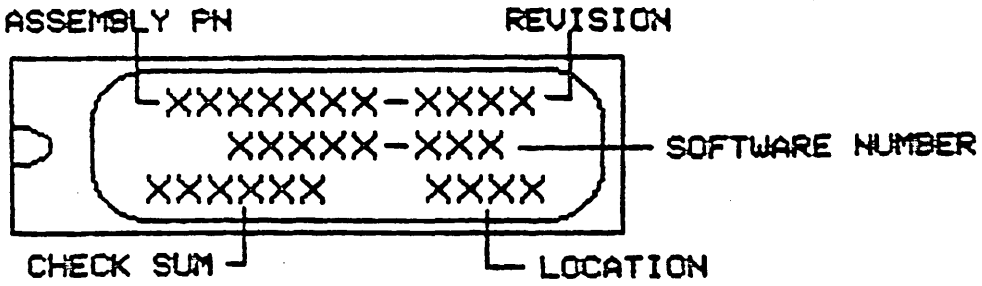
PAL LISTINGS:

1603064-101 PAL EQUATIONS ATTACHED
1602962-101 TO -102 S/B 22FBI-01A 22LBI-01B IS PART NO. 1603109-101
DOCUMENTS FOR BOTH PART NO.'S ATTACHED

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - ECO # 3264 CR	4-23-90	MMahn

PROCEDURE :

1. ASSEMBLY PART NUMBER IS 1603109-101.
2. SEE SEPARATE PARTS LIST.
3. PROGRAM COMPONENT USING DATA FILED IN SOFTWARE NO. 22LB1-01B.
4. MAKE FROM UNPROGRAMMED AMPERIF PART NUMBER 20131900-001.
   VENDOR PN AM27512DC ; DESCRIPTION IC, EPROM, 64K x 8, 250NS, NMOS.
5. USED ON PCBA 1601495-171 LOCATION U3.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.



6. "PROGRAM NUMBER" IS 22 REVISION LB1.
7. "COMPONENT SEQUENCE NUMBER" IS 01.
8. "SOFTWARE CHANGE REVISION" IS B.
9. CHECK SUM IS 8A6E5E.
10. IDENTIFY ON ADHESIVE-BACKED LABEL AS SHOWN AND AFFIX LABEL TO PROGRAMMED PART PER DRAWING ABOVE.

DOCUMENT RELEASE	DATE
ENGINEERING Tom Daa	3/21/90
DRAFTSPERSON C Reynolds	3/20/90
CHECKER L. RNERA	3-21-90
OTHER	
APPROVED Thom Daa 4.01.90	3/21/90

CONFIDENTIAL DOCUMENT
ALL PROHIBITIONS
APPLY.

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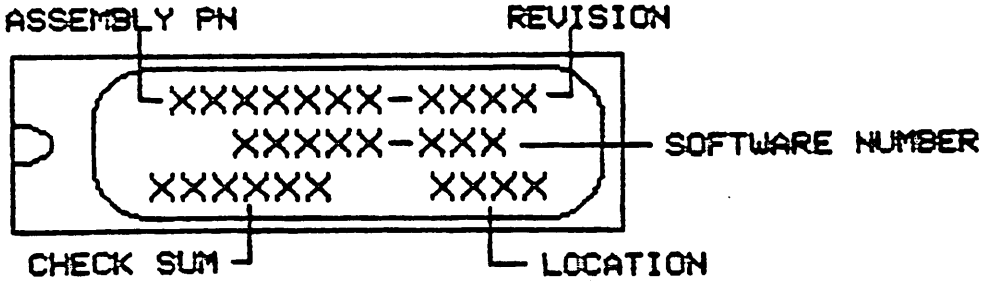
DESCRIPTION	REV
PROM ASSEMBLY, XM16KP OP SYS	A

SIZE	DRAWING NUMBER	SHT	OF
A	1603109-101	1	1

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
	RELEASE - ECO # 3269 CR	4-23-90	MMa...

PROCEDURE :

1. ASSEMBLY PART NUMBER IS 1603109-102.
2. SEE SEPARATE PARTS LIST.
3. PROGRAM COMPONENT USING DATA FILED IN SOFTWARE NO. 22LB1-02.A.
4. MAKE FROM UNPROGRAMMED AMPERIF PART NUMBER 20131900-001.
   VENDOR PN AM27512DC ; DESCRIPTION IC, EPROM, 64K x 8, 250 NS, NMOS.
5. USED ON PCBA 1601495-171 LOCATION U4.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.



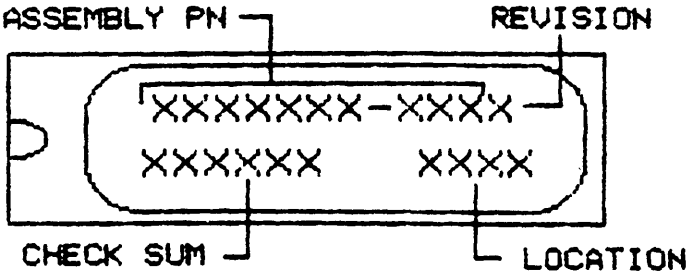
6. "PROGRAM NUMBER" IS 22 REVISION LB1.
7. "COMPONENT SEQUENCE NUMBER" IS 02.
8. "SOFTWARE CHANGE REVISION" IS A.
9. CHECK SUM IS EE0B61.
10. IDENTIFY ON ADHESIVE-BACKED LABEL AS SHOWN AND AFFIX LABEL TO PROGRAMMED PART PER DRAWING ABOVE.

DOCUMENT RELEASE	DATE		
ENGINEERING Tom Lee	3/21/90	CONFIDENTIAL DOCUMENT ALL PROHIBITIONS APPLY. amperif	
DRAFTSPERSON C Rivera	3/20/90		
CHECKER L. RIVERA	3-21-90	DESCRIPTION PROM ASSEMBLY, XM16KP OP SYS	REV A
OTHER		SIZE A	DRAWING NUMBER 1603109-102
APPROVED Steph...	3/21/90		SHT 1 OF 1

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - ECO # 3134 CR	1-17-90	MHB

PROCEDURE :

1. ASSEMBLY PART NUMBER IS 1603064-101.
2. SEE SEPARATE PARTS LIST.
3. PROGRAM COMPONENT USING DATA FILED IN SOFTWARE NO. 43AA0-01A.
4. MAKE FROM UNPROGRAMMED AMPERIF PART NUMBER 20164600-001.
   VENDOR PN AMPAL22V10APC ; DESCRIPTION IC, PAL, 22V10, 25NS.
5. USED ON PCBA 1601916-602 LOCATION U1 thru U16.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.



6. CHECK SUM IS 00A7E5.
7. IDENTIFY ON ADHESIVE-BACKED LABEL AS SHOWN AND AFFIX LABEL TO PROGRAMMED PART PER DRAWING ABOVE.

DOCUMENT RELEASE	DATE	CONFIDENTIAL DOCUMENT ALL PROHIBITIONS APPLY. amperif		
ENGINEERING JK / CAR	12/20/89			
DRAFTSPERSON Cheryl L Reynolds	12/20/89	DESCRIPTION: PAL ASSEMBLY, DDC 7000FPI		REV: A
CHECKER		SIZE: A	DRAWING NUMBER: 1603064	SHT 1 OF 10
OTHER				
APPROVED				

```
*******************************************************************************
                                  9200FP1
*******************************************************************************

CUPL            2.11c Serial# 5-00001-744
Device          p22v10  Library DLIB-f-23-15
Created         Mon Dec 04 13:07:33 1989
Name            9200FP1
Partno          1603064-101 REV A
Date            12/19/89
Partno          43AA0-01A
Revision        02
Date            12/19/89
Designer        J. NELSON
Company         Amperif
Assembly        CDC 7100-30, 7100-35
Location        U1 THRU U16

===============================================================================
                        Expanded Product Terms
===============================================================================

FLTCLR0.ar  =>
    0

FLTCLR0.d  =>
    !FLTCLR0 & DRVSEL0 & FLTCLRS & !RESET
  # FLTCLR0 & !FLTCLRS & !RESET
  # FLTCLR0 & !DRVSEL0 & !RESET

FLTCLR0.oe  =>
    1

FLTCLR0.sp  =>
    0

WP0.ar  =>
    0

WP0.d  =>
    !WP0 & DRVSEL0 & WRTPS
  # WP0 & !WRTPS
  # WP0 & !DRVSEL0

WP0.oe  =>
    1

WP0.sp  =>
    0
```

```
DRVSEL0.ar  =>
    0

DRVSEL0.d  =>
    DRVSEL0S & CDRVSEL & !RESET
  # DRVSEL0 & !CDRVSEL & !RESET
  # ALLDRVS & !RESET

DRVSEL0.oe  =>
    OE

DRVSEL0.sp  =>
    0

PWRONLED =>
    START0

PWRONLED.oe  =>
    OE

START0.ar  =>
    0

START0.d  =>
    PWRONS & DRVSEL0 & !START0 & !RESET
  # !PWRONS & START0 & !RESET
  # !DRVSEL0 & START0 & !RESET

START0.oe  =>
    1

START0.sp  =>
    0

ENCHALED =>
    DISCHA0

ENCHALED.oe  =>
    OE

ENCHBLED =>
    DISCHB0

ENCHBLED.oe  =>
    OE

DISCHA0.ar  =>
    0
```

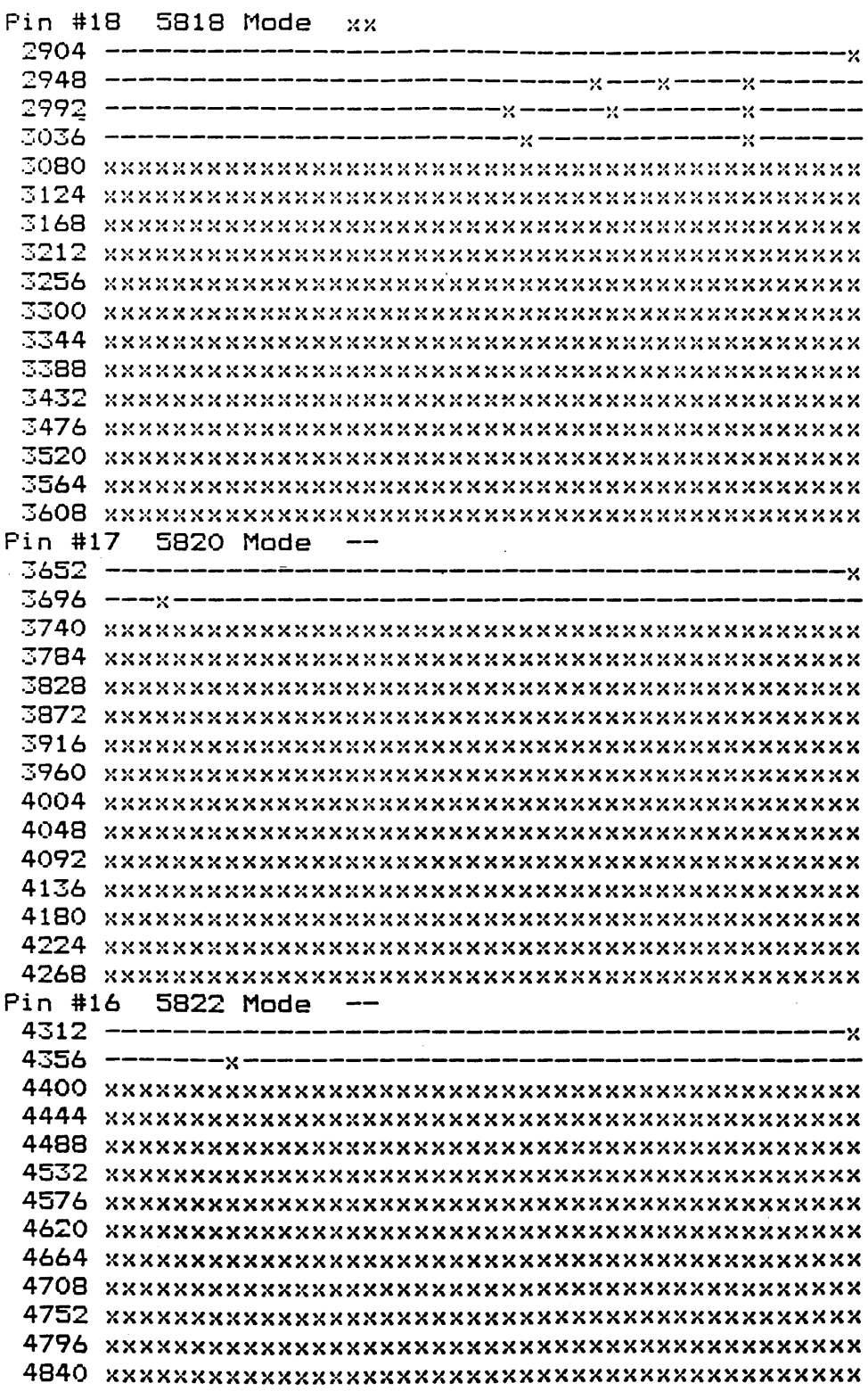
```
DISCHA0.d  =>
    DRVSEL0 & ENCHAS & !DISCHA0
  # !ENCHAS & DISCHA0
  # !DRVSEL0 & DISCHA0


DISCHA0.oe  =>
    1

DISCHA0.sp  =>
    0

WPLED =>
    WP0

WPLED.oe  =>
    OE

DISCHB0.ar  =>
    0

DISCHB0.d  =>
    DRVSEL0 & ENCHBS & !DISCHB0
  # !ENCHBS & DISCHB0
  # !DRVSEL0 & DISCHB0

DISCHB0.oe  =>
    1

DISCHB0.sp  =>
    0
```

Symbol Table

Pin Pol	Variable Name	Ext	Pin	Type	Pterms Used	Max Pterms	Min Level
	PWRONS		6	V	-	-	-
	DRVSEL0S		9	V	-	-	-
!	FLTCLR0		20	V	-	-	-
	FLTCLR0	ar	20	X	1	1	1
!	FLTCLR0	d	20	X	3	14	1
	FLTCLR0	oe	20	X	1	1	1
	FLTCLR0	sp	20	X	1	1	1
!	WP0		21	V	-	-	-
	WP0	ar	21	X	1	1	1
!	WP0	d	21	X	3	12	1
	WP0	oe	21	X	1	1	1
	WP0	sp	21	X	1	1	1
	VCC		24	V	-	-	-
!	DRVSEL0		18	V	-	-	-
	DRVSEL0	ar	18	X	1	1	1
!	DRVSEL0	d	18	X	3	16	1
	DRVSEL0	oe	18	X	1	1	1
	DRVSEL0	sp	18	X	1	1	1
	WRTPS		4	V	-	-	-
	PWRONLED		14	V	1	8	1
	PWRONLED	oe	14	X	1	1	1
	CDRVSEL		8	V	-	-	-
	ENCHAS		2	V	-	-	-
	ENCHBS		3	V	-	-	-
!	OE		13	V	-	-	-
	ALLDRVS		7	V	-	-	-
	FLTCLRS		5	V	-	-	-
!	START0		19	V	-	-	-
	START0	ar	19	X	1	1	1
!	START0	d	19	X	3	16	1
	START0	oe	19	X	1	1	1
	START0	sp	19	X	1	1	1
	CLOCK		1	V	-	-	-
	GROUND		12	V	-	-	-
	ENCHALED		17	V	1	14	1
	ENCHALED	oe	17	X	1	1	1
	ENCHBLED		16	V	1	12	1
	ENCHBLED	oe	16	X	1	1	1
!	DISCHA0		23	V	-	-	-
	DISCHA0	ar	23	X	1	1	1
!	DISCHA0	d	23	X	3	8	1
	DISCHA0	oe	23	X	1	1	1
	DISCHA0	sp	23	X	1	1	1

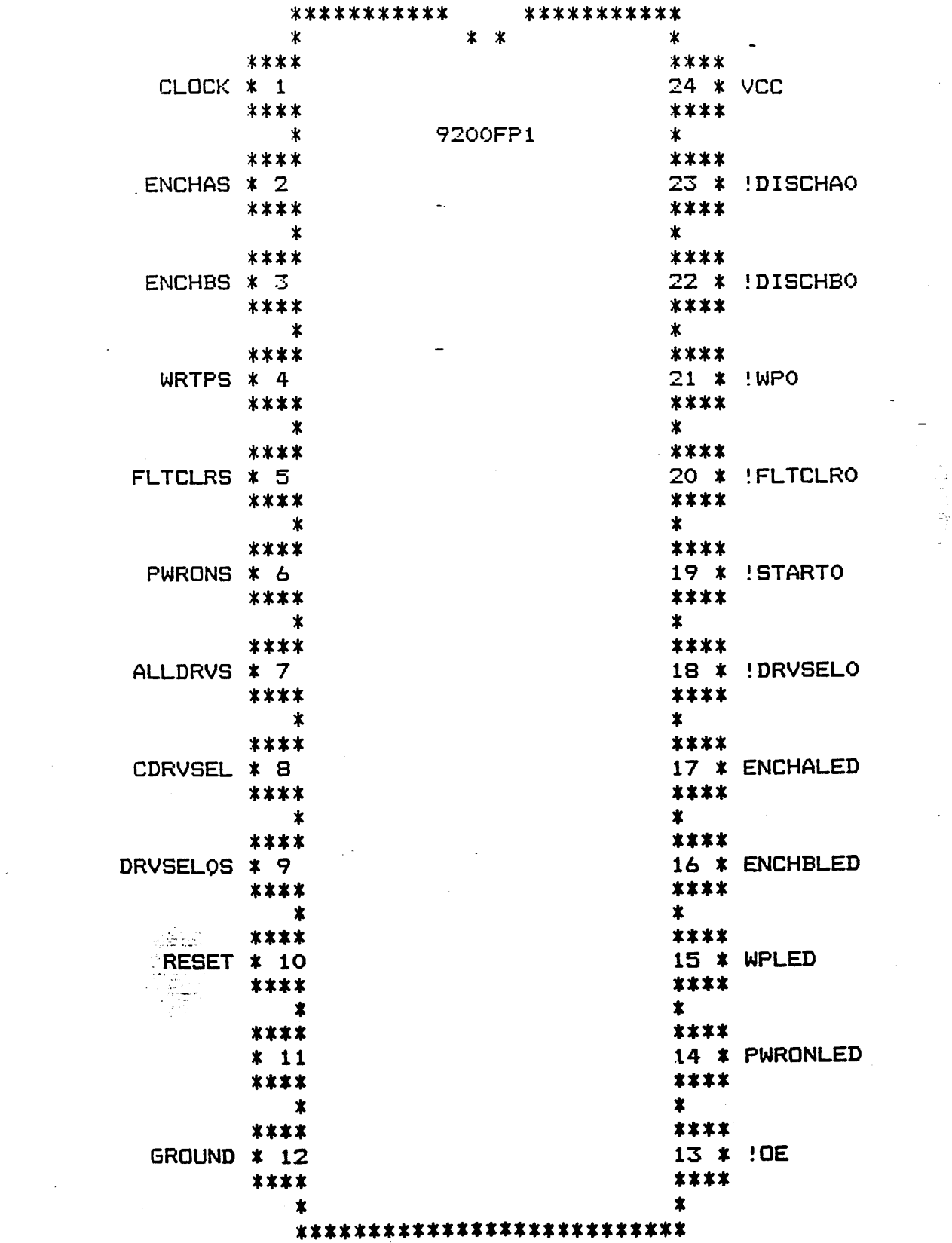
```
    WPLED                    15      V       1       10      1
    WPLED           oe       15      X       1       1       1
 !  DISCHBO                  22      V       -       -       -
    DISCHBO         ar       22      X       1       1       1
 !  DISCHBO         d        22      X       3       10      1
    DISCHBO         oe       22      X       1       1       1
    DISCHBO         sp       22      X       1       1       1
    RESET                    10      V       -       -       -

LEGEND    F : field                      D : default variable
          M : extended node              N : node
          I : intermediate variable      T : function
          V : variable                   X : extended variable
          U : undefined

================================================================
                          Fuse Plot
================================================================

SP
 5764 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

AR
 0000 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

Pin #23  5808 Mode  xx
 0044 ------------------------------------------
 0088 --x-x----------------x--------------------
 0132 ---x-x--------------------------------------
 0176 ---x----------------x--------------------
 0220 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0264 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0308 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0352 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0396 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #22  5810 Mode  xx
 0440 ------------------------------------------
 0484 ------x-x-------------x--------------------
 0528 -------x-x----------------------------------
 0572 -------x--------------x--------------------
 0616 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0660 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0704 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0748 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0792 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0836 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 0880 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```

```
Pin #21  5812 Mode  xx
 0924 ----------------------------------------
 0968 ----------x-x----------x-------------------
 1012 ----------x-x-----------------------------
 1056 ----------x----------x---------------------
 1100 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1144 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1188 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1232 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1276 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1320 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1364 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1408 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1452 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #20  5814 Mode  xx
 1496 ----------------------------------------
 1540 --------------x-x------x-------------x------
 1584 ----------------x-x--------------------x------
 1628 ----------------x------x--------------x------
 1672 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1716 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1760 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1804 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1848 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1892 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1936 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 1980 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2024 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2068 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2112 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #19  5816 Mode  xx
 2156 ----------------------------------------
 2200 ------------------x-x--x-------------x------
 2244 ------------------x-x----------------x------
 2288 ------------------x--x---------------x------
 2332 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2376 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2420 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2464 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2508 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2552 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2596 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2640 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2684 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2728 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2772 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2816 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 2860 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
```


Pin #18 5818 Mode xx
2904
2948
2992
3036
3080
3124
3168
3212
3256
3300
3344
3388
3432
3476
3520
3564
3608
Pin #17 5820 Mode --
3652
3696
3740
3784
3828
3872
3916
3960
4004
4048
4092
4136
4180
4224
4268
Pin #16 5822 Mode --
4312
4356
4400
4444
4488
4532
4576
4620
4664
4708
4752
4796
4840

```
Pin #15  5824 Mode  x-
 4884 ----------------------------------------x
 4928 ----------x-----------------------------
 4972 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5016 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5060 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5104 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5148 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5192 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5236 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5280 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5324 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
Pin #14  5826 Mode  --
 5368 ----------------------------------------x
 5412 ----------x-----------------------------
 5456 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5500 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5544 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5588 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5632 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5676 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
 5720 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx

LEGEND     X : fuse not blown
           - : fuse blown
```

Chip Diagram



ENGINEERING CHANGE REQUEST/ORDER

ECR ☑ ECO ☐

ECR/ECO NO. 3129

PROJ. TITLE	MDW	SFTWR	IAI	CHANGE YES NO	CHANGE CLASS	FIELD	AMENDMENTS
7100-30 7100-10	☐	☑	☐	LAL: ☑ ☐	☒ A ☐ B ☐ C ☐ D	☐ YES ☒ NO	

REQSTR/DRAWN: R. BUSTAMANTE, C. REYNOLDS
DATE: 12-7-89

CHECKED BY

DATE:

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☒ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☐ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: DISABLE CHECKING DRIVE NUMBER IN HEADER.

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
	22FBI	A	B	MICROCODE, XM16KP OPSYS
1602962-102	1602962-102	A	B	PROM ASSY, XM16KP OPSYS, 7100-30
1601495-TAB	—	A	B	ASSY DWG, PROM BD-XM16KP
—	1601495-131	A	B	PL & PCBA, PROM BD-XM16KP
1601495	—	AJ	AK	CONF LIST, PROM BD-XM16KP

INCORPORATION DISPOSITION

Master MM

	USE AS	REWORK	SCRAP
IN FIELD	☐	☒	☐
FIELD SPARES	☐	☒	☐
FINISHED GOODS	☐	☒	☐
FINAL ASSY	☐	☒	☐
IN TEST	☐	☒	☐
IN PROCESS	☐	☒	☐
IN STOCK	☐	☒	☐
NEXT ASSY	☐	☒	☐
ON ORDER	☐	☒	☐
NEXT BUY	☐	☒	☐
OTHER	☐	☒	☐

NOTE: 3 FCO 7100-001

INCORP. OF CHANGE DATE 1-8-90 SERIAL NO CI108

SPECIAL INSTRUCTION: F up

CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	[signature]	12/19/89
SFTWR	[signature]	
MARKETING		
MFG. ENG.	[signature]	12-20-89
QUALITY	A. [signature]	12/20/89
SERVICE	B. [signature]	12/20/89
ENG. SERV.	M [signature]	1/9/90
DIR. OF ENG.	[signature]	

ECO # 3129
SHT 2
OF 7

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 7000-00A REV 1.0
XMC OP SYS

WAS / IS	PROG ADDR / PROM ADDR	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
	11A78	1A7C	1A7B	1A7A	1A79	1A78	1A7D		
WAS	2F14	3 2	7 F				E7	OR ZQ LSBZ,,RO	
IS	2F14	4 3	3 F				EF	RESETR RO	NO DR
	12006	2010	200F	200E	200D	200C	2012		
WAS	3002	3 2	7 F				E7	OR ZQ LSBZ,RO	
IS	3002	4 3	3 F				EF	RESETR RO	NO DR
WAS									
IS									
WAS									
IS									
WAS									
IS									

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT
EE3E10-C.S.

CHANGE DESCRIPTION: DISABLE CHECKING DRIVE NUMBER IN HEADER TO BE USED ON 7100-30 SYSTEM ONLY.

MASTERS TO DOC CTL. _____
DATE _____
NEW PROM REQD. _____
PROM NO. 2

DATE 12-1-89
INIT. BY [illegible]
PAGE 1 OF 1
PCO # 22FB1-XXB

AS OF 1/01/91

FROM: A
TO: B

CLASS CODE: 3
UNASSIGNED

1602962-102 OPCODE: 3 REV: A PROM ASY,XM16KP OP SYS,7100-30
MODEL: 7100-30
ECO NO: 3071
DATE OF LAST ECO: 11/21/89

FROM: 3071 TO: 3129

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20131900-001	IC,EPROM,64KX8,250NS,NMOS	3	A	1	1.000	1.000	EA	P	Y	N	1.000	0	0	22FB1-02A	00/00/00	99/99/99
20144913-001	LABEL,IC,.75X.25,POLYFILM	3	A	2	.000	1.000	RL	F	Y	N	.000	0	0		00/00/00	99/99/99

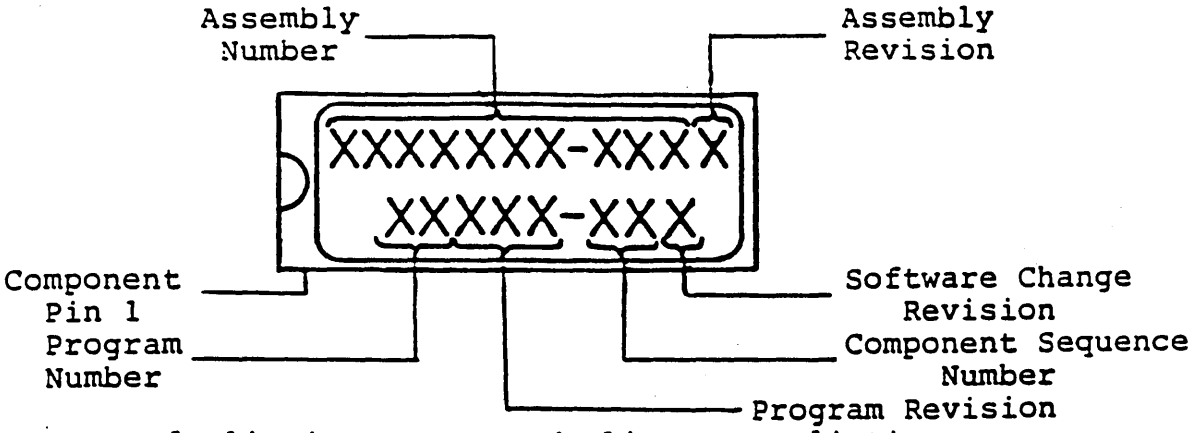
FROM: A
TO: B

ECO # 3129 SHT 3 OF 7

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
AX	PROTOTYPE CR		
A	RELEASE - ECO 3071		
B	UPDATE - ECO 3129		

Procedure:

1. Program component using data filed in software no. 22FB1-02A. FROM: A TO: B
2. Make from unprogrammed part number 20131900-001.
3. Used on PCBA 1601495-131 Location U3.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.
5. "Software Change Revision" is A. FROM: A TO: B
4. "Component Sequence Number" is 02.
3. "Program Number" is 22 Revision FB1.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown. FROM: A TO: B
1. See separate parts list.

ADD: CHKSUM: EE3E10

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	8/31/9
CHECKER	
OTHER ECO # 3129	
APPROVED SNT 4 OF 7	

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amperif memory products

PROM ASSEMBLY, XM16KP OP SYS (SABER 5)

REV A

SIZE	DRAWING NO.	SHEET
A	1602962-102	1 OF 1

LI,200 DATABA01 AMPERIF CORPORATION DISTRIBUTION: CHERYLR - ENG SERVICES
THU, 7, 1989 BILL MATERIAL E NO: 1
AS OF 1/01/91

FROM: A
TO: B

CLASS CODE: 28
PCBA OUTSIDE

1601495-131 OPCODE: 3 REV: A PCBA,PROM BD-XM16KP,7100-30
MODEL: 7100-30
ECO NO: 3071
DATE OF LAST ECO: 11/21/89

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

FROM: 3071 TO: 3129

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
0601458-001	PCB,PROM BD-XM16KP	3	B	1	1.000	1.000	EA	B	Y	N	1.000	0	0	PCB	00/00/00	99/99/99
0601572-001	HSG. PROM BDD. FRONT	3	B	2	1.000	1.000	EA	B	Y	N	1.000	0	0		00/00/00	99/99/99
0601572-002	HSG. PROM BD BACK	3	B	3	1.000	1.000	EA	B	Y	N	1.000	0	0		00/00/00	99/99/99
1602962-101	PROM ASY,XM16KP OP SYS,7100-30	3	A	4	1.000	1.000	EA	B	Y	N	1.000	0	0	U3	00/00/00	99/99/99
1602962-102	PROM ASY,XM16KP OP SYS,7100-30	3	A	5	1.000	1.000	EA	B	Y	N	1.000	0	0	U4	00/00/00	99/99/99
20010800	IC,DRVR,QUAD,3ST,8TO9	3	A	6	1.000	1.000	EA	P	Y	N	1.000	0	0	U2	00/00/00	99/99/99
20018402	CAP,CER,RAD,.1UF,50V,20%,.2 LS	3	A	7	4.000	1.000	EA	P	Y	N	4.000	0	0	C2-C5	00/00/00	99/99/99
20018902	CAP,TANT,RAD,10UF,20%,16V	3	A	8	1.000	1.000	EA	P	Y	N	1.000	0	0	C1	00/00/00	99/99/99
20108108	CONN,DIN,48P,FEM,R/A	3	A	9	1.000	1.000	EA	P	Y	N	1.000	0	0	P1	00/00/00	99/99/99
20119513-006	SCREW,PNHPH,2-56 X 7/16	3	A	10	2.000	1.000	EA	F	Y	N	2.000	0	0		00/00/00	99/99/99
20119513-104	SCREW,PNHPH,4-40 X 5/16,ZINC	3		11	2.000	1.000	EA	F	Y	N	2.000	0	0		00/00/00	99/99/99
20121713-001	NUT,HEX,PLAIN,2-56	3	A	12	2.000	1.000	EA	F	Y	N	2.000	0	0		00/00/00	99/99/99
20121713-002	NUT,PLAIN,HEX ,4-40,CRES	3		13	2.000	1.000	EA	F	Y	N	2.000	0	0		00/00/00	99/99/99
20122113-001	WSHR,SPLK,#2	3	A	14	2.000	1.000	EA	F	Y	N	2.000	0	0		00/00/00	99/99/99
20122113-002	WSHR,SPLK,K#4	3	A	15	2.000	1.000	EA	F	Y	N	2.000	0	0		00/00/00	99/99/99
20131500-001	IC,ADDER,4BIT,BIN,S283	3	A	16	1.000	1.000	EA	P	Y	N	1.000	0	0	U1	00/00/00	99/99/99
20132508-001	RES,SIP,8P,10K,COM	3	A	17	1.000	1.000	EA	P	Y	N	1.000	0	0	RN1	00/00/00	99/99/99
20133203-001	SKT,DIP,28P,PCMT	3	B	18	2.000	1.000	EA	B	Y	N	2.000	0	0	XU3,XU4	00/00/00	99/99/99
20144913-002	LABEL,IC,.80X.50,POLYFILM	3	A	19	.000	1.000	RL	F	Y	N	.000	0	0		00/00/00	99/99/99
20135513-001	JUMPER,WIRE,.1"	3	A	20	4.000	1.000	EA	F	Y	N	4.000	0	0	J1-J4	00/00/00	99/99/99

FROM: A
TO: B

ECO # 3129
SHT 5 OF 7

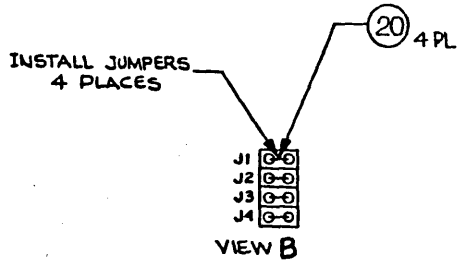
NOTES: UNLESS OTHERWISE SPECIFIED

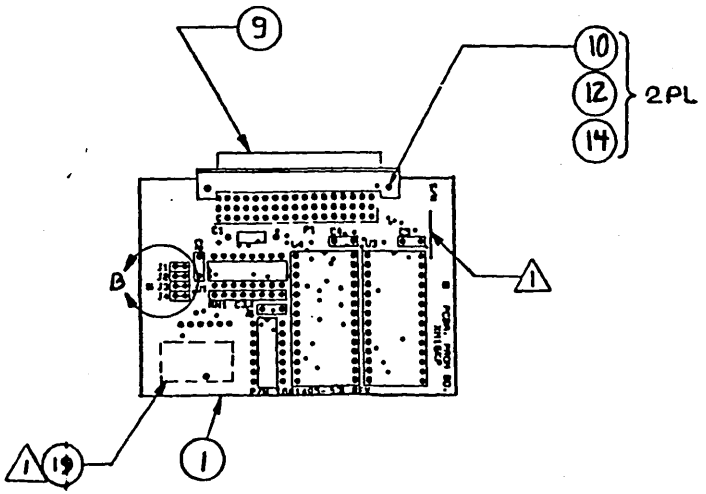
⚠ IDENTIFY ASSY AS P/N 1601495-☐ CURRENT REV LETTER AND S/N APPROX WHERE SHOWN, 2 PLACES.

2. FOR SCHEMATIC SEE DWG NO. 1601495-101.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	NEW COMB PWG ECO 3046		
	B	UPDATE PER ECO 3129		

ADD:



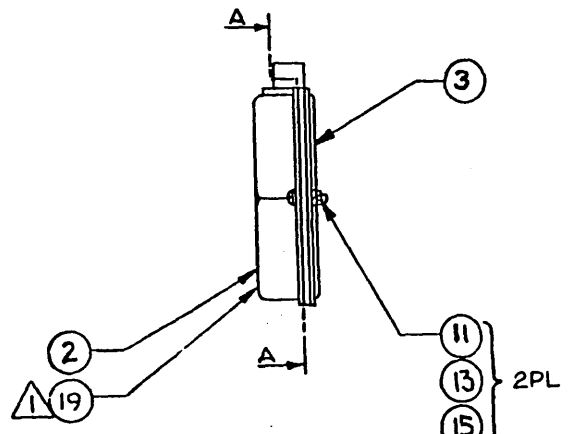


SECTION A-A
(BOARD VIEW ONLY)

FROM: A
TO: B

⚠1

ASSY PN	REV	APPLICABLE OPTION	SYSTEM USE
1601495-141	A	1603005-101 REV A AT LOCATION U3 1603005-102 REV A AT LOCATION U4	'NOT LINKED'
1601495-131	A	1602962-101 REV AX AT LOC. U3 1602962-102 REV AX AT LOC. U4	SABER 5
1601495-121	A	1602504-201 REV A AT LOCATION U3 1602504-202 REV A AT LOCATION U4	CDMF
1601495-111	B	1602627-301 REV B AT LOCATION U3 1602627-302 REV A AT LOCATION U4	CH 7000
1601495-991	B	1602627-201 REV B AT LOCATION U3 1602627-202 REV A AT LOCATION U4	'NOT USED'
1601495-981	A	1602504-101 REV E AT LOCATION U3 1602504-102 REV E AT LOCATION U4	9200-10
1601495-971	A	1602627-101 REV C AT LOCATION U3 1601627-102 REV C AT LOCATION U4	'NOT USED'
1601495-961	A	1602472-201 REV A AT LOCATION U3 1602472-202 REV A AT LOCATION U4	MMFS. SIERRA ST II
1601495-951	C	1602504-101 REV E AT LOCATION U3 1602504-102 REV E AT LOCATION U4	'NOT USED'
1601495-941	A	1602472-101 REV A AT LOCATION U3 1602472-102 REV A AT LOCATION U4	SIERRA. 5090 ST II
1601495-931	A	1602315-101 REV A AT LOCATION U3 1602315-102 REV A AT LOCATION U4	'NOT USED'
1601495-921	D	1602241-101 REV C AT LOCATION U3 1602241-102 REV C AT LOCATION U4	'NOT USED'
1601495-911	C	1602242-101 REV C AT LOCATION U3 1602242-102 REV C AT LOCATION U4	CHIIA SSS
1601495-901	C	1601949-201 REV B AT LOCATION U3 1601949-202 REV B AT LOCATION U4	5090 ST I
1601495-801	B	1601949-101 REV A AT LOCATION U3 1601949-102 REV A AT LOCATION U4	'NOT USED'
1601495-701	H	1601895-101 REV F AT LOCATION U3 1601895-102 REV C AT LOCATION U4	CHIIA. CHIE. CHIIE
1601495-601	D	1601884-101 REV B AT LOCATION U3 1601884-102 REV B AT LOCATION U4	3MB RPQ
1601495-501	B	1601876-101 REV A AT LOCATION U3 1601876-102 REV A AT LOCATION U4	'NOT USED'
1601495-401	C	1601711-101 REV B AT LOCATION U3 1601711-102 REV B AT LOCATION U4	'NOT USED'



FROM: A
TO: B

SEE SEPARATE PARTS LIST

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amperif

PCB ASSEMBLY:
XM16 KP

APPROVALS	DATE
DRAWN L.K	1/14/97
CHECKED	
APPROVED	

SCALE: FULL | SIZE: C | DRAWING NO. 1601495-TAB | A

DO NOT SCALE DRAWING | SHEET 1 OF 1

ECO # 3129

SNT 6 OF 7

ADD: 7

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1601495-131	B	1601495-101	A	0601458-001	B	0601458-001	A	4	-	PROM UPDATE	3129
1601495-141	Ax	1601495-101	A	0601458-001	B	0601458-001	A	4	-	PROM CHG CREATE -141	PROTOTYPE
1601495-131	A	1601495-101	A	0601458-001	B	0601458-001	A	4	-	PROM CHG CREATE -131	3071
1601495-911	C	1601495-101	A	0601458-001	B	0601458-001	A	4	-	PROM UPDATE	3041

NOTES: UNLESS OTHERWISE SPECIFIED.

- FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001
- THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD/ ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

SHT 1 OF 5

NEXT ASSY

USED ON

DR BY

CHK BY

APPROVED BY

CONFIGURATION LIST : PCBA XM16KP-D

FROM: AJ
TO: AK

SIZE A

DWG NO. 1601495

REV AJ

SCALE:

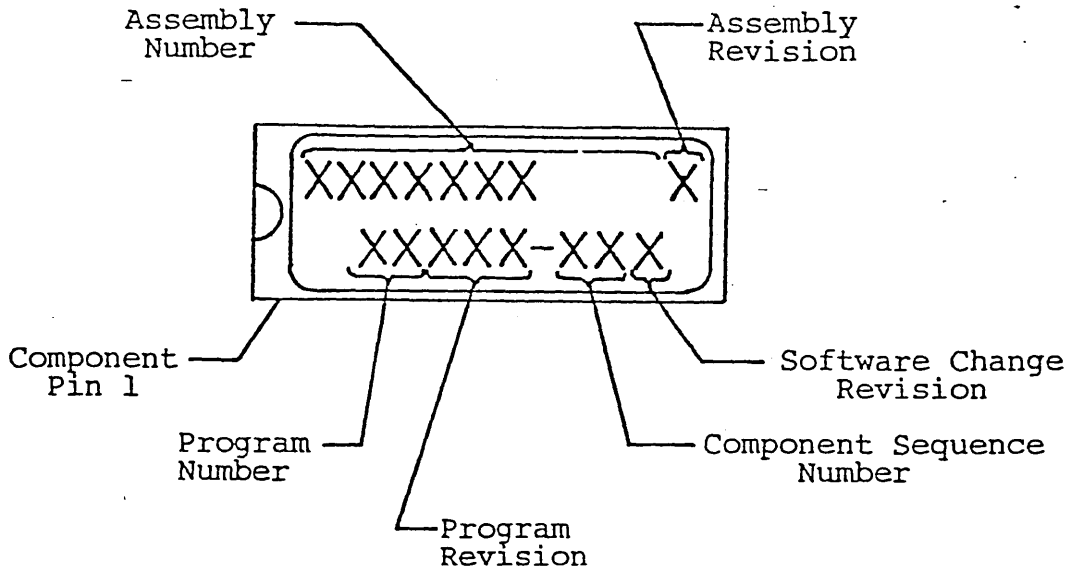
SHEET 5 OF 5

REVISION

LTR	DESCRIPTION	DATE	APPROVED
C	REVISED & REDRAWN SEE ECO 1306	2-5-87	
	ECO 1405	8-31-89	MM

Procedure:

1. Program component using data filed in software No. 28-AO-01A .
2. Make from unprogrammed part number 20012600 .
3. PCBA Used on 1106068-201 Location AK3



6. FOR PROM CODE SEE SEPARATE LISTING.
5. "Software change revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 28 Revision -AO .
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN M. KAISER	1-27-87
CHECKER	
OTHER	
APPROVED	

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amperif memory products

PROM ASSEMBLY, OCPM @ AK3

SIZE	DRAWING NO.	SHEET	REV
A	1106069	1 OF 1	D

© BISHOP GRAPHICS, ACCUPRESS REORDER NO. A-5253

1106069 REV. B

28-A0-01A

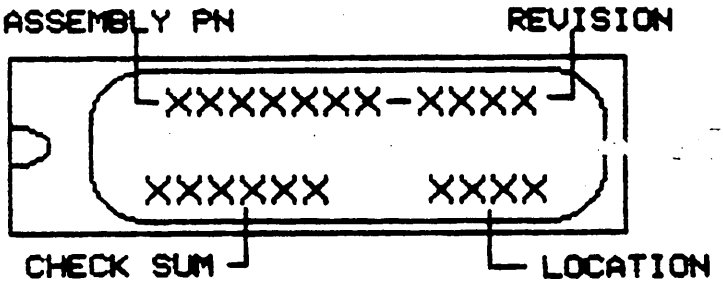
```
$A0000,
0 F F F F F 6 F F F F F F F F F F
0 1 2 3 4 5 6 7 F F F
$A0000,
0 F F F F F 6 F F F F F F F F F F
0 1 2 3 4 5 6 7 F F F
$A0000,
0 F F F F F 6 F F F F F F F F F F
0 1 2 3 4 5 6 7 F F F F F F F F F
0 8 9 A B C 6 D F F F F F F F F F
0 F F F F F 6 F F F F F F F F F F
0 1 2 3 4 5 6 7 F F F F F F F F F
0 1 2 3 4 5 6 7 F F F F F F F F F
0 1 2 3 4 5 6 7 F F F F F F F F F
0 1 2,3 4 5 6 7 F F F F F F F F F

$A0080,
0 8 9 A B C 6 D F F F F F F F F F
0 8 9 A B C 6 D F F F F F F F F F
0 8 9 A B C 6 D F F F F F F F F F
0 8 9 A B C 6 D F F F F F F F F F
0 F F F F F 6 F F F F F F F F F F
0 F F F F F 6 F F F F F F F F F F
0 F F F F F 6 F F F F F F F F F F
0 F F F F F 6 F F F F F F F F F F
$S0BA5,
```

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
NIX	PROTOTYPE		
A	PROD. REL. ECO 3071	12/5/89	M Mayer
B	INK CHG PER ECO 3214	3/12/90	M Mayer

PROCEDURE :

1. ASSEMBLY PART NUMBER IS 1602963-101.
2. SEE SEPARATE PARTS LIST.
3. PROGRAM COMPONENT USING DATA FILED IN SOFTWARE NO. 24RA0-01A.
4. MAKE FROM UNPROGRAMMED AMPERIF PART NUMBER 20071199.
   VENDOR PN AM27S29PC ; DESCRIPTION IC,PROM,512x8,35T,70NS.
5. USED ON PCBA 1601716-802 LOCATION U125.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.



6. "PROGRAM NUMBER" IS 24 REVISION RA0.
7. "COMPONENT SEQUENCE NUMBER" IS 01.
8. "SOFTWARE CHANGE REVISION" IS A.
9. CHECK SUM IS 01F38E.
10. IDENTIFY ON ADHESIVE-BACKED LABEL AS SHOWN AND AFFIX LABEL TO PROGRAMMED PART PER DRAWING ABOVE.

DOCUMENT RELEASE	DATE
ENGINEERING Bruce Lee	11/20/89
DRAFTSPERSON Cheryl Reynolds	11/9/9
CHECKER [illegible]	11/17/89
OTHER	
APPROVED Paul D. Walker	11-20-89

CONFIDENTIAL DOCUMENT
ALL PROHIBITIONS
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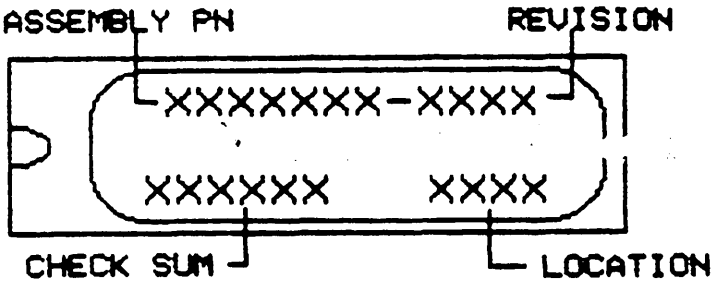
DESCRIPTION	REV
PROM ASSEMBLY, DIF DR CONS-LSB	B

SIZE	DRAWING NUMBER	SHT OF
A	1602963-101	1 1

REVISION			
TR	DESCRIPTION	DATE	APPROVED
AX	PROTOTYPE		
A	PROD. REL ECO 3071	12-5-89	M Mallia
B	INC CHG PER ECO 3214	3-12-90	M Mallia

PROCEDURE :

1. ASSEMBLY PART NUMBER IS 1602964-101.
2. SEE SEPARATE PARTS LIST.
3. PROGRAM COMPONENT USING DATA FILED IN SOFTWARE NO. 24SA0-01A.
4. MAKE FROM UNPROGRAMMED AMPERIF PART NUMBER 20071199.
   VENDOR PN AM27S29PC ; DESCRIPTION IC, PROM, 512x8, 3ST, 70NS.
5. USED ON PCBA 1601716-802 LOCATION U405.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.



6. "PROGRAM NUMBER" IS 24 REVISION SA0.
7. "COMPONENT SEQUENCE NUMBER" IS 01.
8. "SOFTWARE CHANGE REVISION" IS A.
9. CHECK SUM IS 01FD84.
10. IDENTIFY ON ADHESIVE-BACKED LABEL AS SHOWN AND AFFIX LABEL TO PROGRAMMED PART PER DRAWING ABOVE.

DOCUMENT RELEASE	DATE
ENGINEERING Bruce Chan	11/20/89
DRAFTSPERSON Cheryl Reynolds	11/9/9
CHECKER J Beers	11/17/89
OTHER	
APPROVED John C. Walker	11-22-89

CONFIDENTIAL DOCUMENT
ALL PROHIBITIONS
APPLY.

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DESCRIPTION	REV
PROM ASSEMBLY, DIF DR CONS - MSB	B

SIZE	DRAWING NUMBER	SHT	OF
A	1602964-101	1	1

```
Addr    Line

                1   ;
                2   ;
                3   ;       DIFF Drive Constant PROMS
                4   ;       MSB = DF52-U105      LSB = DF38-U125
                5   ;
                6   ;       Date: 11-AUG-88
                7   ;
                8   ;       For BURROUGHS word prep length 40 words/record.
                9   ;       Hard Sector track formatting only.
               10   ;
               11   ;
               12   ;                   Drive Pointer Index Table
               13   ;
               14   ;       Addr        Drive Type          Size          Type Number
               15   ;
               16   ;       000         Drive not defined
               17   ;       012         Fujitsu M2344 (SW4) 690 MB.............5
               18   ;                   [116 prep] 1=12, 2=96, 3=116, 4=192
               19   ;                   [456 prep] 1=1B, 2=9F, 3=11F, 4=19B
               20   ;
               21   ;       024         Drive not defined
               22   ;
               23   ;       036         Drive not defined
               24   ;
               25   ;       048         Fujitsu M2333 (SW3) 337 MB.............3
               26   ;                   [116 prep] 1=48, 2=CC, 3=14C, 4=1C8
               27   ;                   [456 prep] 1=51, 2=D5, 3=155, 4=1D1
               28   ;
               29   ;       05A         Fujitsu M2382 (SW5) 1.02 GB............4
               30   ;                   [40 prep] 1=5A, 2=DE, 3=15E, 4=1DA
               31   ;
               32   ;       06C         CDC 368              337 MB.........data copy
               33   ;                   [256 prep] 1=6C, 2=F0, 3=170, 4=1EC
               34   ;
               35   ;       075         Fujitsu M2333 (SW3) 337 MB.........data copy
               36   ;                   [256 prep] 1=75, 2=F9, 3=179, 4=1F5
               37   ;
               38   ;   Legend: 1 = Read Header
               39   ;           2 = Read Data
               40   ;           3 = Write Data
               41   ;           4 = Format
               42
```

```
Addr  Line

      43        EJECT
      44    ;*****************************************************************
      45    ;  The values below were calculated with the following           *
      46    ;  equations.                                                     *
      47    ;                                                               *
      48    ;  1. data bytes/words per formatted record:                      *
      49    ;     bytes = (bytes/record - overhead bytes/record)            *
      50    ;     words = (bytes/record div.by 4.5)                         *
      51    ;  2. data bytes/track = (records/track * data bytes/record)     *
      52    ;  3. data words/track = ((data bytes/record * records/track)    *
      53    ;                         div.by 4.5)                           *
      54    ;  4. data words/cylinder = (data words/track * tracks/cylinder) *
      55    ;  5. records/track = ((bytes/track div.by bytes/record) -1)     *
      56    ;  6. record time = (bytes/record * byte time)                   *
      57    ;  7. % of formatted track utilization = ((data bytes/record *   *
      58    ;                           records/track) div.by bytes/track)  *
      59    ;                                                               *
      60    ;*****************************************************************
```

```
Addr  Line

                61        EJECT
                62
                63    ;*************************************************************
                64    ;*          Fujitsu M2333 (SW3) 337 MB  drive type #3        *
                65    ;*************************************************************
                66    ;*                                                           *
                67    ;* data bytes/words per formatted record:...180/40           *
                68    ;*                                                           *
                69    ;* write to read recovery time = 9.74 usec = 24 bytes        *
                70    ;* bytes per record:.........................250             *
                71    ;* bytes per track:........................40,960           *
                72    ;* records per track:.......................162             *
                73    ;* bytes per track used:...................40,500           *
                74    ;* byte time (nano secs.):..................406             *
                75    ;* record time (usecs.):...................101.50           *
                76    ;* % of formatted track utilization.........71.2           *
                77    ;* data words per track:..................6,480           *
                78    ;* tracks per cylinder:.....................10             *
                79    ;* data words per cylinder:...............64,800           *
                80    ;* overhead per record (bytes):.............70             *
                81    ;*                                                           *
                82    ;*     sector switch setting                                 *
                83    ;*      SW1                  SW2                             *
                84    ;* 1 2 3 4 5 6 7      1 2 3 4 5 6 7                         *
                85    ;* ---------------    ---------------                       *
                86    ;* 0 1 1 1 1 0 1 0    0 1 0 0 0 0 0                         *
                87    ;*************************************************************
                88    ;*                                                           *
                89    ;* data bytes/words per formatted record:...180/40           *
                90    ;*                                                           *
                91    ;* bytes per record:.........................250             *
                92    ;* bytes per track:........................40,960           *
                93    ;* records per track:.......................162             *
                94    ;* bytes per track used:...................40,500           *
                95    ;* byte time (nano secs.):..................406             *
                96    ;* record time (usecs.).....................101.5            *
                97    ;* % of formatted track utilization.........71.2           *
                98    ;* data words per track:..................6,480           *
                99    ;* tracks per cylinder:.....................10             *
               100    ;* data words per cylinder:...............64,800           *
               101    ;* overhead per record (bytes):.............70             *
               102    ;*                                                           *
               103    ;* sector switch setting same as 522/116 blocking factor    *
               104    ;*************************************************************
```

```
Addr  Line

      105         EJECT
      106     ;*****************************************************************
      107     ;*          Fujitsu M2344 (SW4)  690 MB  drive type #5           *
      108     ;*****************************************************************
      109     ;*                                                               *
      110     ;* data bytes/words per formatted record:...180/40              *
      111     ;*                                                               *
      112     ;* write to read recovery time = 10.55 usec = 26 bytes           *
      113     ;* bytes per record:.........................266                  *
      114     ;* bytes per track:........................40,960                *
      115     ;* records per track:.......................152                  *
      116     ;* bytes per track used:...................40,432                *
      117     ;* byte time (nano secs.):..................406                  *
      118     ;* record time (usecs.).....................108                  *
      119     ;* % of formatted track utilization.........66.8                 *
      120     ;* data words per track:...................6,080                 *
      121     ;* tracks per cylinder:.....................27                   *
      122     ;* data words per cylinder:.............164,160                   *
      123     ;* overhead per record (bytes):.............86                   *
      124     ;*                                                               *
      125     ;* sector switch setting                                         *
      126     ;*       SW1                 SW2                                 *
      127     ;* 1 2 3 4 5 6 7       1 2 3 4 5 6 7                             *
      128     ;* -------------       -------------                             *
      129     ;* 0 1 1 1 0 1 0       0 1 0 0 0 0 0                             *
      130     ;*                                                               *
      131     ;*****************************************************************
      132     ;*                                                               *
      133     ;* data bytes/words per formatted record:...180/40              *
      134     ;*                                                               *
      135     ;* bytes per record:.........................266                  *
      136     ;* bytes per track:........................40,960                *
      137     ;* records per track:.......................152                  *
      138     ;* bytes per track used:...................40,432                *
      139     ;* byte time (nano secs.):..................406                  *
      140     ;* record time (usecs.).....................108                  *
      141     ;* % of formatted track utilization.........66.8                 *
      142     ;* data words per track:...................6,080                 *
      143     ;* tracks per cylinder:.....................27                   *
      144     ;* data words per cylinder:.............164,160                   *
      145     ;* overhead per record (bytes):.............86                   *
      146     ;*                                                               *
      147     ;* sector switch setting same as 522/116 blocking factor         *
      148     ;*****************************************************************
```

```
Addr  Line

      149         EJECT
      150     ;*************************************************************
      151     ;*       Fujitsu M2382 (SW5)  1.02 GB drive type 83          *
      152     ;*************************************************************
      153     ;*                                                           *
      154     ;* data bytes/words per formatted record:...180/40           *
      155     ;*                                                           *
      156     ;* write to read recovery time = 11.32 usec = 34 bytes       *
      157     ;* bytes per record:.........................276              *
      158     ;* bytes per track:........................49,728             *
      159     ;* records per track:.......................181 - (xmc)      *
      160     ;*                          ...............180 - (host)     *
      161     ;* bytes per track used:...................49,680             *
      162     ;* byte time (nano secs.):..................333              *
      163     ;* record time (usecs.).....................91.9              *
      164     ;* % of formatted track utilization.........65.15            *
      165     ;* data words per track:...................7,200             *
      166     ;* tracks per cylinder:.....................27               *
      167     ;* data words per cylinder:.............194,400               *
      168     ;* overhead per record (bytes):.............86+10(pad)       *
      169     ;*                                                           *
      170     ;*              sector switch setting                        *
      171     ;*              SW4                SW5                       *
      172     ;*         7 6 5 4 3 2 1      7 6 5 4 3 2 1                 *
      173     ;*         -------------      -------------                 *
      174     ;*         0 0 0 1 0 0 0      0 0 0 0 0 0 1                 *
      175     ;*                                                           *
      176     ;*         SW1-5 = 0/HARD SECTOR FORMAT                      *
      177     ;*                                                           *
      178     ;*************************************************************
```

```
Addr  Line

      179        EJECT
      180    ;*************************************************************
      181    ;*         CDC 368   337 MB data copy drive                  *
      182    ;*************************************************************
      183    ;*                                                           *
      184    ;* data bytes/words per formatted record:..1152/256          *
      185    ;*                                                           *
      186    ;* write to read recovery time = 12.67 usec = 23 bytes       *
      187    ;* bytes per record:.....................1,224               *
      188    ;* bytes per track:.....................30,240               *
      189    ;* records per track:.....................24                  *
      190    ;* bytes per track used:................29,376               *
      191    ;* byte time (nano secs.):...............551.2               *
      192    ;* record time (usecs.)..................674.67              *
      193    ;* % of formatted track utilization.....91.4                 *
      194    ;* data words per track:................6,144                *
      195    ;* tracks per cylinder:..................10                  *
      196    ;* data words per cylinder:............61,440                *
      197    ;* overhead per record (bytes):............72                *
      198    ;*                                                           *
      199    ;*     sector switch setting                                 *
      200    ;*      SW1                SW2                               *
      201    ;* 1 2 3 4 5 6 7      1 2 3 4 5 6 7                          *
      202    ;* -------------      -------------                          *
      203    ;* X X X X X X X      X X X X X X X                          *
      204    ;*************************************************************
      205    ;*        Fujitsu M2333 (SW3) 337 MB data copy drive         *
      206    ;*************************************************************
      207    ;*                                                           *
      208    ;* data bytes/words per formatted record:..1152/256          *
      209    ;*                                                           *
      210    ;* bytes per record:.....................1,222               *
      211    ;* bytes per track:.....................40,960               *
      212    ;* records per track:.....................33                  *
      213    ;* bytes per track used:................40,326               *
      214    ;* byte time (nano secs.):...............406                 *
      215    ;* records time (usecs.).................496.13               *
      216    ;* % of formatted track utilization.....92.81                *
      217    ;* data words per track:................8,448                *
      218    ;* tracks per cylinder:..................10                  *
      219    ;* data words per cylinder:............84,480                *
      220    ;* overhead per record (bytes):............70                *
      221    ;*                                                           *
      222    ;* sector switch setting is a don't care                     *
      223    ;*************************************************************
```

```
 Addr    Line

                 224         EJECT
                 225     ;*************************************************************
                 226     ;*
                 227     ;* READ HEADER
                 228     ;*
                 229     ;* DRIVE TYPE = GENERAL DRIVE DEFAULT VALUES
                 230     ;* BLOCK SIZE = N/A
                 231     ;*
                 232     ;****** ADDRESSES '00' AND '09' ARE USED FOR VERIFY AND READ HEADER
                 233     ;****** COMMANDS. THIS APPLIES TO ALL DRIVE TYPES USED WHEN THE
                 234     ;****** XMC IS TRYING TO FIND THE DRIVE TYPE OF THE DEVICE
                 235     ;****** SELECTED TO BE READ.
                 236     ;*
00000            237         ORG     H#00
00000 00FFFE     238         DW 02-  ;PLO TO SYNC DELAY
00001 00FFD8     239         DW 40-  ;SYNC WINDOW
00002 00FFFB     240         DW 05-  ;OF HEADER DATA
00003 00FFFC     241         DW 04-  ;HEADER ECC
00004 00FFFE     242         DW 02-  ;READ/WRITE PAD
                 243     ;*
                 244     ;* READ HEADER
                 245     ;*
00009            246         ORG     H#09
00009 00FFFB     247         DW  05- ;PLO TO SYNC DELAY
0000A 00FFEC     248         DW 20-  ;SYNC WINDOW
0000B 00FFFB     249         DW 05-  ;OF HEADER DATA
0000C 00FFFC     250         DW 04-  ;HEADER ECC
0000D 00FFFE     251         DW 02-  ;READ/WRITE PAD
                 252     ;*
                 253     ;* READ HEADER
                 254     ;*
                 255     ;* DRIVE TYPE = FUJI 2344 (SW4)
                 256     ;* BLOCK SIZE = 180/40
                 257     ;*
00012            258         ORG H#12
00012 00FFF6     259         DW  10- ;PLO TO SYNC DELAY
00013 00FFE4     260         DW  28- ;SYNC WINDOW
00014 00FFFB     261         DW  5-  ;OF HEADER DATA
00015 00FFFC     262         DW  4-  ;HEADER ECC
00016 00FFFE     263         DW  2-  ;READ/WRITE PAD
                 264     ;
                 265     ;*
                 266     ;* READ HEADER
                 267     ;*
                 268     ;* DRIVE TYPE = FUJI 2344 (SW4)
                 269     ;* BLOCK SIZE = 180/40
                 270     ;*
0001B            271         ORG H#1B
0001B 00FFF6     272         DW  10- ;PLO TO SYNC DELAY
0001C 00FFE4     273         DW  28- ;SYNC WINDOW
0001D 00FFFB     274         DW  5-      ;OF HEADER DATA
0001E 00FFFC     275         DW  4-      ;HEADER ECC
0001F 00FFFE     276         DW  2-      ;READ/WRITE PAD
                 277     ;*
                 278     ;* READ HEADER
```

```
Addr     Line
                279     ;*
                280     ;* DRIVE TYPE = FUJI 2333 (SW3)
                281     ;* BLOCK SIZE = 180/40
                282     ;*
00048           283         ORG H#48
00048 00FFFF    284         DW  2-  ;PLO TO SYNC DELAY
00049 00FFD0    285         DW  48- ;SYNC WINDOW
0004A 00FFFB    286         DW  5-  ;OF HEADER DATA
0004B 00FFFC    287         DW  4-  ;HEADER ECC
0004C 00FFFE    288         DW  2-  ;READ/WRITE PAD
                289     ;
                290     ;*
                291     ;* READ HEADER
                292     ;*
                293     ;* DRIVE TYPE = FUJI 2333 (SW3)
                294     ;* BLOCK SIZE = 180/40
                295     ;*
00051           296         ORG H#51
00051 00FFFE    297         DW  2-  ;PLO TO SYNC DELAY
00052 00FFD0    298         DW  48- ;SYNC WINDOW
00053 00FFFB    299         DW  5-  ;OF HEADER DATA
00054 00FFFC    300         DW  4-  ;HEADER ECC
00055 00FFFE    301         DW  2-  ;READ/WRITE PAD
```

```
 Addr      Line

                302         EJECT
                303     ;*
                304     ;* READ HEADER
                305     ;*
                306     ;* DRIVE TYPE = FUJI 2382 (SW5)
                307     ;* BLOCK SIZE = 180/40
                308     ;*
0005A           309         ORG H#5A
0005A 00FFFE    310         DW  2-  ;PLO TO SYNC DELAY
0005B 00FFD0    311         DW  48- ;SYNC WINDOW
0005C 00FFFB    312         DW  5-  ;OF HEADER DATA
0005D 00FFFC    313         DW  4-  ;HEADER ECC
0005E 00FFFC    314         DW  4-  ;READ/WRITE PAD
                315     ;
                316     ;*
                317     ;* READ HEADER
                318     ;*
                319     ;* DRIVE TYPE = FUJI 2382 (SW5)
                320     ;* BLOCK SIZE = 180/40
                321     ;*
00063           322         ORG H#63
00063 00FFFE    323         DW  2-  ;PLO TO SYNC DELAY
00064 00FFD0    324         DW  48- ;SYNC WINDOW
00065 00FFFB    325         DW  5-  ;OF HEADER DATA
00066 00FFFC    326         DW  4-  ;HEADER ECC
00067 00FFFC    327         DW  4-  ;READ/WRITE PAD
                328     ;*
                329     ;* READ HEADER
                330     ;*
                331     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
                332     ;* BLOCK SIZE = 1152/256
                333     ;*
0006C           334         ORG H#6C
0006C 00FFF7    335         DW  9-  ;PLO TO SYNC DELAY
0006D 00FFF0    336         DW  16- ;SYNC WINDOW
0006E 00FFFB    337         DW  5-  ;OF HEADER DATA
0006F 00FFFC    338         DW  4-  ;HEADER ECC
00070 00FFFE    339         DW  2-  ;READ/WRITE PAD
                340     ;
                341     ;*
                342     ;* READ HEADER
                343     ;*
                344     ;* DRIVE TYPE = FUJI 2382 (DATA COPY DRIVE)
                345     ;* BLOCK SIZE = 1152/256
                346     ;*
00075           347         ORG H#75
00075 00FFFE    348         DW  2-  ;PLO TO SYNC DELAY
00076 00FFD0    349         DW  48- ;SYNC WINDOW
00077 00FFFB    350         DW  5-  ;OF HEADER DATA
00078 00FFFC    351         DW  4-  ;HEADER ECC
00079 00FFFC    352         DW  4-  ;READ/WRITE PAD
```

```
Addr     Line
                  353          EJECT
                  354      ;*
                  355      ;* READ DATA
                  356      ;*
                  357      ;* DRIVE TYPE = FUJI 2344 (SW4)
                  358      ;* BLOCK SIZE = 180/40
                  359      ;*
00096             360          ORG H#096
00096 00FFFE      361          DW  2-  ;READ GATE ENABLE
00097 00FFD0      362          DW  48- ;PLO GAP  TO SYNC
00098 00FF4B      363          DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
00099 00FFFC      364          DW  4-  ;DATA ECC
0009A 00FFFE      365          DW  2-  ;READ/WRITE PAD
                  366      ;
                  367      ;*
                  368      ;* READ DATA
                  369      ;*
                  370      ;* DRIVE TYPE = FUJI 2344 (SW4)
                  371      ;* BLOCK SIZE = 180/40
                  372      ;*
0009F             373          ORG H#09F
0009F 00FFFE      374          DW  2-  ;READ GATE ENABLE
000A0 00FFD0      375          DW  48- ;PLO GAP  TO SYNC
000A1 00FF4B      376          DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
000A2 00FFFC      377          DW  4-  ;DATA ECC
000A3 00FFFE      378          DW  2-  ;READ/WRITE PAD
                  379      ;*
                  380      ;* READ DATA
                  381      ;*
                  382      ;* DRIVE TYPE = FUJI 2333 (SW3)
                  383      ;* BLOCK SIZE = 180/40
                  384      ;*
000CC             385          ORG H#0CC
000CC 00FFFF      386          DW  2-  ;READ GATE ENABLE
000CD 00FFD0      387          DW  48- ;PLO GAP  TO SYNC
000CE 00FF4B      388          DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
000CF 00FFFC      389          DW  4-  ;DATA ECC
000D0 00FFFE      390          DW  2-  ;READ/WRITE PAD
                  391      ;
                  392      ;*
                  393      ;* READ DATA
                  394      ;*
                  395      ;* DRIVE TYPE = FUJI 2333 (SW3)
                  396      ;* BLOCK SIZE = 180/40
                  397      ;*
000D5             398          ORG H#0D5
000D5 00FFFE      399          DW  2-  ;READ GATE ENABLE
000D6 00FFD0      400          DW  48- ;PLO GAP  TO SYNC
000D7 00FF4B      401          DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
000D8 00FFFC      402          DW  4-  ;DATA ECC
000D9 00FFFE      403          DW  2-  ;READ/WRITE PAD
```

```
Addr    Line
                404         EJECT
                405     ;*
                406     ;* READ DATA
                407     ;*
                408     ;* DRIVE TYPE = FUJI 2382 (SW5)
                409     ;* BLOCK SIZE = 180/40
                410     ;*
000DE           411         ORG H#0DE
000DE 00FFFE    412         DW  2-  ;READ GATE ENABLE
000DF 00FFD0    413         DW  48- ;PLO GAP  TO SYNC
000E0 00FF4B    414         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
000E1 00FFFC    415         DW  4-  ;DATA ECC
000E2 00FFFE    416         DW  2-  ;READ/WRITE PAD
                417     ;
                418     ;*
                419     ;* READ DATA
                420     ;*
                421     ;* DRIVE TYPE = FUJI 2382 (SW5)
                422     ;* BLOCK SIZE = 180/40
                423     ;*
000E7           424         ORG H#0E7
000E7 00FFFE    425         DW  2-  ;READ GATE ENABLE
000E8 00FFD0    426         DW  48- ;PLO GAP  TO SYNC
000E9 00FF4B    427         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
000EA 00FFFC    428         DW  4-  ;DATA ECC
000EB 00FFFE    429         DW  2-  ;READ/WRITE PAD
                430     ;*
                431     ;* READ DATA
                432     ;*
                433     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
                434     ;* BLOCK SIZE = 1152/256
                435     ;*
000F0           436         ORG H#0F0
000F0 00FFFE    437         DW  2-  ;READ GATE ENABLE
000F1 00FFE0    438         DW  32- ;PLO GAP  TO SYNC
000F2 00FB7F    439         DW  1152*   ;RECORD LENGTH (ONES COMPLEMENT)
000F3 00FFFC    440         DW  4-  ;DATA ECC
000F4 00FFFE    441         DW  2-  ;READ/WRITE PAD
                442     ;
                443     ;*
                444     ;* READ DATA
                445     ;*
                446     ;* DRIVE TYPE = FUJI 2382 (DATA COPY DRIVE)
                447     ;* BLOCK SIZE = 1152/256
                448     ;*
000F9           449         ORG H#0F9
000F9 00FFFE    450         DW  2-  ;READ GATE ENABLE
000FA 00FFD0    451         DW  48- ;PLO GAP  TO SYNC
000FB 00FB7F    452         DW  1152*   ;RECORD LENGTH (ONES COMPLEMENT)
000FC 00FFFC    453         DW  4-  ;DATA ECC
000FD 00FFFE    454         DW  2-  ;READ/WRITE PAD
```

```
 Addr     Line

                  455         EJECT
                  456     ;*
                  457     ;* WRITE DATA
                  458     ;*
                  459     ;* DRIVE TYPE = FUJI 2344 (SW4)
                  460     ;* BLOCK SIZE = 180/40
                  461     ;*
00116             462         ORG H#116
00116 00FFFE      463         DW  2-  ;WRITE GATE ENABLE
00117 00FFF1      464         DW  15- ;PLO GAP
00118 00FF4B      465         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
00119 00FFFB      466         DW  5-  ;DATA ECC
0011A 00FFFE      467         DW  2-  ;END OF RECORD PAD
                  468     ;*
                  469     ;* WRITE DATA
                  470     ;*
                  471     ;* DRIVE TYPE = FUJI 2344 (SW4)
                  472     ;* BLOCK SIZE = 180/40
                  473     ;*
0011F             474         ORG H#11F
0011F 00FFFE      475         DW  2-  ;WRITE GATE ENABLE
00120 00FFF1      476         DW  15- ;PLO GAP
00121 00FF4B      477         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
00122 00FFFB      478         DW  5-  ;DATA ECC
00123 00FFFE      479         DW  2-  ;END OF RECORD PAD
                  480     ;*
                  481     ;* WRITE DATA
                  482     ;*
                  483     ;* DRIVE TYPE = FUJI 2333 (SW3)
                  484     ;* BLOCK SIZE = 180/40
                  485     ;*
0014C             486         ORG H#14C
0014C 00FFFF      487         DW  2-  ;WRITE GATE ENABLE
0014D 00FFF1      488         DW  15- ;PLO GAP
0014E 00FF4B      489         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
0014F 00FFFB      490         DW  5-  ;DATA ECC
00150 00FFFE      491         DW  2-  ;END OF RECORD PAD
                  492     ;*
                  493     ;* WRITE DATA
                  494     ;*
                  495     ;* DRIVE TYPE = FUJI 2333 (SW3)
                  496     ;* BLOCK SIZE = 180/40
                  497     ;*
00155             498         ORG H#155
00155 00FFFE      499         DW  2-  ;WRITE GATE ENABLE
00156 00FFF1      500         DW  15- ;PLO GAP
00157 00FF4B      501         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
00158 00FFFB      502         DW  5-  ;DATA ECC
00159 00FFFE      503         DW  2-  ;END OF RECORD PAD
```

```
Addr    Line

                504         EJECT
                505     ;*
                506     ;* WRITE DATA
                507     ;*
                508     ;* DRIVE TYPE = FUJI 2382 (SW5)
                509     ;* BLOCK SIZE = 180/40
                510     ;*
0015E           511         ORG H#15E
0015E 00FFFE    512         DW  2-  ;WRITE GATE ENABLE
0015F 00FFEF    513         DW  17- ;PLO GAP
00160 00FF4B    514         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
00161 00FFFB    515         DW  5-  ;DATA ECC
00162 00FFFE    516         DW  2-  ;END OF RECORD PAD
                517     ;*
                518     ;* WRITE DATA
                519     ;*
                520     ;* DRIVE TYPE = FUJI 2382 (SW5)
                521     ;* BLOCK SIZE = 180/40
                522     ;*
00167           523         ORG H#167
00167 00FFFE    524         DW  2-  ;WRITE GATE ENABLE
00168 00FFEF    525         DW  17- ;PLO GAP
00169 00FF4B    526         DW  180*    ;RECORD LENGTH (ONES COMPLEMENT)
0016A 00FFFB    527         DW  5-  ;DATA ECC
0016B 00FFFE    528         DW  2-  ;END OF RECORD PAD
                529     ;*
                530     ;* WRITE DATA
                531     ;*
                532     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
                533     ;* BLOCK SIZE = 1152/256
                534     ;*
00170           535         ORG H#170
00170 00FFFE    536         DW  2-  ;WRITE GATE ENABLE
00171 00FFF8    537         DW  8-  ;PLO GAP
00172 00FB7F    538         DW  1152*   ;RECORD LENGTH (ONES COMPLEMENT)
00173 00FFFB    539         DW  5-  ;DATA ECC
00174 00FFFE    540         DW  2-  ;END OF RECORD PAD
                541     ;*
                542     ;* WRITE DATA
                543     ;*
                544     ;* DRIVE TYPE = FUJI 2382 (DATA COPY DRIVE)
                545     ;* BLOCK SIZE = 1152/256
                546     ;*
00179           547         ORG H#179
00179 00FFFE    548         DW  2-  ;WRITE GATE ENABLE
0017A 00FFEF    549         DW  17- ;PLO GAP
0017B 00FB7F    550         DW  1152*   ;RECORD LENGTH (ONES COMPLEMENT)
0017C 00FFFB    551         DW  5-  ;DATA ECC
0017D 00FFFE    552         DW  2-  ;END OF RECORD PAD
```

```
 Addr      Line

                553         EJECT
                554     ;*
                555     ;* FORMAT
                556     ;*
                557     ;* DRIVE TYPE = FUJI 2344 (SW4)
                558     ;* BLOCK SIZE = 180/40
                559     ;*
00192           560         ORG H#192
00192 00FFF0    561         DW  16- ;HEAD SCATTER
00193 00FFFD    562         DW  3-  ;GAP/AM
00194 00FFEE    563         DW  18- ;PLO GAP
00195 00FFFA    564         DW  6-  ;HEADER DATA
00196 00FFFC    565         DW  4-  ;HEADER ECC
00197 00FFEB    566         DW  21- ;GAP 2
00198 00FF4C    567         DW  180-    ;(181) DATA AND SYNC (two's COMPLEMENT)
00199 00FFFB    568         DW  5-  ;DATA ECC
0019A 00FFF4    569         DW  12- ;WRITE/READ RECOVERY
                570     ;*
                571     ;* FORMAT
                572     ;*
                573     ;* DRIVE TYPE = FUJI 2344 (SW4)
                574     ;* BLOCK SIZE = 180/40
                575     ;*
0019B           576         ORG H#19B
0019B 00FFF0    577         DW  16- ;HEAD SCATTER
0019C 00FFFD    578         DW  3-  ;GAP/AM
0019D 00FFEE    579         DW  18- ;PLO GAP
0019E 00FFFA    580         DW  6-  ;HEADER DATA
0019F 00FFFC    581         DW  4-  ;HEADER ECC
001A0 00FFEB    582         DW  21- ;GAP 2
001A1 00FF4C    583         DW  180-    ;(181) DATA AND SYNC (two's COMPLEMENT)
001A2 00FFFB    584         DW  5-  ;DATA ECC
001A3 00FFF4    585         DW  12- ;WRITE/READ RECOVERY
```

```
Addr     Line
                  586          EJECT
                  587      ;*
                  588      ;* FORMAT
                  589      ;*
                  590      ;* DRIVE TYPE = FUJI 2333 (SW3)
                  591      ;* BLOCK SIZE = 180/40
                  592      ;*
001C8             593          ORG H#1C8
001C8 00FFF8      594          DW  8-   ;HEAD SCATTER
001C9 00FFFD      595          DW  3-   ;GAP/AM
001CA 00FFFA      596          DW  6-   ;PLO GAP
001CB 00FFFA      597          DW  6-   ;HEADER DATA
001CC 00FFFC      598          DW  4-   ;HEADER ECC
001CD 00FFEB      599          DW  21-  ;GAP 2
001CE 00FF4C      600          DW  180-     ;(181) DATA AND SYNC (two's COMPLEMENT)
001CF 00FFFB      601          DW  5-   ;DATA ECC
001D0 00FFF0      602          DW  16-  ;WRITE/READ RECOVERY
                  603      ;*
                  604      ;* FORMAT
                  605      ;*
                  606      ;* DRIVE TYPE = FUJI 2333 (SW3)
                  607      ;* BLOCK SIZE = 180/40
                  608      ;*
001D1             609          ORG H#1D1
001D1 00FFF8      610          DW  8-   ;HEAD SCATTER
001D2 00FFFD      611          DW  3-   ;GAP/AM
001D3 00FFFA      612          DW  6-   ;PLO GAP
001D4 00FFFA      613          DW  6-   ;HEADER DATA
001D5 00FFFC      614          DW  4-   ;HEADER ECC
001D6 00FFEB      615          DW  21-  ;GAP 2
001D7 00FF4C      616          DW  180-     ;(181) DATA AND SYNC (two's COMPLEMENT)
001D8 00FFFB      617          DW  5-   ;DATA ECC
001D9 00FFF0      618          DW  16-  ;WRITE/READ RECOVERY
```

```
Addr     Line

                619         EJECT
                620     ;*
                621     ;* FORMAT
                622     ;*
                623     ;* DRIVE TYPE = FUJI 2382 (SW5)
                624     ;* BLOCK SIZE = 180/40
                625     ;*
001DA           626         ORG H#1DA
001DA 00FFF8    627         DW  8-      ;HEAD SCATTER
001DB 00FFFD    628         DW  3-      ;GAP/AM
001DC 00FFF8    629         DW  8-      ;PLO GAP
001DD 00FFFA    630         DW  6-      ;HEADER DATA
001DE 00FFFC    631         DW  4-      ;HEADER ECC
001DF 00FFE7    632         DW  25-     ;GAP 2
001E0 00FF4C    633         DW  180-    ;(181) DATA AND SYNC (two's COMPLEMENT)
001E1 00FFFB    634         DW  5-      ;DATA ECC
001E2 00FFE6    635         DW  26-     ;WRITE/READ RECOVERY
                636     ;*
                637     ;* FORMAT
                638     ;*
                639     ;* DRIVE TYPE = FUJI 2382 (SW5)
                640     ;* BLOCK SIZE = 180/40
                641     ;*
001E3           642         ORG H#1E3
001E3 00FFF8    643         DW  8-      ;HEAD SCATTER
001E4 00FFFD    644         DW  3-      ;GAP/AM
001E5 00FFF8    645         DW  8-      ;PLO GAP
001E6 00FFFA    646         DW  6-      ;HEADER DATA
001E7 00FFFC    647         DW  4-      ;HEADER ECC
001E8 00FFE7    648         DW  25-     ;GAP 2
001E9 00FF4C    649         DW  180-    ;(181) DATA AND SYNC (two's COMPLEMENT)
001EA 00FFFB    650         DW  5-      ;DATA ECC
001EB 00FFE6    651         DW  26-     ;WRITE/READ RECOVERY
```

```
Addr     Line

                652         EJECT
                653     ;*
                654     ;* FORMAT
                655     ;*
                656     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
                657     ;* BLOCK SIZE = 1152/256
                658     ;*
001EC           659         ORG H#1EC
001EC 00FFF0    660         DW  16- ;HEAD SCATTER
001ED 00FFFD    661         DW  3-  ;GAP/AM
001EE 00FFF3    662         DW  13- ;PLO GAP
001EF 00FFFA    663         DW  6-  ;HEADER DATA
001F0 00FFFC    664         DW  4-  ;HEADER ECC
001F1 00FFF2    665         DW  14- ;GAP 2
001F2 00FB80    666         DW  1152-   ;(1153) DATA AND SYNC (two's COMPLEMENT)
001F3 00FFFB    667         DW  5-  ;DATA ECC
001F4 00FFF6    668         DW  10- ;WRITE/READ RECOVERY
                669     ;*
                670     ;* FORMAT
                671     ;*
                672     ;* DRIVE TYPE = FUJI 2382 (DATA COPY DRIVE)
                673     ;* BLOCK SIZE = 1152/256
                674     ;*
001F5           675         ORG H#1F5
001F5 00FFF8    676         DW  8-  ;HEAD SCATTER
001F6 00FFFD    677         DW  3-  ;GAP/AM
001F7 00FFF8    678         DW  8-  ;PLO GAP
001F8 00FFFA    679         DW  6-  ;HEADER DATA
001F9 00FFFC    680         DW  4-  ;HEADER ECC
001FA 00FFE6    681         DW  26- ;GAP 2
001FB 00FB80    682         DW  1152-   ;(1153) DATA AND SYNC (two's COMPLEMENT)
001FC 00FFFB    683         DW  5-  ;DATA ECC
001FD 00FFE7    684         DW  25- ;WRITE/READ RECOVERY
                685     ;
                686         END
```

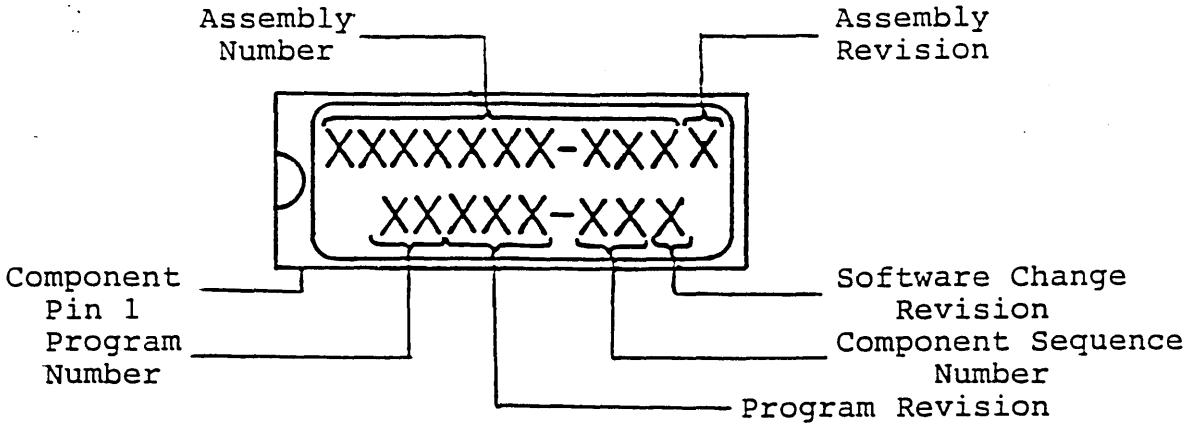
```
 DW              D                NARG      A 0000000
```

```
Assembly Phase complete.
    0 error(s) detected.
```

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO #2548 CR	7/25/89	[illegible]

Procedure:

1. Program component using data filed in software no. 29-A0-01A.
2. Make from unprogrammed part number 20012900.
3. Used on PCBA 1601494-101, 201, 202 Location U41.
   Used on PCBA 1602522-101 Location U73.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.
5. "Software Change Revision" is A.
4. "Component Sequence Number" is 01.
3. "Program Number" is 29 Revision -A0.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	5/15/89
CHECKER	
OTHER	
APPROVED	

CONFIDENTIAL DOCUMENT
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amperif memory products

PROM ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601611-001	1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PN 1601611-001

SID 29-A0-01A

EXP MEM STACK PROM

$A0000.

71 91 80 D6 A0 A0 80 80 D6 D6 80 80 A0 A0 80 80

B8 D0 80 80 80 F8 80 D0 80 80 B8 D0 80 80 80 80

$S137C.

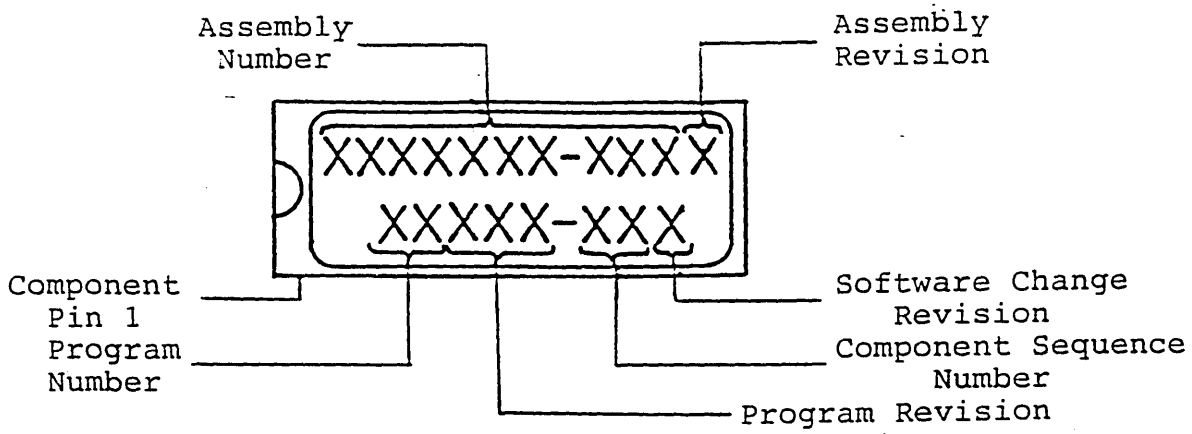
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
F	REVISED & REDRAWN - SEE ECO # 1935	5/18/88	

Procedure:

1. Program component using data filed in software no. 26DA0-01 B.

2. Make from unprogrammed part number 20071299.

3. Used on PCBA 1120010-201,202 Location AA01.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is B.

4. "Component Sequence Number" is 01.

3. "Program Number" is 26 Revision DA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
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CHECKER	
OTHER	
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amperif memory products

PROM ASSEMBLY,

XMCIP CONTROL 3

REV F

SIZE	DRAWING NO.	SHEET
A	1601415-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PROGRAM FOR XMCIP CONTROL 3 PROM

```
EC EC EC EC 8E EC EC 9E 7C 7C FC 7C EC EC EC EC
ED EE FC FC CC AC 7C EC 7C FC EC EC EC EC EC EC
EC EC EC EC EC EC EC EC EC EC EC EC EC EC EC EC
EC EC EC EC EC EC EC EC EC EC EC EC EC EC EC EC
EC EC EC EC EC EC EC EC EC EC EC EC EC EC EC EC
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FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
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FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
```

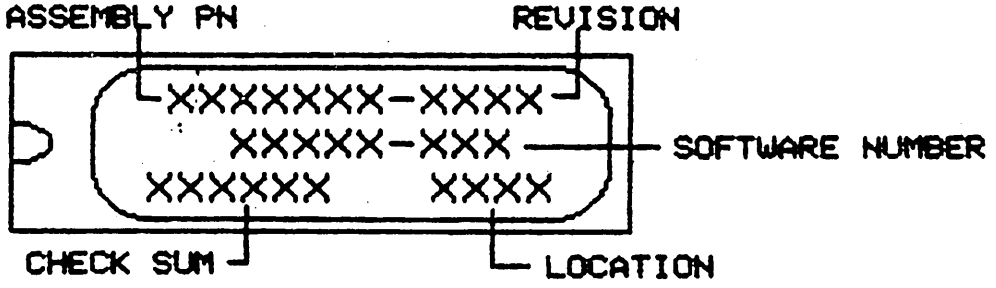
ASSEMBLY NUMBER 1601415-001
SOFTWARE NUMBER 26DA0-01B

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD. REL. ECO 3071	12-5-89	MMcA
B	INC PER ECO 3149	1-19-90	MMcA

PROCEDURE :

1. ASSEMBLY PART NUMBER IS 1602962-101.
2. SEE SEPARATE PARTS LIST.
3. PROGRAM COMPONENT USING DATA FILED IN SOFTWARE NO. 22FB1-01A.
4. MAKE FROM UNPROGRAMMED AMPERIF PART NUMBER 20131900-0011.
   VENDOR PN AM27512DC ; DESCRIPTION IC,EPROM,64K×8,70NS,NMOS.
5. USED ON PCBA 1601495-131 LOCATION U3.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.



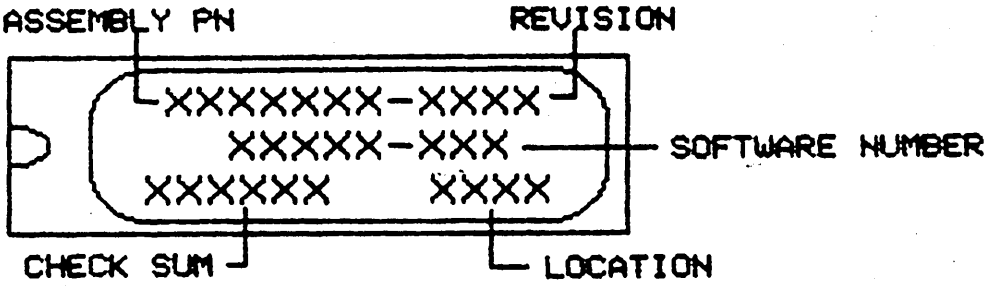
6. "PROGRAM NUMBER" IS 22 REVISION FB1.
7. "COMPONENT SEQUENCE NUMBER" IS 01.
8. "SOFTWARE CHANGE REVISION" IS A.
9. CHECK SUM IS 8AA667.
10. IDENTIFY ON ADHESIVE-BACKED LABEL AS SHOWN AND AFFIX LABEL TO PROGRAMMED PART PER DRAWING ABOVE.

DOCUMENT RELEASE	DATE		
ENGINEERING Bruce Olson	11/20/89	CONFIDENTIAL DOCUMENT ALL PROHIBITIONS APPLY. amperif	
DRAFTSPERSON Cheryl Reynolds	11/9/9		
CHECKER [illegible]	11/17/89	DESCRIPTION PROM ASSEMBLY, XMILKP OP SYS	REV B
OTHER			
APPROVED John G. Walker	11-20-89	SIZE A / DRAWING NUMBER 1602962-101	SHT 1 OF 1

REVISION				
LTR	DESCRIPTION		DATE	APPROVED
A	PROD. REL. ECO 3071	JB	12-5-89	M Mack
B	UPDATE - ECO 3129	CR	1-16-90	C Reynolds
C	INC PER ECO 3149	CR	1-16-90	C Reynolds

PROCEDURE :

1. ASSEMBLY PART NUMBER IS 1602962-102.
2. SEE SEPARATE PARTS LIST.
3. PROGRAM COMPONENT USING DATA FILED IN SOFTWARE NO. 22FB1-02B.
4. MAKE FROM UNPROGRAMMED AMPERIF PART NUMBER 20131900-001.
   VENDOR PN AM27512DC ; DESCRIPTION IC, EPROM, 64K×8, 70NS, NMOS.
5. USED ON PCBA 1601495-131 LOCATION U4.
   USED ON PCBA _____ LOCATION _____.
   USED ON PCBA _____ LOCATION _____.



6. "PROGRAM NUMBER" IS 22 REVISION FB1.
7. "COMPONENT SEQUENCE NUMBER" IS 02.
8. "SOFTWARE CHANGE REVISION" IS B.
9. CHECK SUM IS EE3E10.
10. IDENTIFY ON ADHESIVE-BACKED LABEL AS SHOWN AND AFFIX LABEL TO PROGRAMMED PART PER DRAWING ABOVE.

DOCUMENT RELEASE	DATE
ENGINEERING Bruce Ava	11/20/89
DRAFTSPERSON Cheryl Reynolds	11/9/9
CHECKER J Sears	11/17/89
OTHER	
APPROVED John G. Walker	11-20-89

CONFIDENTIAL DOCUMENT
ALL PROHIBITIONS
APPLY.

amperif

DESCRIPTION	REV
PROM ASSEMBLY, XM16KP OP SYS	C

SIZE	DRAWING NUMBER	SHT	OF
A	1602962-102	1	1

```
Addr  Line

      1   ;
      2   ;
      3   ;       DIFP Drive Constant PROMS
      4   ;       MSB = DF52      LSB = DF38 (OLD DIFP)
      5   ;       MSB = U105      LSB = U125 (NEW DIFP)
      6   ;
      7   ;       Date: 09-JUN-89
      8   ;
      9   ;       For CDC word prep length of 116 and 456 words/record.
     10   ;       This file has the hard and soft sector constant values.
     11   ;
     12   ;                 Drive Pointer Index Table
     13   ;
     14   ;       Addr      Drive Type          Size          Type Number
     15   ;
     16   ;       000       Drive not defined
     17   ;       012       Fujitsu M2344 (SW4) 690 MB.............5
     18   ;                 [116 prep] 1=12, 2=96, 3=116, 4=192
     19   ;                 [456 prep] 1=1B, 2=9F, 3=11F, 4=19B
     20   ;
     21   ;       024       Drive not defined
     22   ;
     23   ;       036       Drive not defined
     24   ;
     25   ;       048       Fujitsu M2333 (SW3) 337 MB.............3
     26   ;                 [116 prep] 1=48, 2=CC, 3=14C, 4=1C8
     27   ;                 [456 prep] 1=51, 2=D5, 3=155, 4=1D1
     28   ;
     29   ;       05A       Fujitsu M2382 (SW5) 1.02 GB............4
     30   ;                 [116 prep] 1=5A, 2=DE, 3=15E, 4=1DA
     31   ;                 [456 prep] 1=63, 2=E7, 3=167, 4=1E3
     32   ;
     33   ;       06C       MPI 9720            337 MB.........data copy
     34   ;                 [256 prep] 1=6C, 2=F0, 3=170, 4=1EC
     35   ;
     36   ;       075       Fujitsu M2333 (SW3) 337 MB.........data copy
     37   ;                 [256 prep] 1=75, 2=F9, 3=179, 4=1F5
     38   ;
     39   ;     Legend: 1 = Read Header
     40   ;             2 = Read Data
     41   ;             3 = Write Data
     42   ;             4 = Format
     43   ;
```

CDC 7001 SABER 5 XMC OP SYS
PN 1602962-101 AND 102
SID 22FB1 (REV A)

```
Addr    Line

        44          EJECT
        45      ;*****************************************************
        46      ;   The values below were calculated with the following   *
        47      ;   equations.                                            *
        48      ;                                                         *
        49      ;   1. data bytes/words per formatted record:             *
        50      ;      bytes = (bytes/record - overhead bytes/record)     *
        51      ;      words = (bytes/record div.by 4.5)                  *
        52      ;   2. data bytes/track = (records/track * data           *
        53      ;                                        bytes/record)    *
        54      ;   3. data words/track = ((data bytes /record *          *
        55      ;                       records/track) * div.by 4.5)      *
        56      ;                                                         *
        57      ;   4. data words/cylinder  = (data words/track *         *
        58      ;                                 tracks/cylinder)        *
        59      ;   5. records/track = ((bytes/track div.by               *
        60      ;                                 bytes/record) -1)       *
        61      ;   6. record time = (bytes/record * byte time)           *
        62      ;   7. % of formmatted track utilization = ((data         *
        63      ;       bytes/record * records/track) div.by bytes/track) *
        64      ;                                                         *
        65      ;*********************************************************
```

```
Addr    Line

          66        EJECT
          67    ;*****************************************************
          68    ;*         Fujitsu M2333 (SW3) 337 MB  drive type #3     *
          69    ;*****************************************************
          70    ;*                                                       *
          71    ;* bytes/words per record:...522/116                     *
          72    ;*                                                       *
          73    ;* write to read recovery time = 3.77 usec = 24 bytes    *
          74    ;* total bytes per record:.................592           *
          75    ;* total bytes per track:..............40,960           *
          76    ;* records per track:.....................67            *
          77    ;* bytes per track used:..............39,664           *
          78    ;* byte time (nano secs.):................406           *
          79    ;* record time (usec.s)...................240.4          *
          80    ;* % of formatted track utilization.....88.2           *
          81    ;* words per track:.....................7,772           *
          82    ;* tracks per cylinder:....................10           *
          83    ;* words per cylinder:................77,720           *
          84    ;* overhead per record (bytes):.............70          *
          85    ;*                                                       *
          86    ;*     sector switch setting                             *
          87    ;*      SW1                SW2                           *
          88    ;* 1 2 3 4 5 6 7      1 2 3 4 5 6 7                      *
          89    ;* ---------------    ---------------                    *
          90    ;* 0 1 1 1 0 1 0      0 1 0 0 0 0 0                      *
          91    ;*                                                       *
          92    ;*****************************************************
```

```
Addr    Line

          93        EJECT
          94      ;*****************************************************************
          95      ;*          Fujitsu M2333 (SW3) 337 MB  drive type #3            *
          96      ;*****************************************************************
          97      ;*                                                               *
          98      ;* bytes/words per record:...2052/456                            *
          99      ;*                                                               *
         100      ;* total bytes per record:.................2,122                *
         101      ;* total bytes per track:................40,960                *
         102      ;* records per track:.......................19                   *
         103      ;* bytes per track used:................40,318                   *
         104      ;* byte time (nano secs.):..................406                  *
         105      ;* record time (usec.s).....................861.5                 *
         106      ;* % of formatted track utilization.........96.7                 *
         107      ;* words per track:.....................8,664                    *
         108      ;* tracks per cylinder:.....................10                   *
         109      ;* words per cylinder:..................86,640                    *
         110      ;* overhead per record (bytes):.............70                   *
         111      ;*                                                               *
         112      ;*      sector switch setting                                    *
         113      ;*       SW1                 SW2                                 *
         114      ;* 1 2 3 4 5 6 7       1 2 3 4 5 6 7                            *
         115      ;* ---------------     ---------------                          *
         116      ;* 0 1 0 1 0 1 0       0 0 0 1 0 0 0                            *
         117      ;*                                                               *
         118      ;*****************************************************************
```

```
Addr    Line

        119         EJECT
        120     ;*****************************************************************
        121     ;*          Fujitsu M2344 (SW4)  690 MB  drive type #5           *
        122     ;*****************************************************************
        123     ;*                                                               *
        124     ;* bytes/words per record:...522/116                             *
        125     ;*                                                               *
        126     ;* write to read recovery time = 10.55 usec = 26 bytes           *
        127     ;* total bytes per record:.................609                   *
        128     ;* total bytes per track:..............40,960                    *
        129     ;* records per track:.....................67                      *
        130     ;* bytes per track used:...............40,803                    *
        131     ;* byte time (nano secs.):................406                     *
        132     ;* record time (usec.s)...................247.3                   *
        133     ;* % of formatted track utilization.........85.7                 *
        134     ;* words per track:.....................7772                     *
        135     ;* tracks per cylinder:...................27                      *
        136     ;* words per cylinder:................209,844                    *
        137     ;* overhead per record (bytes):.............70                   *
        138     ;*                                                               *
        139     ;* sector switch setting                                         *
        140     ;*      SW1                 SW2                                  *
        141     ;* 1 2 3 4 5 6 7      1 2 3 4 5 6 7                              *
        142     ;* ---------------    ---------------                            *
        143     ;* 0 1 1 1 0 1 0      0 1 0 0 0 0 0                              *
        144     ;*                                                               *
        145     ;*****************************************************************
        146     ;* bytes/words per record:...2052/456                            *
        147     ;*                                                               *
        148     ;* total bytes per record:..............2,138                    *
        149     ;* total bytes per track:..............40,960                    *
        150     ;* records per track:.....................19                      *
        151     ;* bytes per track used:...............40,622                    *
        152     ;* byte time (nano secs.):................406                     *
        153     ;* record time (usec.s)...................868.0                   *
        154     ;* % of formatted track utilization.........95.98                *
        155     ;* words per track:.....................8,664                    *
        156     ;* tracks per cylinder:...................27                      *
        157     ;* words per cylinder:................233,928                    *
        158     ;* overhead per record (bytes):.............70                   *
        159     ;*                                                               *
        160     ;* sector switch setting same as 522/116 blocking factor         *
        161     ;*****************************************************************
```

```
Addr    Line

        162         EJECT
        163     ;*****************************************************************
        164     ;*      Fujitsu M2382 (SW5)  1.02 GB drive type #3               *
        165     ;*****************************************************************
        166     ;*                                                               *
        167     ;* bytes/words per record:....522/116                            *
        168     ;*                                                               *
        169     ;* write to read recovery time = 11.32 usec = 34 bytes           *
        170     ;* total bytes per record:.................608                   *
        171     ;* total bytes per track:..............49,728                    *
        172     ;* records per track:.....................80                     *
        173     ;* bytes per track used:..............48,640                     *
        174     ;* byte time (nano secs.):................333                    *
        175     ;* record time (usec.s):..................202.5                  *
        176     ;* % of formatted track utilization.........97.8                 *
        177     ;* words per track:.....................9280                     *
        178     ;* tracks per cylinder:....................27                     *
        179     ;* words per cylinder:................250,560                    *
        180     ;* overhead per record (bytes):.............86                   *
        181     ;*                                                               *
        182     ;*             sector switch setting                             *
        183     ;*             SW4                SW5                            *
        184     ;*       7 6 5 4 3 2 1      7 6 5 4 3 2 1                        *
        185     ;*       -------------      -------------                        *
        186     ;*       0 1 1 0 1 0 1      0 0 0 0 0 1 0                        *
        187     ;*                                                               *
        188     ;*       SW1-5 = 0/HARD SECTOR MODE                              *
        189     ;*                                                               *
        190     ;*                                                               *
        191     ;*****************************************************************
```

```
Addr    Line

        192      EJECT
        193     ;*****************************************************************
        194     ;*      Fujitsu M2382 (SW5)  1.02 GB drive type #3               *
        195     ;*****************************************************************
        196     ;*                                                               *
        197     ;* bytes/words per record:..2052/456                             *
        198     ;*                                                               *
        199     ;* total bytes per record:.............2,138                     *
        200     ;* total bytes per track:.............49,728                     *
        201     ;* records per track:.....................23                     *
        202     ;* bytes per track used:..............49,174                     *
        203     ;* byte time (nano secs.):................333                     *
        204     ;* record time (usec.s)...................711.9                   *
        205     ;* % of formatted track utilization.....98.0                     *
        206     ;* words per track:....................10,488                    *
        207     ;* tracks per cylinder:....................27                     *
        208     ;* words per cylinder:................283,176                    *
        209     ;* overhead per record (bytes):.............86                   *
        210     ;*                                                               *
        211     ;*            SW4                 SW5                            *
        212     ;*       7 6 5 4 3 2 1       7 6 5 4 3 2 1                       *
        213     ;*       -------------       -------------                       *
        214     ;*       0 1 1 0 0 1 0       0 0 0 1 0 0 0                       *
        215     ;*                                                               *
        216     ;*       SW1-5 = 0/HARD SECTOR MODE                              *
        217     ;*                                                               *
        218     ;*                                                               *
        219     ;*****************************************************************
```

```
Addr    Line

        220         EJECT
        221     ;*****************************************************************
        222     ;*          CDC 368   337 MB data copy drive                     *
        223     ;*****************************************************************
        224     ;*                                                               *
        225     ;* bytes/words per record:..1152/256                             *
        226     ;*                                                               *
        227     ;* write to read recovery time = 12.67 usec = 23 bytes           *
        228     ;* total bytes per record:.............1,224                     *
        229     ;* total bytes per track:.............30,240                     *
        230     ;* records per track:.....................24                     *
        231     ;* bytes per track used:..............39,376                     *
        232     ;* byte time (nano secs.):..............551.2                     *
        233     ;* record time (usec.s).................674.7                     *
        234     ;* % of formatted track utilization.....94.1                     *
        235     ;* words per track:....................6,144                     *
        236     ;* tracks per cylinder:...................10                     *
        237     ;* words per cylinder:................61,440                     *
        238     ;* overhead per record (bytes):.............72                   *
        239     ;*                                                               *
        240     ;*     sector switch setting                                     *
        241     ;*      SW1                SW2                                   *
        242     ;* 1 2 3 4 5 6 7      1 2 3 4 5 6 7                              *
        243     ;* -------------      -------------                              *
        244     ;* X X X X X X X      X X X X X X X                              *
        245     ;*****************************************************************
        246     ;*        Fujitsu M2333 (SW3) 337 MB data copy drive             *
        247     ;*****************************************************************
        248     ;*                                                               *
        249     ;* bytes/words per record:...1152/256                            *
        250     ;*                                                               *
        251     ;* total bytes per record:.............1,222                     *
        252     ;* total bytes per track:.............40,960                     *
        253     ;* records per track:....................33                     *
        254     ;* bytes per track used:..............40,326                     *
        255     ;* byte time (nano secs.):..............406                     *
        256     ;* record time (usec.s).................496.1                     *
        257     ;* % of formatted track utilization.....94.3                     *
        258     ;* words per track:....................8,448                     *
        259     ;* tracks per cylinder:...................10                     *
        260     ;* words per cylinder:................84,480                     *
        261     ;* overhead per record (bytes):.............70                   *
        262     ;*                                                               *
        263     ;* sector switch setting is a don't care                         *
        264     ;*****************************************************************
```

```
 Addr        Line

             265        EJECT
             266    ;*************************************************************
             267    ;*
             268    ;* READ HEADER
             269    ;*
             270    ;* DRIVE TYPE = GENERIC
             271    ;* BLOCK SIZE = N/A
             272    ;*
00000        273        ORG H#00
00000 00FFFE 274        DW  2-    ;PLO TO SYNC DELAY
00001 00FFD8 275        DW  40-   ;SYNC WINDOW
00002 00FFFB 276        DW  5-      ;OF HEADER DATA
00003 00FFFC 277        DW  4-      ;HEADER ECC
00004 00FFFE 278        DW  2-      ;READ/WRITE PAD
             279    ;*
             280    ;* READ HEADER
             281    ;*
             282    ;* DRIVE TYPE = GENERIC
             283    ;* BLOCK SIZE = N/A
             284    ;*
00009        285        ORG H#09
00009 00FFFB 286        DW  5-    ;PLO TO SYNC DELAY
0000A 00FFEC 287        DW  20-   ;SYNC WINDOW
0000B 00FFFB 288        DW  5-      ;OF HEADER DATA
0000C 00FFFC 289        DW  4-      ;HEADER ECC
0000D 00FFFE 290        DW  2-      ;READ/WRITE PAD
             291    ;*
             292    ;* READ HEADER
             293    ;*
             294    ;* DRIVE TYPE = FUJI 2344 (SW4)
             295    ;* BLOCK SIZE = 522/116
             296    ;*
00012        297        ORG H#12
00012 00FFF6 298        DW  10-   ;PLO TO SYNC DELAY
00013 00FFE4 299        DW  28-   ;SYNC WINDOW
00014 00FFFB 300        DW  5-      ;OF HEADER DATA
00015 00FFFC 301        DW  4-      ;HEADER ECC
00016 00FFFE 302        DW  2-      ;READ/WRITE PAD
             303    ;
             304    ;*
             305    ;* READ HEADER
             306    ;*
             307    ;* DRIVE TYPE = FUJI 2344 (SW4)
             308    ;* BLOCK SIZE = 2052/456
             309    ;*
0001B        310        ORG H#1B
0001B 00FFF6 311        DW  10-   ;PLO TO SYNC DELAY
0001C 00FFE4 312        DW  28-   ;SYNC WINDOW
0001D 00FFFB 313        DW  5-      ;OF HEADER DATA
0001E 00FFFC 314        DW  4-      ;HEADER ECC
0001F 00FFFE 315        DW  2-      ;READ/WRITE PAD
             316    ;*
             317    ;* READ HEADER
             318    ;*
             319    ;* DRIVE TYPE = CDC 1.2 GIGABYTE (SABER)
```

```
 Addr        Line

             320    ;* BLOCK SIZE = 522/116
             321    ;*
 )36         322       ORG   H#36
00036 00FFFB 323        DW  5-   ;PLO TO SYNC DELAY
00037 00FFF0 324        DW  16-  ;SYNC WINDOW
00038 00FFFB 325        DW  5-      ;OF HEADER DATA
00039 00FFFC 326        DW  4-      ;HEADER ECC
0003A 00FFFC 327        DW  4-      ;READ/WRITE PAD
             328    ;* ...
             329    ;* READ HEADER
             330    ;*
             331    ;* DRIVE TYPE = FUJI 2333 (SW3)
             332    ;* BLOCK SIZE = 522/116
             333    ;*
 )48         334        ORG H#48
00048 00FFFE 335        DW  2-      ;PLO TO SYNC DELAY
00049 00FFD0 336        DW  48-  ;SYNC WINDOW
0004A 00FFFB 337        DW  5-      ;OF HEADER DATA
0004B 00FFFC 338        DW  4-      ;HEADER ECC
0004C 00FFFE 339        DW  2-      ;READ/WRITE PAD
             340    ;
             341    ;*
             342    ;* READ HEADER
             343    ;*
             344    ;* DRIVE TYPE = FUJI 2333 (SW3)
             345    ;* BLOCK SIZE = 2052/456
             346    ;*
 )51         347        ORG H#51
00051 00FFFE 348        DW  2-      ;PLO TO SYNC DELAY
00052 00FFD0 349        DW  48-  ;SYNC WINDOW
00053 00FFFB 350        DW  5-      ;OF HEADER DATA
00054 00FFFC 351        DW  4-      ;HEADER ECC
00055 00FFFE 352        DW  2-      ;READ/WRITE PAD
```

```
Addr        Line

            353         EJECT
            354     ;*
            355     ;* READ HEADER
            356     ;*
            357     ;* DRIVE TYPE = FUJI 2382 (SW5)
            358     ;* BLOCK SIZE = 522/116
            359     ;*
0005A       360         ORG H#5A
0005A 00FFFE 361        DW  2-      ;PLO TO SYNC DELAY
0005B 00FFD0 362        DW  48-  ;SYNC WINDOW
0005C 00FFFB 363        DW  5-      ;OF HEADER DATA
0005D 00FFFC 364        DW  4-      ;HEADER ECC
0005E 00FFFC 365        DW  4-      ;READ/WRITE PAD
            366     ;
            367     ;*
            368     ;* READ HEADER
            369     ;*
            370     ;* DRIVE TYPE = FUJI 2382 (SW5)
            371     ;* BLOCK SIZE = 2052/456
            372     ;*
00063       373         ORG H#63
00063 00FFFE 374        DW  2-      ;PLO TO SYNC DELAY
00064 00FFD0 375        DW  48-  ;SYNC WINDOW
00065 00FFFB 376        DW  5-      ;OF HEADER DATA
00066 00FFFC 377        DW  4-      ;HEADER ECC
00067 00FFFC 378        DW  4-      ;READ/WRITE PAD
            379     ;*
            380     ;* READ HEADER
            381     ;*
            382     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
            383     ;* BLOCK SIZE = 1152/256
            384     ;*
0006C       385         ORG H#6C
0006C 00FFF7 386        DW  9-      ;PLO TO SYNC DELAY
0006D 00FFF0 387        DW  16-    ;SYNC WINDOW
0006E 00FFFB 388        DW  5-      ;OF HEADER DATA
0006F 00FFFC 389        DW  4-      ;HEADER ECC
00070 00FFFE 390        DW  2-      ;READ/WRITE PAD
            391     ;
            392     ;*
            393     ;* READ HEADER
            394     ;*
            395     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
            396     ;* BLOCK SIZE = 1152/256
            397     ;*
00075       398         ORG H#75
00075 00FFFE 399        DW  2-      ;PLO TO SYNC DELAY
00076 00FFD0 400        DW  48-  ;SYNC WINDOW
00077 00FFFB 401        DW  5-      ;OF HEADER DATA
00078 00FFFC 402        DW  4-      ;HEADER ECC
00079 00FFFE 403        DW  2-      ;READ/WRITE PAD
```

```
 Addr        Line

                404         EJECT
                405     ;*
                406     ;* READ DATA
                407     ;*
                408     ;* DRIVE TYPE = FUJI 2344 (SW4)
                409     ;* BLOCK SIZE = 522/116
                410     ;*
00096           411         ORG H#096
00096 00FFFE    412         DW  2-      ;READ GATE ENABLE
00097 00FFD0    413         DW  48-  ;PLO GAP  TO SYNC
00098 00FDF5    414         DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
00099 00FFFC    415         DW  4-      ;DATA ECC
0009A 00FFFE    416         DW  2-      ;READ/WRITE PAD
                417     ;
                418     ;*
                419     ;* READ DATA
                420     ;*
                421     ;* DRIVE TYPE = FUJI 2344 (SW4)
                422     ;* BLOCK SIZE = 2052/456
                423     ;*
0009F           424         ORG H#09F
0009F 00FFFE    425         DW  2-      ;READ GATE ENABLE
000A0 00FFD0    426         DW  48-  ;PLO GAP  TO SYNC
000A1 00F7FB    427         DW  2052*    ;RECORD LENGTH (ONES COMPLEMENT)
000A2 00FFFC    428         DW  4-      ;DATA ECC
000A3 00FFFE    429         DW  2-      ;READ/WRITE PAD
                430     ;*
                431     ;* READ DATA
                432     ;*
                433     ;* DRIVE TYPE = CDC 1.2 GIGABYTE (SABER)
                434     ;* BLOCK SIZE = 522/116
                435     ;*
000BA           436         ORG H#0BA
000BA 00FFFE    437         DW  2-      ;READ GATE ENABLE
000BB 00FFE0    438         DW  32-  ;PLO GAP  TO SYNC
000BC 00FDF5    439         DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
000BD 00FFFC    440         DW  4-      ;DATA ECC
000BE 00FFFE    441         DW  2-      ;READ/WRITE PAD
                442     ;*
                443     ;* READ DATA
                444     ;*
                445     ;* DRIVE TYPE = FUJI 2333 (SW3)
                446     ;* BLOCK SIZE = 522/116
                447     ;*
000CC           448         ORG H#0CC
000CC 00FFFE    449         DW  2-      ;READ GATE ENABLE
000CD 00FFD0    450         DW  48-  ;PLO GAP  TO SYNC
000CE 00FDF5    451         DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
000CF 00FFFC    452         DW  4-      ;DATA ECC
000D0 00FFFE    453         DW  2-      ;READ/WRITE PAD
                454     ;
                455     ;*
                456     ;* READ DATA
                457     ;*
                458     ;* DRIVE TYPE = FUJI 2333 (SW3)
```

```
 Addr        Line

                459     ;* BLOCK SIZE = 2052/456
                460     ;*
00D5            461         ORG H#0D5
00D5 00FFFE     462         DW  2-      ;READ GATE ENABLE
00D6 00FFD0     463         DW  48-  ;PLO GAP  TO SYNC
00D7 00F7FB     464         DW  2052*    ;RECORD LENGTH (ONES COMPLEMENT)
00D8 00FFFC     465         DW  4-      ;DATA ECC
00D9 00FFFE     466         DW  2-      ;READ/WRITE PAD
```

```
Addr        Line

            467         EJECT
            468     ;*
            469     ;* READ DATA
            470     ;*
            471     ;* DRIVE TYPE = FUJI 2382 (SW5)
            472     ;* BLOCK SIZE = 522/116
            473     ;*
000DE       474         ORG H#0DE
000DE 00FFFE 475        DW  2-      ;READ GATE ENABLE
000DF 00FFD0 476        DW  48-  ;PLO GAP  TO SYNC
000E0 00FDF5 477        DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
000E1 00FFFC 478        DW  4-      ;DATA ECC
000E2 00FFFE 479        DW  2-      ;READ/WRITE PAD
            480     ;
            481     ;*
            482     ;* READ DATA
            483     ;*
            484     ;* DRIVE TYPE = FUJI 2382 (SW5)
            485     ;* BLOCK SIZE = 2052/456
            486     ;*
000E7       487         ORG H#0E7
000E7 00FFFE 488        DW  2-      ;READ GATE ENABLE
000E8 00FFD0 489        DW  48-  ;PLO GAP  TO SYNC
000E9 00F7FB 490        DW  2052*    ;RECORD LENGTH (ONES COMPLEMENT)
000EA 00FFFC 491        DW  4-      ;DATA ECC
000EB 00FFFE 492        DW  2-      ;READ/WRITE PAD
            493     ;*
            494     ;* READ DATA
            495     ;*
            496     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
            497     ;* BLOCK SIZE = 1152/256
            498     ;*
000F0       499         ORG H#0F0
000F0 00FFFE 500        DW  2-      ;READ GATE ENABLE
000F1 00FFE0 501        DW  32-  ;PLO GAP  TO SYNC
000F2 00FB7F 502        DW  1152*    ;RECORD LENGTH (ONES COMPLEMENT)
000F3 00FFFC 503        DW  4-      ;DATA ECC
000F4 00FFFE 504        DW  2-      ;READ/WRITE PAD
            505     ;
            506     ;*
            507     ;* READ DATA
            508     ;*
            509     ;* DRIVE TYPE = FUJI 2333 (DATA COPY DRIVE)
            510     ;* BLOCK SIZE = 1152/256
            511     ;*
000F9       512         ORG H#0F9
000F9 00FFFE 513        DW  2-      ;READ GATE ENABLE
000FA 00FFD0 514        DW  48-  ;PLO GAP  TO SYNC
000FB 00FB7F 515        DW  1152*    ;RECORD LENGTH (ONES COMPLEMENT)
000FC 00FFFC 516        DW  4-      ;DATA ECC
000FD 00FFFE 517        DW  2-      ;READ/WRITE PAD
```

```
 Addr      Line

                518         EJECT
                519     ;*
                520     ;* WRITE DATA
                521     ;*
                522     ;* DRIVE TYPE = FUJI 2344 (SW4)
                523     ;* BLOCK SIZE = 522/116
                524     ;*
00116           525         ORG H#116
00116 00FFFE    526         DW  2-      ;WRITE GATE ENABLE
00117 00FFF1    527         DW  15-  ;PLO GAP
00118 00FDF5    528         DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
00119 00FFFB    529         DW  5-      ;DATA ECC
0011A 00FFFE    530         DW  2-      ;END OF RECORD PAD
                531     ;*
                532     ;* WRITE DATA
                533     ;*
                534     ;* DRIVE TYPE = FUJI 2344 (SW4)
                535     ;* BLOCK SIZE = 2052/456
                536     ;*
0011F           537         ORG H#11F
0011F 00FFFE    538         DW  2-      ;WRITE GATE ENABLE
00120 00FFF1    539         DW  15-  ;PLO GAP
00121 00F7FB    540         DW  2052*    ;RECORD LENGTH (ONES COMPLEMENT)
00122 00FFFB    541         DW  5-      ;DATA ECC
00123 00FFFE    542         DW  2-      ;END OF RECORD PAD
                543     ;*
                544     ;* WRITE DATA
                545     ;*
                546     ;* DRIVE TYPE = CDC 1.2 GIGABYTE (SABER)
                547     ;* BLOCK SIZE = 522/116
                548     ;*
0013A           549         ORG H#13A
0013A 00FFFE    550         DW  2-      ;WRITE GATE ENABLE
0013B 00FFF6    551         DW  10-  ;PLO GAP
0013C 00FDF5    552         DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
0013D 00FFFB    553         DW  5-      ;DATA ECC
0013E 00FFFE    554         DW  2-      ;END OF RECORD PAD
                555     ;*
                556     ;* WRITE DATA
                557     ;*
                558     ;* DRIVE TYPE = FUJI 2333 (SW3)
                559     ;* BLOCK SIZE = 522/116
                560     ;*
0014C           561         ORG H#14C
0014C 00FFFE    562         DW  2-      ;WRITE GATE ENABLE
0014D 00FFF1    563         DW  15-  ;PLO GAP
0014E 00FDF5    564         DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
0014F 00FFFB    565         DW  5-      ;DATA ECC
00150 00FFFE    566         DW  2-      ;END OF RECORD PAD
                567     ;*
                568     ;* WRITE DATA
                569     ;*
                570     ;* DRIVE TYPE = FUJI 2333 (SW3)
                571     ;* BLOCK SIZE = 2052/456
                572     ;*
```

```
 Addr        Line

00155         573        ORG H#155
00155 00FFFE  574        DW  2-       ;WRITE GATE ENABLE
00156 00FFF1  575        DW  15-  ;PLO GAP
00157 00F7FB  576        DW  2052*     ;RECORD LENGTH (ONES COMPLEMENT)
00158 00FFFB  577        DW  5-       ;DATA ECC
00159 00FFFE  578        DW  2-       ;END OF RECORD PAD
```

```
Addr        Line

            579         EJECT
            580     ;*
            581     ;* WRITE DATA
            582     ;*
            583     ;* DRIVE TYPE = FUJI 2382 (SW5)
            584     ;* BLOCK SIZE = 522/116
            585     ;*
0015E       586         ORG H#15E
0015E 00FFFE 587        DW  2-      ;WRITE GATE ENABLE
0015F 00FFEF 588        DW  17-  ;PLO GAP
00160 00FDF5 589        DW  522*     ;RECORD LENGTH (ONES COMPLEMENT)
00161 00FFFB 590        DW  5-      ;DATA ECC
00162 00FFFE 591        DW  2-      ;END OF RECORD PAD
            592     ;*
            593     ;* WRITE DATA
            594     ;*
            595     ;* DRIVE TYPE = FUJI 2382 (SW5)
            596     ;* BLOCK SIZE = 2052/456
            597     ;*
00167       598         ORG H#167
00167 00FFFE 599        DW  2-      ;WRITE GATE ENABLE
00168 00FFEF 600        DW  17-  ;PLO GAP
00169 00F7FB 601        DW  2052*    ;RECORD LENGTH (ONES COMPLEMENT)
0016A 00FFFB 602        DW  5-      ;DATA ECC
0016B 00FFFE 603        DW  2-      ;END OF RECORD PAD
            604     ;*
            605     ;* WRITE DATA
            606     ;*
            607     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
            608     ;* BLOCK SIZE = 1152/256
            609     ;*
00170       610         ORG H#170
00170 00FFFE 611        DW  2-     ;WRITE GATE ENABLE
00171 00FFF8 612        DW  8-      ;PLO GAP
00172 00FB7F 613        DW  1152*    ;RECORD LENGTH (ONES COMPLEMENT)
00173 00FFFB 614        DW  5-      ;DATA ECC
00174 00FFFE 615        DW  2-      ;END OF RECORD PAD
            616     ;*
            617     ;* WRITE DATA
            618     ;*
            619     ;* DRIVE TYPE = FUJI 2333 (DATA COPY DRIVE)
            620     ;* BLOCK SIZE = 1152/256
            621     ;*
00179       622         ORG H#179
00179 00FFFE 623        DW  2-      ;WRITE GATE ENABLE
0017A 00FFF1 624        DW  15-  ;PLO GAP
0017B 00F7FB 625        DW  2052*    ;RECORD LENGTH (ONES COMPLEMENT)
0017C 00FFFB 626        DW  5-      ;DATA ECC
0017D 00FFFE 627        DW  2-      ;END OF RECORD PAD
```

```
Addr        Line

            628         EJECT
            629     ;*
            630     ;* FORMAT
            631     ;*
            632     ;* DRIVE TYPE = FUJI 2344 (SW4)
            633     ;* BLOCK SIZE = 522/116
            634     ;*
00192       635         ORG H#192
00192 00FFF0 636        DW  16-  ;HEAD SCATTER
00193 00FFFD 637        DW  3-       ;GAP/AM
00194 00FFEE 638        DW  18-  ;PLO GAP
00195 00FFFA 639        DW  6-       ;HEADER DATA
00196 00FFFC 640        DW  4-       ;HEADER ECC
00197 00FFEB 641        DW  21-  ;GAP 2
0019[illegible]3 00FDF6 642        DW  522-     ;(523) DATA AND SYNC (two's COMPLEMENT)
00199 00FFFB 643        DW  5-       ;DATA ECC
0019A 00FFF4 644        DW  12-  ;WRITE/READ RECOVERY
            645     ;*
            646     ;* FORMAT
            647     ;*
            648     ;* DRIVE TYPE = FUJI 2344 (SW4)
            649     ;* BLOCK SIZE = 2052/456
            650     ;*
0019B       651         ORG H#19B
0019B 00FFF0 652        DW  16-  ;HEAD SCATTER
0019C 00FFFD 653        DW  3-       ;GAP/AM
0019D 00FFEE 654        DW  18-  ;PLO GAP
0019[illegible]E 00FFFA 655        DW  6-       ;HEADER DATA
0019F 00FFFC 656        DW  4-       ;HEADER ECC
001A0 00FFEB 657        DW  21-  ;GAP 2
001A1 00F7FC 658        DW  2052-    ;(2053) DATA AND SYNC (two's COMPLEMENT)
001A2 00FFFB 659        DW  5-       ;DATA ECC
001A3 00FFF4 660        DW  12-  ;WRITE/READ RECOVERY
```

```
Addr        Line

            661         EJECT
            662     ;*
            663     ;* FORMAT
            664     ;*
            665     ;* DRIVE TYPE = CDC 1.2 GIGABYTE (SABER)
            666     ;* BLOCK SIZE = 522/116
            667     ;*
001B6       668         ORG H#1B6
001B6 00FFF2 669        DW  14-     ;HEAD SCATTER
001B7 00FFFD 670        DW  3-      ;GAP/AM
001B8 00FFF5 671        DW  11-     ;PLO GAP
001B9 00FFFA 672        DW  6-      ;HEADER DATA
001BA 00FFFC 673        DW  4-      ;HEADER ECC
001BB 00FFF1 674        DW  15-  ;GAP 2
001BC 00FDF6 675        DW  522-     ;(522) DATA AND SYNC (two's COMPLEMENT)
001BD 00FFFB 676        DW  5-      ;DATA ECC
001BE 00FF60 677        DW  160-   ;WRITE/READ RECOVERY (Temp. for CDC7001 only!)
            678     ;*
            679     ;* FORMAT
            680     ;*
            681     ;* DRIVE TYPE = FUJI 2333 (SW3)
            682     ;* BLOCK SIZE = 522/116
            683     ;*
001C8       684         ORG H#1C8
001C8 00FFF8 685        DW  8-      ;HEAD SCATTER
001C9 00FFFD 686        DW  3-      ;GAP/AM
001CA 00FFFA 687        DW  6-      ;PLO GAP
001CB 00FFFA 688        DW  6-      ;HEADER DATA
001CC 00FFFC 689        DW  4-      ;HEADER ECC
001CD 00FFEB 690        DW  21-  ;GAP 2
001CE 00FDF6 691        DW  522-     ;(523) DATA AND SYNC (two's COMPLEMENT)
001CF 00FFFB 692        DW  5-      ;DATA ECC
001D0 00FFF0 693        DW  16-  ;WRITE/READ RECOVERY
            694     ;*
            695     ;* FORMAT
            696     ;*
            697     ;* DRIVE TYPE = FUJI 2333 (SW3)
            698     ;* BLOCK SIZE = 2052/456
            699     ;*
001D1       700         ORG H#1D1
001D1 00FFF8 701        DW  8-      ;HEAD SCATTER
001D2 00FFFD 702        DW  3-      ;GAP/AM
001D3 00FFFA 703        DW  6-      ;PLO GAP
001D4 00FFFA 704        DW  6-      ;HEADER DATA
001D5 00FFFC 705        DW  4-      ;HEADER ECC
001D6 00FFEB 706        DW  21-  ;GAP 2
001D7 00F7FC 707        DW  2052-    ;(2053) DATA AND SYNC (two's COMPLEMENT)
001D8 00FFFB 708        DW  5-      ;DATA ECC
001D9 00FFF0 709        DW  16-  ;WRITE/READ RECOVERY
```

```
 Addr        Line

             710         EJECT
             711     ;*
             712     ;* FORMAT
             713     ;*
             714     ;* DRIVE TYPE = FUJI 2382 (SW5)
             715     ;* BLOCK SIZE = 522/116
             716     ;*
 001DA       717         ORG H#1DA
 001DA 00FFF8 718        DW  8-      ;HEAD SCATTER
 001DB 00FFFD 719        DW  3-      ;GAP/AM
 001DC 00FFF8 720        DW  8-      ;PLO GAP
 001DD 00FFFA 721        DW  6-      ;HEADER DATA
 001DE 00FFFC 722        DW  4-       ;HEADER ECC
 001DF 00FFE7 723        DW  25-  ;GAP 2
 001E0 00FDF6 724        DW  522-     ;(523) DATA AND SYNC (two's COMPLEMENT)
 001E1 00FFF8 725        DW  5-      ;DATA ECC
 001E2 00FFE6 726        DW  26-  ;WRITE/READ RECOVERY
             727     ;*
             728     ;* FORMAT
             729     ;*
             730     ;* DRIVE TYPE = FUJI 2382 (SW5)
             731     ;* BLOCK SIZE = 2052/456
             732     ;*
 001E3       733         ORG H#1E3
 001E3 00FFF8 734        DW  8-      ;HEAD SCATTER
 001E4 00FFFD 735        DW  3-      ;GAP/AM
 001E5 00FFF8 736        DW  8-      ;PLO GAP
 001E6 00FFFA 737        DW  6-      ;HEADER DATA
 001E7 00FFFC 738        DW  4-      ;HEADER ECC
 001E8 00FFE7 739        DW  25-  ;GAP 2
 001E9 00F7FC 740        DW  2052-    ;(2053) DATA AND SYNC (two's COMPLEMENT)
 001EA 00FFFB 741        DW  5-      ;DATA ECC
 001EB 00FFE6 742        DW  26-    ;WRITE/READ RECOVERY
```

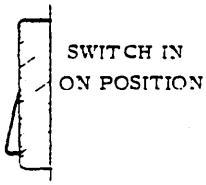
```
Addr        Line

            743         EJECT
            744     ;*
            745     ;* FORMAT
            746     ;*
            747     ;* DRIVE TYPE = CDC 368 (DATA COPY DRIVE)
            748     ;* BLOCK SIZE = 1152/256
            749     ;*
001EC       750         ORG H#1EC
001EC 00FFF0 751        DW  16-  ;HEAD SCATTER
001ED 00FFFD 752        DW  3-     ;GAP/AM
001EE 00FFF3 753        DW  13-  ;PLO GAP
001EF 00FFFA 754        DW  6-     ;HEADER DATA
001F0 00FFFC 755        DW  4-    ;HEADER ECC
001F1 00FFF2 756        DW  14-  ;GAP 2
001F2 00FB80 757        DW  1152-    ;(1153) DATA AND SYNC (two's COMPLEMENT)
001F3 00FFFB 758        DW  5-     ;DATA ECC
001F4 00FFF6 759        DW  10-  ;WRITE/READ RECOVERY
            760     ;*
            761     ;* FORMAT
            762     ;*
            763     ;* DRIVE TYPE = FUJI 2333 (DATA COPY DRIVE)
            764     ;* BLOCK SIZE = 1152/256
            765     ;*
001F5       766         ORG H#1F5
001F5 00FFF8 767        DW  8-     ;HEAD SCATTER
001F6 00FFFD 768        DW  3-     ;GAP/AM
001F7 00FFFA 769        DW  6-     ;PLO GAP
001F8 00FFFA 770        DW  6-     ;HEADER DATA
001F9 00FFFC 771        DW  4-     ;HEADER ECC
001FA 00FFEB 772        DW  21-    ;GAP 2
001FB 00FB80 773        DW  1152-  ;(1153) DATA AND SYNC (two's COMPLEMENT)
001FC 00FFFB 774        DW  5-     ;DATA ECC
001FD 00FFF0 775        DW  16-    ;WRITE/READ RECOVERY
            776     ;
            777         END
```

DW D NARG A 00000000

Assembly Phase complete.
0 error(s) detected.

3. When Speed/Density has been determined, note switch positions of the 7-position switch located on PC board C1A1. These switches are factory set and should require no change. Refer to the table below for switch location.



SWITCH		TAPE MODELS	100 IPS 800/1600	100 IPS 1600/6250	100 IPS 7TRK 556/800	150 IPS 800/1600	150 IPS 1600/6250	150 IPS 7TRK 556/800	200 IPS 800/1600	200 IPS 1600/6250	200 IPS 7TRK 556/800
MODE		1	ON	ON	ON	ON	ON	ON	ON	ON	ON
		2	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF
		3	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON
SPEED		4	ON	OFF	ON	ON	OFF	ON	ON	OFF	ON
		5	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF
		6	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON	ON
		7	ON	ON	ON	ON	ON	ON	OFF	OFF	OFF

C1A1 7-POSITION SWITCH

4. Reinstall C1A1 PC board when Speed/Density has been verified.

c. Perform test 1 of Minimum Performance Standards Test, Table 2-8.

d. Load a reel of tape without a write enable ring installed.

e. Execute a tape load. Observe that tape threads from supply reel to takeup reel, drops into loop columns, and positions at load point marker. Ensure write enable solenoid plunger does not rub ring access in rear of supply reel. Observe for WRITE DISABLE illumination.

f. Perform tests 3.a, b and c of Minimum Performance Standards Test, Table 2-8. Consult Table 2-1 for appropriate tools and test equipment.

g. Perform capstan alignment procedure per RRA-1010.

NOTE

Whenever transport is moved from one location to another (including within a site), this test must be performed.

h. Execute an unload procedure.

j. Install a write enable ring into supply reel and load tape; WRITE DISABLE extinguishes.

k. Run appropriate diagnostics.

The foregoing checks are intended to indicate the general operability of the transport upon initial installation, and to disclose problems accuring from damage during transit. If required result are not obtained, consult paragraph 2-4, Troubleshooting.

1-3.4 REPACKING

Using the materials that were stored in step i, paragraph 1-3.2, repack the transport by performing steps a thru f of paragraph 1-3.2 in reverse order.

CAUTION

Always replace blown fuse with one of identical ampere rating. If power interrupt or failure to sustain correct operation persists, discontinue operation and power down equipment.

1-3.3 POWER UP AND CHECKOUT

Following satisfactory completion of Initial Visual Inspection, the transport is ready for power connection.

a. Ensure site power source matches the configuration shown in Figure 1-4. Appropriate mating receptacles are Hubbel 2513 or equivalent for 60 Hz and Hubble 2533 or equivalent for 50 Hz.

b. Speed/Density Verification

1. Remove sensor and model decode PC board from location C1A1.
2. Identify transport recording modes and number of tracks by comparing nameplate (located on front of unit) and the number on product identification plate (located on inside rear of unit) with the following data in the table below.

SYSTEM NUMBER	EQUIPMENT NUMBER	SPEED (ips)	RECORDING MODE	DENSITY (bpi)	TRACK
679-7	BW401/402/411	200	PE/GCR	1600/6250	9
679-6	BW401/402/412	150	PE/GCR	1600/6250	9
679-5	BW401/402/413	100	PE/GCR	1600/6250	9
679-4	BW401/402/414	200	DM	800/1600	9
679-3	BW401/402/415	150	DM	800/1600	9
679-2	BW401/402/416	100	DM	800/1600	9
677-4	BW401/402/201	200	NRZI	556/800	7
677-3	BW401/402/202	150	NRZI	556/800	7
677-2	BW401/402/208	100	NRZI	556/800	7
GCR	BW430/431/432	200	PE/GCR	1600/6250	9

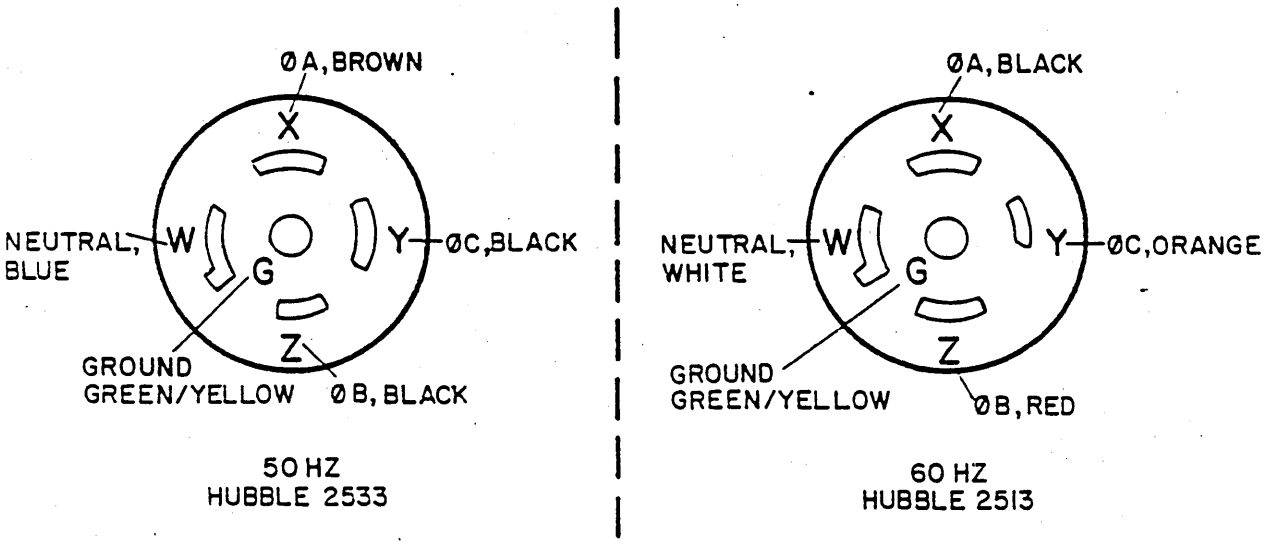


Figure 1-4. AC Power Connector

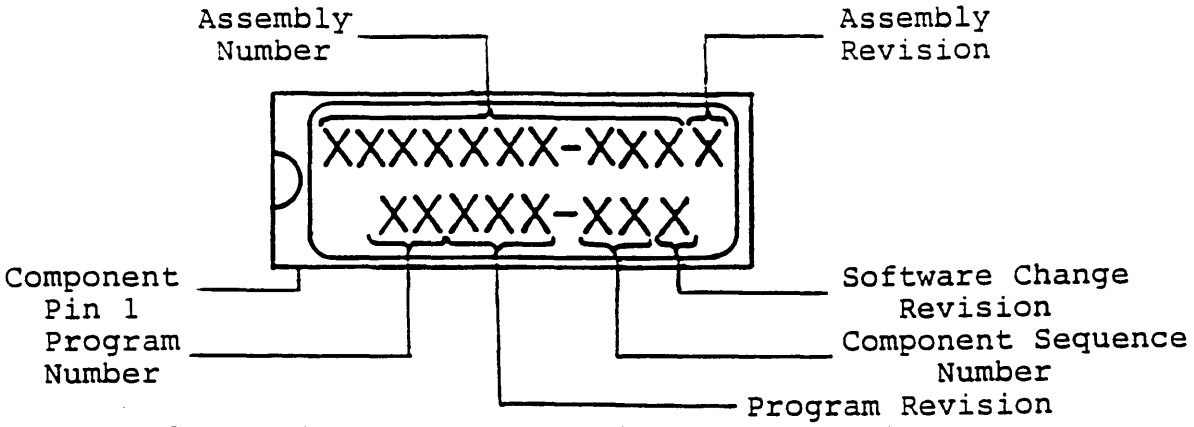
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33FA0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U18.
   Used on PCBA 1602522-101 Location U51.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision FA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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DRAFTSMAN Cheryl Reynolds	5/15/89
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APPROVED	

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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601572-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

3B1B

PAL20L8 AMPERIF CORPORATION

REF NO.15, REV.1
JACK SERAFIN, 8/25/86
5 EN 1ADCKC 5EPDATEN 1SRADCEN 1DRYRUN 1ONLINE 3FFF GND GND GND
GND GND GND GND NC NC NC NC 3FFFQ 5MILATE 5CADSEN 5OLLED GND VCC

/5OLLED = 5NOPEN

/5CADSEN = /5EPDATEN + 1SRADCEN * 1DRYRUN

/5MILATE = 1SRADCEN * 1DRYRUN * 1ADCKC + 1ONLINE + /5EPDATEN * 1ADCKC

/3FFFQ = /3FFF + /1DRYRUN

P/N 1601572-001 33FA0

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE PAL ASSEMBLY, EXP MEM	REV. D
DRAWING NO. 1601572-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9254

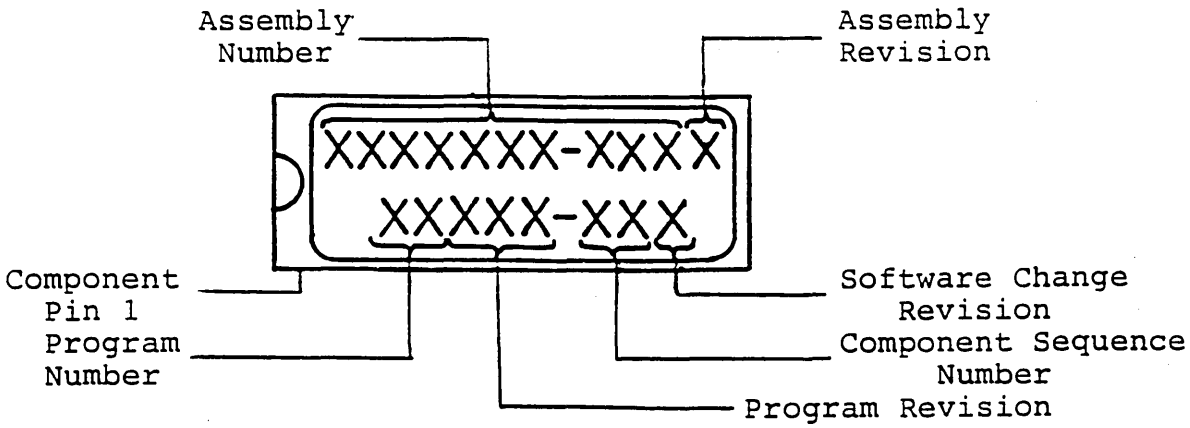
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - ECO # 2029 CR	8-4-89	MM

Procedure:

1. Program component using data filed in software no. 42BA0-01 A.

2. Make from unprogrammed part number 20156600-001.

3. Used on PCBA 1601962-101,201,202 Location U167.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 42 Revision BA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

CHECKSUM = 97E8

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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amperif memory products

PAL ASSEMBLY,

XMCP2

REV A

SIZE	DRAWING NO.	SHEET
A	1602232-101	1 OF 3

```
Partno      0000-0000 ;
Date        04/APR/88 ;
Revision    01        ;
Designer    R.BUSTAMANTE;
Company     Amperif   ;
Assembly    XMC       ;
Location    U167   ;

/*************************************************************************************



 ************************************************************************************
    Allowable Target Device Types:
 ************************************************************************************/


/** Re-define operators **/

$define :+: $           /* XOR operator                                    */
$define  +  #           /* OR  operator                                    */


/**  Inputs  **/

Pin 1    = A          ;    /*                                              */
Pin 2    =  ALUY1     ;    /*                                              */
Pin 3    =  SMCMDLC   ;    /*                                              */
Pin 4    =  MINST20   ;    /*                                              */
Pin 5    =  MINST21   ;    /*                                              */
Pin 6    =  MINST22   ;    /*                                              */
Pin 7    =  MINST23   ;    /*                                              */
Pin 8    =  !ALUFOUT  ;    /*                                              */
Pin 9    =  !CLK12    ;    /*                                              */
Pin 10   =  !CLK1     ;    /*                                              */
Pin 11   =  !CLEAR    ;    /*                                              */
Pin 20   =  ALUY0     ;    /*                                              */
Pin 14   =  HIOEN     ;    /*                                              */
Pin 16   =  HIOENA    ;    /*                                              */


/**  Outputs  **/

Pin 23   =  SEQIR12   ;    /*                                              */
Pin 22   =  SEQIR13   ;    /*                                              */
Pin 21   =  SMCMDLB   ;    /*                                              */
Pin 19   =  RSTIRU    ;    /*                                              */
Pin 18   =  C         ;    /*                                              */
Pin 17   = !RSHENA    ;    /*                                              */
Pin 15   = !RSHEN     ;    /*                                              */


/** Un-Used Pins **/
/*

*/
```

```
/** Declarations and Intermediate Variable Definitions **/

SETIRU = MINST20 & !MINST21 & !MINST22 &  MINST23 & ALUFOUT ;
RSTIRU = !MINST20 & MINST21 & MINST22 &  MINST23 ;

/**  Logic Equations  **/

 SEQIR12.D  = ALUY0 & SETIRU + SEQIR12 & !RSTIRU & !CLEAR + SEQIR12 & !ALUFOUT
 & !CLEAR ;
 SEQIR12.CK = !CLK1  ;
 SEQIR12.AP =  CLEAR ;
 SEQIR13.D  = ALUY1 & SETIRU + SEQIR13 & !RSTIRU & !CLEAR + SEQIR13 & !ALUFOUT
 & !CLEAR ;
 SEQIR13.CK = !CLK1  ;
 SEQIR13.AP =  CLEAR ;
 SMCMDLB.D  = !SMCMDLB & SMCMDLC ;
 SMCMDLB.CK = !CLK12  ;
 RSHEN.D    =  HIOEN  ;
 RSHEN.CK   = !CLK1   ;
 RSHENA.D   =  HIOENA ;
 RSHENA.CK  = !CLK1   ;
```

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV.
PAL ASSEMBLY, XMCP2	A
DRAWING NO. 1602232-101	SHEET 3 OF 3

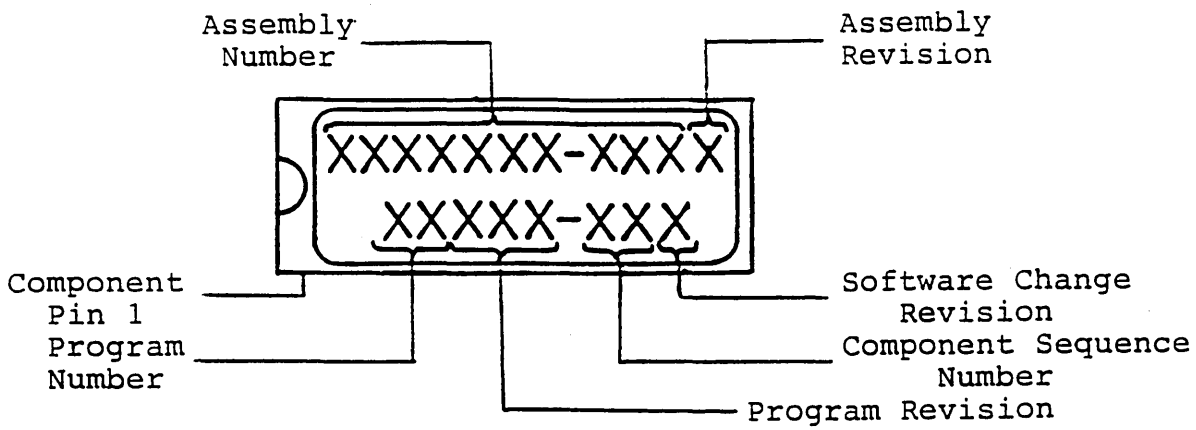
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - ECO # 2029 CR	8-4-89	MM

Procedure:

1. Program component using data filed in software no. 42AA0-01A.

2. Make from unprogrammed part number 20156600-001.

3. Used on PCBA 1601962-101,201,202 Location U136.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 42 Revision AA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

CHECKSUM = DE8D

NOTES: Unless Otherwise Specified.

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PAL ASSEMBLY,

XMCP1

REV A

SIZE	DRAWING NO.	SHEET
A	1602231-101	1 OF 3

```
Partno      0000-0000 ;
Date        04/APR/88 ;
Revision    01        ;
Designer    R.BUSTAMNTE;
Company     Amperif   ;
Assembly    XMC       ;
Location    U136   ;

/*****************************************************************************
 THIS PAL SET PARITY ERROR STATUS FOR ALL THE BUSSES,IT ALL PRESENT STATUS
ON THE ALU INPUT BUSS.



 *****************************************************************************
    Allowable Target Device Types:
 *****************************************************************************/

/** Re-define operators **/

$define :+: $           /* XOR operator                                      */
$define  +  #           /* OR  operator                                      */


/**  Inputs  **/

Pin 1    =   A        ;   /*                                                  */
Pin 2    =  UPARERU   ;   /*                                                  */
Pin 3    =  !HRCVGT2  ;   /*                                                  */
Pin 4    =  UPARERL   ;   /*                                                  */
Pin 5    =  !HRCVGT1  ;   /*                                                  */
Pin 6    =  CTSDPE    ;   /*                                                  */
Pin 7    =  !RDSPAD   ;   /*                                                  */
Pin 8    =  CTSPDN    ;   /*                                                  */
Pin 9    =  !CLK1     ;   /*                                                  */
Pin 10   =  !CLK12    ;   /*                                                  */
Pin 11   =  !CLEAR    ;   /*                                                  */
Pin 18   =  !SMCSTEN  ;   /*                                                  */


/**  Outputs  **/

Pin 23   =  !RSSMCB   ;   /*                                                  */
Pin 22   =   UPERL    ;   /*                                                  */
Pin 21   =   UPERU    ;   /*                                                  */
Pin 20   =   CTSDPER  ;   /*                                                  */
Pin 19   =   SPPER    ;   /*                                                  */
Pin 17   =  !ALUO0    ;   /*                                                  */
Pin 16   =  !ALUO1    ;   /*                                                  */
Pin 15   =  !ALUO2    ;   /*                                                  */
Pin 14   =  !ALUO3    ;   /*                                                  */


/** Un-Used Pins **/
/*

*/


/** Declarations and Intermediate Variable Definitions **/
```

```
/**  Logic Equations  **/

RSSMCB.D  =  SMCSTEN  ;
RSSMCB.CK = !CLK1     ;
RSSMCB.AR =  CLEAR    ;
UPERL.D   = HRCVGT1 & UPARERL
          + !RSSMCB & UPERL & !CLEAR ;
UPERL.CK  = !CLK1     ;
UPERL.AP  =  CLEAR    ;
UPERU.D   = HRCVGT2 & UPARERU
          + !RSSMCB & UPERU & !CLEAR ;
UPERU.CK  = !CLK1     ;
UPERU.AP  =  CLEAR    ;
CTSDPER.D = CTSPDN
          + !RSSMCB & CTSDPER & !CLEAR ;
CTSDPER.CK = !CLK1    ;
CTSDPER.AP =  CLEAR   ;
SPPER.D    = RDSPAD & CTSDPE
           + !RSSMCB & SPPER & !CLEAR ;
SPPER.CK   = !CLK1    ;
SPPER.AP   =  CLEAR   ;
ALUO0.D    = HRCVGT1 & UPARERL
           + !RSSMCB & UPERL & !CLEAR ;
ALUO0.CK   = !CLK1    ;
ALUO0.AR   =  CLEAR   ;
ALUO0.OE   =  SMCSTEN ;
ALUO1.D    =  HRCVGT2 & UPARERU
           + !RSSMCB & UPERU & !CLEAR ;
ALUO1.CK   = !CLK1    ;
ALUO1.AR   =  CLEAR   ;
ALUO1.OE   =  SMCSTEN ;
ALUO2.D    =  CTSPDN
           + !RSSMCB & CTSDPER & !CLEAR ;
ALUO2.CK   = !CLK1    ;
ALUO2.AR   =  CLEAR   ;
ALUO2.OE   =  SMCSTEN ;
ALUO3.D    = RDSPAD & SPPER
           + !RSSMCB & SPPER & !CLEAR;
ALUO3.CK   = !CLK1    ;
ALUO3.AR   =  CLEAR   ;
ALUO3.OE   =  SMCSTEN ;
```

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DOCUMENT TITLE	REV.
PAL ASSEMBLY, XMCP1	A
DRAWING NO. 1602231-101	SHEET 3 OF 3

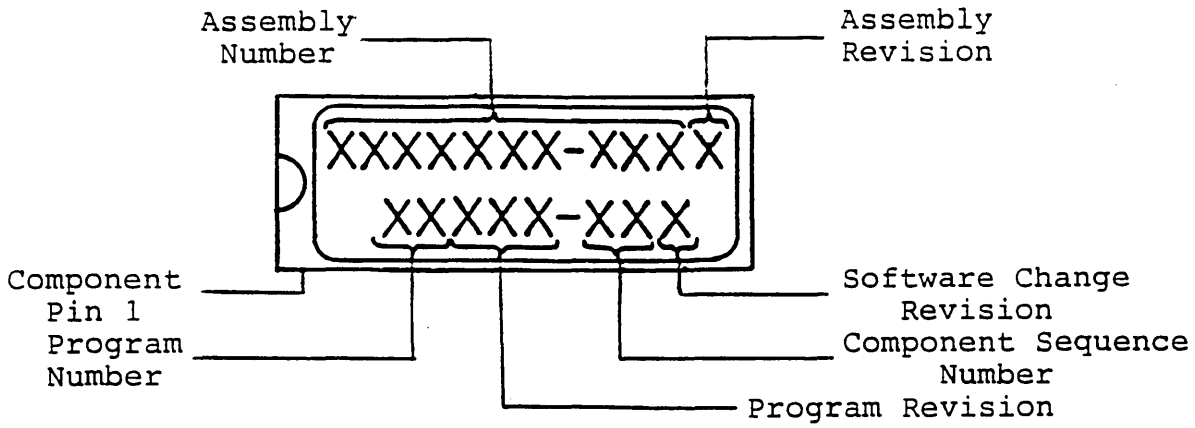
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
9	RELEASE - ECO #2029 CR	8-4-89	MM

Procedure:

1. Program component using data filed in software no. 42-A0-01 A.

2. Make from unprogrammed part number 20156600-001.

3. Used on PCBA 1601962-101,201,202 Location U166.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 42 Revision -A0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

CHECKSUM = C517

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY,

XMCP0

REV A

SIZE	DRAWING NO.	SHEET
A	1602230-101	1 OF 3

```
Partno      0000-0000 ;
Date        05/APR/88 ;
Revision    01        ;
Designer    R.BUSTAMANTE;
Company     Amperif   ;
Assembly    XMC/PCB   ;
Location    U166      ;

/*************************************************************************
   THIS PAL DECODE AN SET HIO CONTROL TAGS. THE PAL IS PART OF THE XMC BOARD
 FOR THE NEW MULTI HOST SHARING.



 *************************************************************************
    Allowable Target Device Types: 20RA10
 *************************************************************************/


/** Re-define operators **/

$define :+: $           /* XOR operator                                  */
$define  +  #           /* OR  operator                                  */


/**  Inputs  **/

Pin 1    =  A         ;    /*                                            */
Pin 2    =  MINST21   ;    /*                                            */
Pin 3    =  MINST22   ;    /*                                            */
Pin 4    =  MINST23   ;    /*                                            */
Pin 5    =  MINST24   ;    /*                                            */
Pin 6    =  MINST25   ;    /*                                            */
Pin 7    = !HIOTCK3   ;    /*                                            */
Pin 8    = !HMODCK    ;    /*                                            */
Pin 9    =  SEQYB12   ;    /*                                            */
Pin 10   = !CLK1      ;    /*                                            */
Pin 11   = !CLEAR     ;    /*                                            */
Pin 17   =  MINST20   ;    /*                                            */
Pin 13   =   B        ;

/**  Outputs  **/

Pin 23   = !ODREQB    ;    /*                                            */
Pin 22   = !SETIDRB   ;    /*                                            */
Pin 21   = !EFREQB    ;    /*                                            */
Pin 20   = !HDRVGT    ;    /*                                            */
Pin 19   = !HIOTGT    ;    /*                                            */
Pin 18   = !HSIMGT    ;    /*                                            */
Pin 16   =  SEQAR12   ;    /*                                            */
Pin 15   = !ODREQ     ;    /*                                            */
Pin 14   = !SETIDR    ;    /*                                            */


/** Un-Used Pins **/
/*

*/


/** Declarations and Intermediate Variable Definitions **/
```

```
/**  Logic Equations  **/

ODREQB.D    =   MINST20 ;
ODREQB.CK   =  !HIOTCK3 ;
ODREQB.AR   =   CLEAR   ;
ODREQB.OE   =   HIOTGT  ;
SETIDRB.D   =   MINST21 ;
SETIDRB.CK  =  !HIOTCK3 ;
SETIDRB.AR  =   CLEAR   ;
SETIDRB.OE  =   HIOTGT  ;
EFREQB.D    =   MINST23 ;
EFREQB.CK   =  !HIOTCK3 ;
EFREQB.AR   =   CLEAR   ;
EFREQB.OE   =   HIOTGT  ;
HDRVGT.d    =  MINST20
            +   HDRVGT & !MINST21  ;
HDRVGT.CK   =  !HMODCK  ;
HDRVGT.AR   =   CLEAR   ;
HIOTGT.D    =  MINST22
            +   HIOTGT & !MINST23  ;
HIOTGT.CK   =  !HMODCK  ;
HIOTGT.AR   =   CLEAR   ;
HSIMGT.D    =   MINST24
            +   HSIMGT & !MINST25  ;
HSIMGT.CK   =  !HMODCK  ;
HSIMGT.AR   =   CLEAR   ;
SEQAR12.D   =  SEQYB12  ;
SEQAR12.CK  =  !CLK1    ;
ODREQ.D     =  MINST20  ;
ODREQ.CK    =  !HIOTCK3 ;
ODREQ.AR    =   CLEAR   ;
SETIDR.D    =  MINST21  ;
SETIDR.CK   =  !HIOTCK3 ;
SETIDR.AR   =   CLEAR   ;
```

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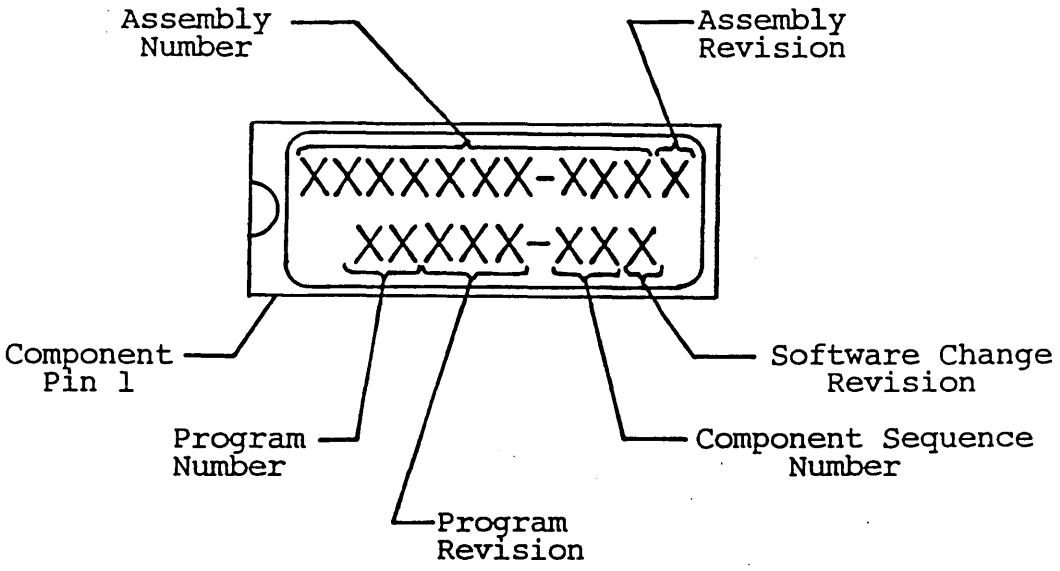
DOCUMENT TITLE	REV.
PAL ASSEMBLY, XMCP1	A
DRAWING NO. 1602230-101	SHEET 3 OF 3

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label nm	10-19-87	

Procedure:

1. Program component using data filed in software No. 36DA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location EA26



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision DA0 .
2. Make from unprogrammed part number 20051400 .
1. See separate parts list.

NOTES: Unless Otherwise Specified

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PAL ASSEMBLY, XMCIP@EA26

SIZE	DRAWING NO.	SHEET	REV
A	1601696-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PN 1601696-001
PAL16R4

SID 36DA0-01A
LOCATION EA26

```
/UA   /UB   /UC   /UD   /PA   /PB   /PC   /PC   BCT3  GND
BCT2  NC    BCT1  BCT0  /B3   MC2   /RW   /X    PE    VCC

(IF VCC)
X    = UA * PA * MC2 * B3 * /BCT3 * /BCT2 * /RW
     + UB * PB * MC2 * BCT0 * /BCT1 * BCT2 * /BCT3 * B3 * /RW
     + /UB * /PB * MC2 * BCT0 * /BCT1 * BCT2 * /BCT3 * B3 * /RW
     + UC * PC * MC2 * BCT0 * BCT1 * BCT2 * /BCT3 * /RW
     + /UC * /PC * MC2 * BCT0 * BCT1 * BCT2 * /BCT3 * /RW
     + UD * PD * MC2 * /BCT0 * /BCT1 * /BCT2 * /BCT3 * /RW
     + /UD * /PD * MC2 * /BCT0 * /BCT1 * /BCT2 * /BCT3 * /RW

(IF VCC)
/PE = /X * UA + /X * PA + /X * /MC2 + /X * /B3
     + /X * BCT2 + /X * BCT3 + /X * RW
```

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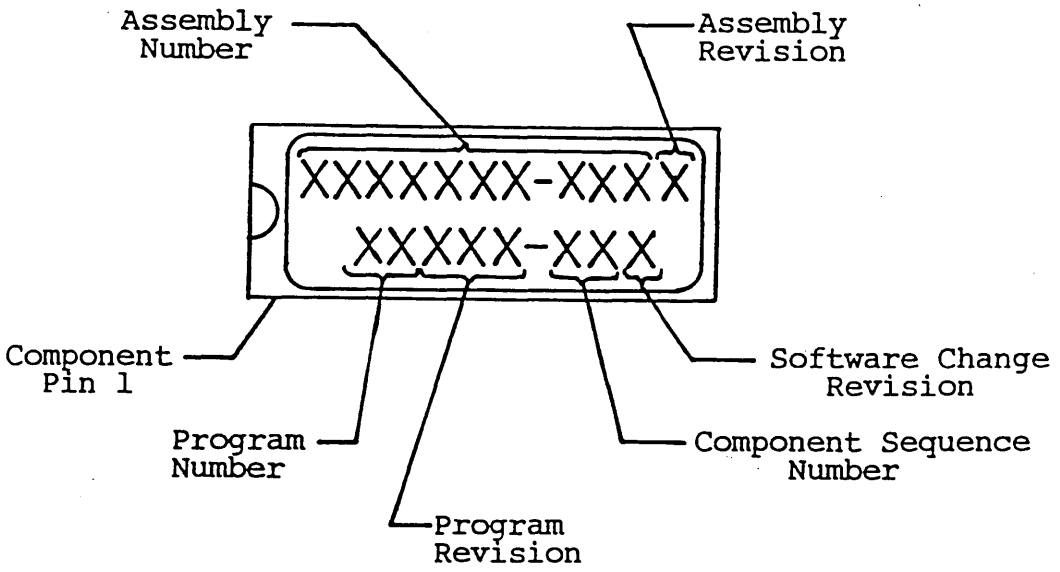
DOCUMENT TITLE	REV
PAL ASSY, XMCI @ EA26	B
DOCUMENT NUMBER 1601696-001	SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label MM	10-19-87	

Procedure:

1. Program component using data filed in software No. 36CA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location EA51



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision CA0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

NOTES: Unless Otherwise Specified

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PAL ASSEMBLY, XMCIP@EA51

SIZE	DRAWING NO.	SHEET	REV
A	1601695-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PN 1601695-001 SID 36CA0-01A
PAL16R4 LOCATION EA51

```
/CLK  /PU  /PL  /PA  /PB  /PC  /PD  /REG1  /REG2  GND
OE    UL   UU   /UD  /UC  /UB  /UA  /RW    NC     VCC

UA:   = REG1 & pu = /REG1 * UA

UB:   = REG1 * PL + /REG1 * UB

UC:   = REG2 * PU + /REG2 * UC

UD:   = REG2 * PL + /REG2 * UD

(IF VCC)
/UL   = PB * PD + PB * /REG2 + /REG1 * PD + /REG1 * /REG2

(IF VCC)
/UU   = PA * PC + PA * /REG2 + /REG1 * PC + /REG1 * /REG2
```

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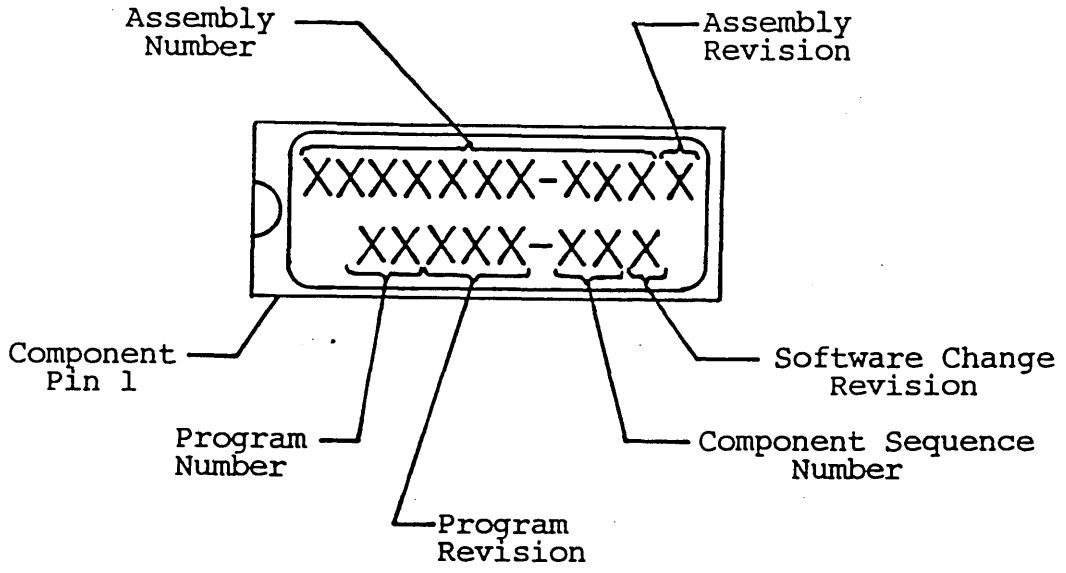
DOCUMENT TITLE	REV
PAL ASSY, XMCI @ EA51	B
DOCUMENT NUMBER 1601695-001	SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label mm	10-19-87	

Procedure:

1. Program component using data filed in software No. 36BA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location EA37



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision BA0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

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PAL ASSEMBLY, XMCIP @EA37

SIZE	DRAWING NO.	SHEET	REV
A	1601694-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9253

PN 1601694-001 SID 36BA0-01A
PAL16R4 LOCATION EA37

```
/CLK  /C   /D   /4U   /4L   BCT0  BCT1  BCT2  BCT3  GND
OE    /INC /80  MC2   /MC1  /PD   /PC   /PDJ  /PCJ  VCC

MC1: = INC

/MC2:= /MC1

PC:   = 4L * BCT0 * /BCT1 * BCT2 * /BCT3 * MC1
      + 80 * /BCT0 * BCT1 * BCT2 * /BCT3 * MC1 * /PC
      + 4U * /C * BCT0 * BCT1 * BCT2 * /BCT3 * MC1 * /PC
      + /4U * C * BCT0 * BCT1 * BCT2 * /BCT3 * MC1 * /PC
      + PCJ
      + PC * /MC1

PD:   = D * BCT0 * BCT1 * BCT2 * /BCT3 * MC1
      + 80 * /BCT0 * /BCT1 * /BCT2 * BCT3 * MC1 * /PD
      + 80 * /BCT0 * /BCT1 * /BCT2 * /BCT3 * MC1 * /PD
      + PDJ
      + PD * /MC1
      + BCT3 * BCT2 * PD
      + /BCT1 * BCT0 * PD
      + BCT1 * /BCT0 * PD

(IF VCC)
PCJ   = /BCT0 * BCT1 * BCT2 * /BCT3 * 4U * 4L * MC1 * PC
      + /BCT0 * BCT1 * BCT2 * /BCT3 * /4U * /4L * MC1 * PC
      + BCT0 * BCT1 * BCT2 * /BCT3 * 4U * /C * MC1 * PC
      + BCT0 * BCT1 * BCT2 * /BCT3 * /4U * /C * MC1 * PC
      + /BCT3 * /BCT2 * PC
      + BCT3 * PC
      + /BCT1 * /BCT0 * PC

(IF VCC)
PBJ   = /BCT0 * /BCT1 * /BCT2 * BCT3 * 4U * 4L * MC1 * PD
      + /BCT0 * /BCT1 * /BCT2 * BCT3 * /4U * /4L * MC1 * PD
      + /BCT0 * /BCT1 * /BCT2 */BCT3 * 4U * 4L * MC1 * PD
      + /BCT0 * /BCT1 * /BCT2 * /BCT3 * /4U * /4L * MC1 * PD
      + BCT3 * BCT1 * BCT0 * PD
      + /BCT3 * /BCT2 * BCT1 * PD
      + /BCT3 * BCT2 * /BCT1 * PD
```

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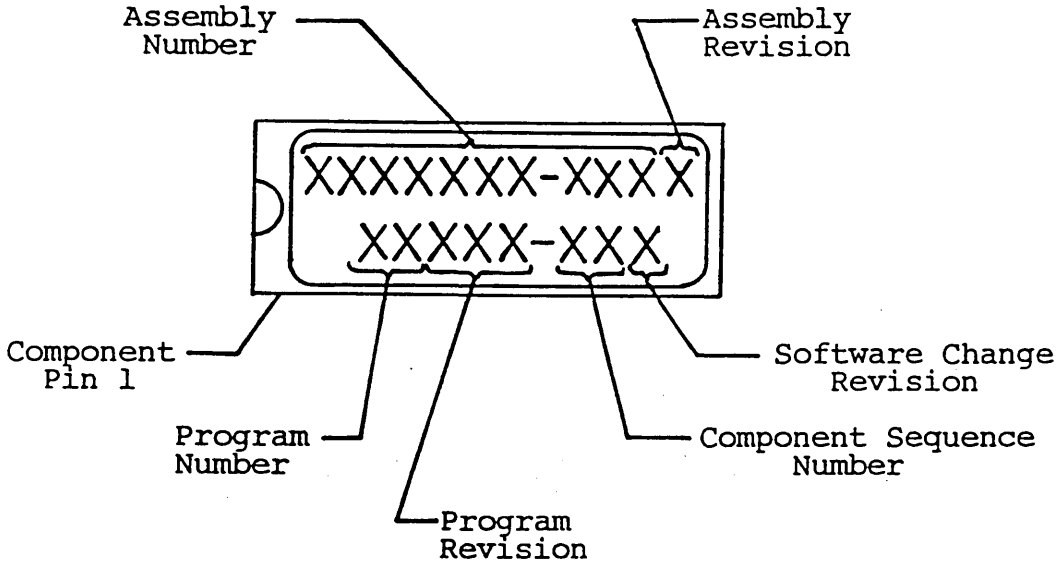
DOCUMENT TITLE	REV
PAL ASSY, XMCI @ EA37	B
DOCUMENT NUMBER 1601694-001	SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label MM	10-19-87	

Procedure:

1. Program component using data filed in software No. 36AA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location DL36



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision AA0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

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PAL ASSEMBLY, XMCIP@ DL36

SIZE	DRAWING NO.	SHEET	REV
A	1601693-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

```
FN 1601693-001                                  SID 36AA0-01A
PAL16R4                                         LOCATION DL36


/CLK  /A   /B   /4U   /4L   BCT0  BCT1  BCT2  BCT3  GND
NC    /INC NC   /B3   /MC1  /PB   /PA   /PBJ  /PAJ  VCC

MC1: = INC

B3:  = BCT0 * BCT1 * /BCT2 * /BCT3
     + /BCT0 * /BCT1 * BCT2 * /BCT3 * B3
     + BCT0 * /BCT1 * BCT2 * /BCT3 * B3

PA:  = 4L * /4U * BCT0 * /BCT1 * /BCT2 * /BCT3 * MC1
     + /4L * 4U * BCT0 * /BCT1 * /BCT2 * /BCT3 * MC1
     + 4L * /4U * /BCT0 * BCT1 * /BCT2 * /BCT3 * MC1 * /PA
     + /4L * 4U * /BCT0 * BCT1 * /BCT2 * /BCT3 * MC1 * /PA
     + A * BCT0 * BCT1 * /BCT2 * /BCT3 * MC1 * /PA
     + PAJ
     + PA * /MC1

PB:  = B * /4L * BCT0 * BCT1 * /BCT2 * /BCT3 * MC1
     + /B * 4L * BCT0 * BCT1 * /BCT2 * /BCT3 * MC1
     + 4L * /4U * /BCT0 * /BCT1 * BCT2 * /BCT3 * MC1 * /PB
     + /4L * 4U * /BCT0 * /BCT1 * BCT2 * /BCT3 * MC1 * /PB
     + 4U * BCT0 * /BCT1 * BCT2 * /BCT3 * MC1 * /PB
     + PBJ
     + PB * /MC1
     + BCT3 * PB

(IF VCC)
PAJ  = /BCT0 * BCT1 * /BCT2 * /BCT3 * 4U * 4L * MC1 * PA
     + /BCT0 * BCT1 * /BCT2 * /BCT3 * /4U * /4L * MC1 * PA
     + BCT0 * BCT1 * /BCT2 * /BCT3 * /A * MC1 * PA
     + BCT3 * PA
     + /BCT3 * BCT2 * PA
     + /BCT1 * /BCT0 * PA

(IF VCC)
PBJ  = /BCT0 * /BCT1 * BCT2 * /BCT3 * 4U * 4L * MC1 * PB
     + /BCT0 * /BCT1 * BCT2 * /BCT3 * /4U * /4L * MC1 * PB
     + BCT0 * /BCT1 * BCT2 */BCT3 * /4U * MC1 * PB
     + BCT1 * BCT2 * /BCT3 * PB
     + BCT1 * /BCT0 * PB
     + /BCT3 * /BCT2 * /BCT1 * PB
```

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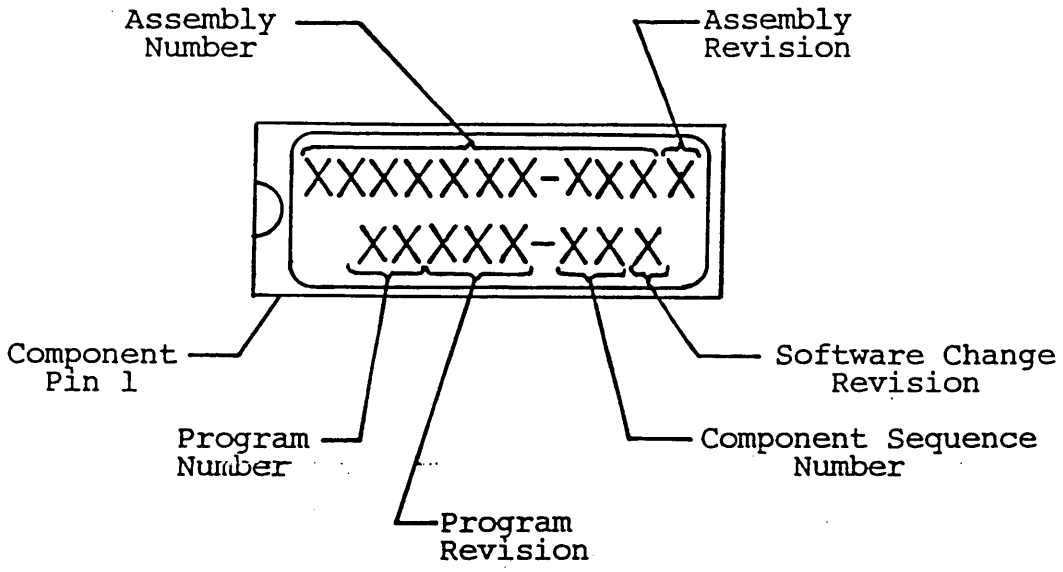
DOCUMENT TITLE	REV
PAL ASSY, XMCI @ DL36	B
DOCUMENT NUMBER 1601693-001	SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label MM	10-19-87	

Procedure:

1. Program component using data filed in software No. 36-A0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Useci on 1120010-201-202 Location DJ28



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision -A0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

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PAL ASSEMBLY, XMCIP @ DJ28

SIZE	DRAWING NO.	SHEET	REV
A	1601692-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

FN 1601692-001
PAL16R4

SID 36-A0-01A
LOCATION DJ28

```
/CLK    /D0    /D1    /D2    /D3    /D4    /D5    /D6    /D7    GND
OE      /4L    /4U    /D     /C     /B     /A     /80    NC     VCC
```

```
A: = D7 * /D6 + /D7 * D6
B: = D5 * /D4 + /D5 * D4
C: = D3 * /D2 + /D3 * D2
D: = D1 * /D0 + /D1 * D0

4U = A * /B + /A * B
4L = C * /D + /C * D

80 = 4L * /4U + /4L * 4U
```

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DOCUMENT TITLE: PAL ASSY, XMCI @ DJ28

REV: B

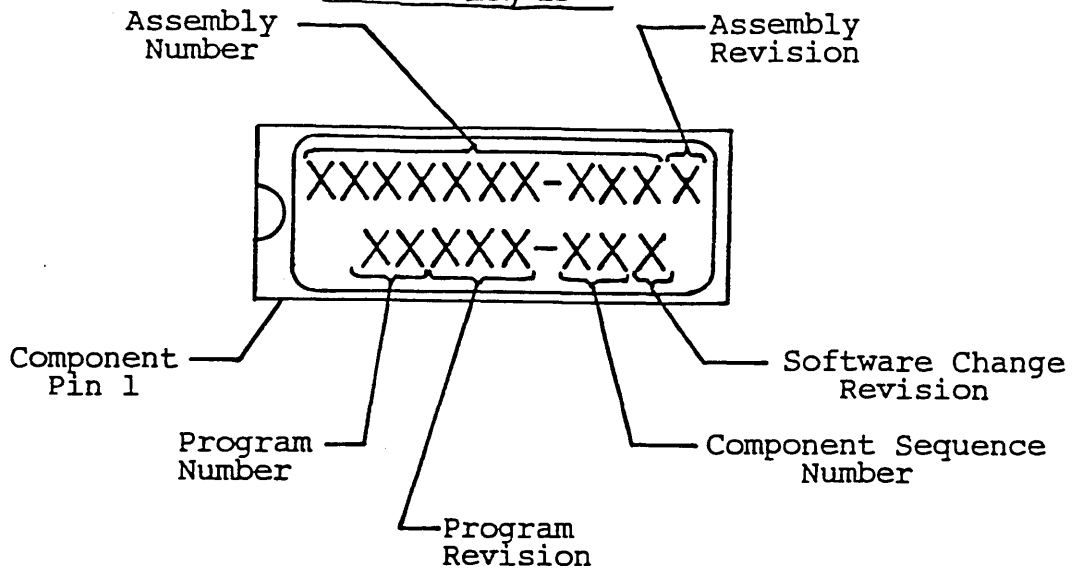
DOCUMENT NUMBER: 1601692-001

SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1270	2-23-87	CP
B	ECO1408 Add label MM	10-19-87	[illegible]

Procedure:

1. Program component using data filed in software No. 24CA0-01A .
2. Make from unprogrammed part number 20051700 .
3. PCBA Used on 1120012-301 / 1601553-201,-202 Location EA45



5. "Software change revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 24 Revision CA0 .
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified

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PAL ASSEMBLY, DIFP, FIFO EMPTY CHECK (EA45)

SIZE	DRAWING NO.	SHEET	REV
A	1601662-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

DIF FIFO EMPTY CHECK PAL

PN 1601662-001
SID 24CA0-01A

PAL16R4
LOCATION EA45

CONTROL/DRIVE SEQUENCER CHECK LOGIC

```
/C ECCI0 ECCI1 ECCI2 ECCI3 /OPCMPL /FMWRTM /DIFRST2 /CLK100 GND
/ENA /DR1CLK FIFOOR NC NC /EFIFOE /DIFSEQER TINDEX /CO VCC

DIFSEQER : = ECCI0 * ECCI1 * /ECCI2 * ECCI3 * /FMWRTM * FIFOOR *
             /DIFRST2

           + OPCMPL * FMWRTM * FIFOOR * /DIFRST2

           + EFIFOE * /DIFRST2

           + DIFSEQER * /DIFRST2

EFIOE : = ECCI0 * /ECCI1 * ECCI2 * ECCI3 * FMWRTM * TINDEX *
          /DIFRST2

        + EFIFOE * /DIFRST2

IF (VCC) CO = CLK100 * /FMWRTM
        + DR1CLK * FMWRTM
```

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DOCUMENT TITLE	REV
PAL ASSY, DIF (FIFO EMPTY CHECK)	B
DOCUMENT NUMBER 1601662-001	SHEET 2 OF 2

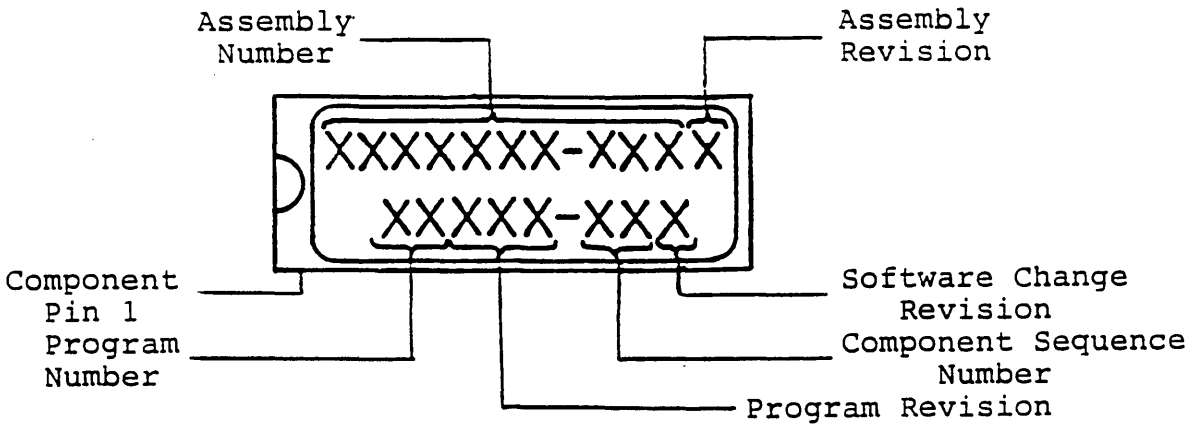
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33EA0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U17.
   Used on PCBA 1602522-101 Location U12.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision EA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601571-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

4508

PAL20L8 AMPERIF CORPORATION

REF NO.14, REV.0
JACK SERAFIN, 6/12/86
E RUN 5XXACT 1EPLDEND 1EPENBLD 1MONLN 1MSTRT 1PUH 1PUL 5PURST 1EENSW
5XENSW GND GND GND NC NC NC NC 1ESWQ 5ESRST 1PWRUP 5DRTRIG GND VCC

/5DRTRIG = /5XDRUN + 1EPLDEND + /1EPENBLD * 5XXACT * /1MONLN * 1MSTRT

/1PWRUP = /1PUH + /1PUL

/5ESRST = 1MONLN + /5PURST + /5XXACT

/1ESWQ = /1EENSW + /5XENSW

P/N 1601571-001 33 EA0

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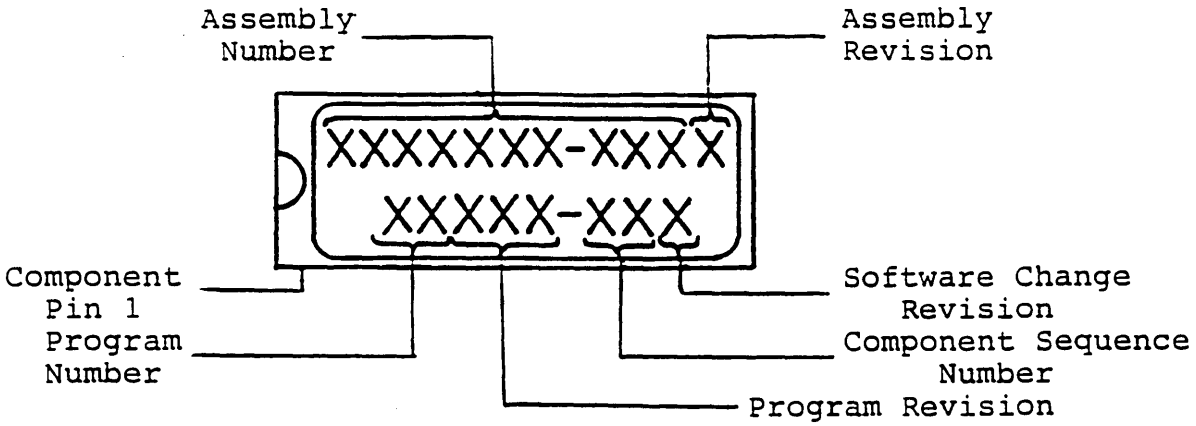
DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXP MEM	D
DRAWING NO. 1601571-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33DA0-01A.
2. Make from unprogrammed part number 20132100-001.
3. Used on PCBA 1601494-101,201,202 Location U16.
   Used on PCBA 1602522-101 Location U14.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.
5. "Software Change Revision" is A.
4. "Component Sequence Number" is 01.
3. "Program Number" is 33 Revision DA0.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601570-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

667E

PAL20L8 AMPERIF CORPORATION

REF NO.13, REV.0
JACK SERAFIN, 6/12/86
RLOAD 5PURST 5MRSPLSE 1ERLKUP 5XRST 1DRUNEND 5EADRCLR 1MSTRT 1DRYRUN 3FFF
1PWRUP GND 5SRCNTEN 5EPDATEN 5EPTRIG 1EPENBLD 5XEPLD NC NC 1SRADCEN 5SADRCLR
5DRRST 1MONLN VCC

/5DRRST = 1EPRLOAD + /5MRSPLSE + /5PURST + 1ERLKUP + /5XRST + 1DRUNEND

/5SADRCLR = /5PURST + /5XRST + /5EADRCLR + 1MSTRT + 1DRYRUN * 5SRCNTEN
+ 3FFF * 1DRYRUN

/1SRADCEN = 5EPDATEN * 5SRCNTEN

/5EPTRIG = 1PWRUP * 1MONLN + 1PWRUP * 1EPENBLD + 1EPENBLD * 1MSTRT + /5XEPLD

P/N 1601570-001 33DA0

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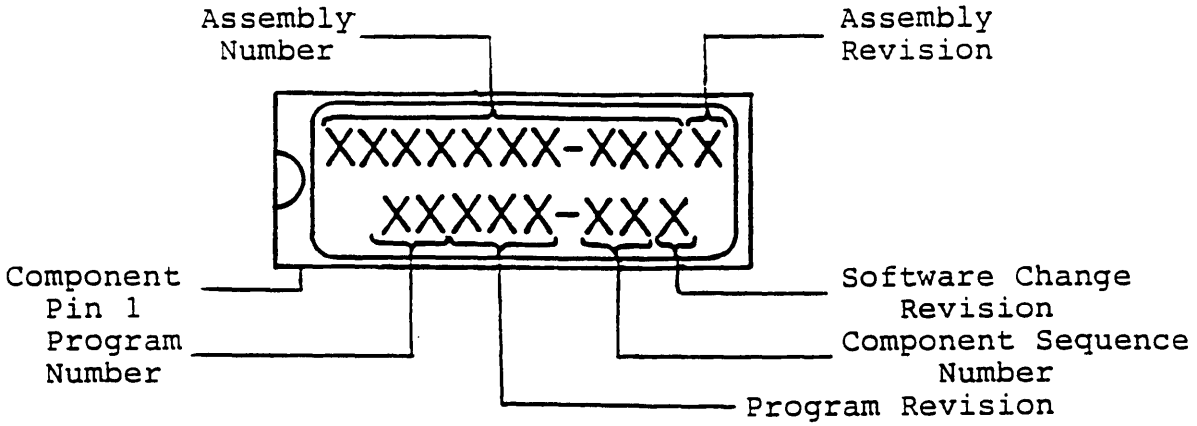
DOCUMENT TITLE PAL ASSEMBLY EXP MEM	REV. D
DRAWING NO. 1601570-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # Z548 CR	7/25/89	[illegible]

Procedure:

1. Program component using data filed in software no. 33CA0-01A.
2. Make from unprogrammed part number 20132100-001.
3. Used on PCBA 1601494-101,201,202 Location U15.
   Used on PCBA 1602522-101 Location U15.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.
5. "Software Change Revision" is A.
4. "Component Sequence Number" is 01.
3. "Program Number" is 33 Revision CA0.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified.

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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601569-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

A297

RAL20L8

AMPERIF CORPORATION

REF NO.12, REV.0
J ?< SERAFIN, 6/12/86
1 ENBLD 5PWRDN 1EPRLOAD 1EPTRIG 1DRTRIG 1DRUNEND 1DRYRUN 5PURST 1MSTRT 5XRST
1EPLDEND GND 5EPADCEN 5MRSPLSE 5ELDRST NC NC 5BNDRT 5EACRST 5EADRCLR 5BDBSY
5EENLED 1ERLKUP VCC

/5EENLED = 1EPENBLD * 5BDBSY

/5BDBSY = 1EPRLOAD + 1EPTRIG + 1DRTRIG + 1DRUNEND + 1DRYRUN + /5PWRDN

/5EADRCLR = /5PURST + 1MSTRT + /5XRST + 1EPRLOAD * 5EPADCEN + 1EPLDEND

/5EACRST = /5MRSPLSE + /5XRST + 1EPLDEND + /5PURST + 1ERLKUP

/5BNDRT = /5MRSPLSE + /5XRST + 1ERLKUP + /5PURST

/5ELDRST = /5MRSPLSE + /5XRST + 1DRTRIG + /5PURST + 1ERLKUP + 1DRYRUN

P/N 1601569-001

33CA0

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DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXP MEM	D.
DRAWING NO. 1601569-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

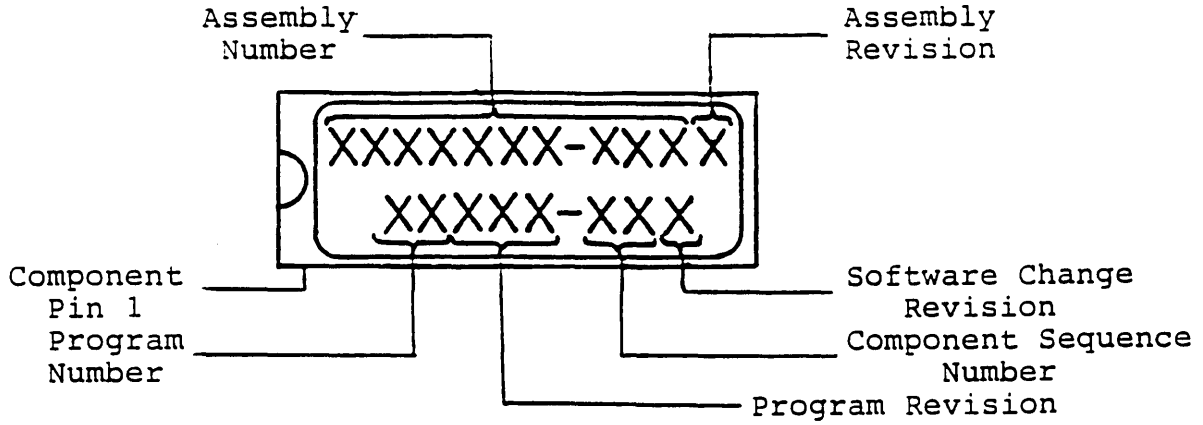
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # Z548 CR	7/25/89	[signature]

Procedure:

1. Program component using data filed in software no. 33BA0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U14.
   Used on PCBA 1602522-101 Location U97.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision BA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601568-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9263

PAL20L8 AMPERIF CORPORATION

REF NO.11, REV.0
JACK SERAFIN, 8/11/86
E)RCLR 5ELFG 5PRWTEN5 5XLFG 1PARER0 1PARER1 1PARER2 1PARER3 1PARER4 5PURST
GND GND GND GND NC NC NC 5NOPRST 5SERLED 5LERLED 1ERLKUP 5EBTCLR GND VCC

/5EBTCLR = /5EADRCLR + /5PRWTEN5

/1ERLKUP = /1PARER0 * /1PARER1 * /1PARER2 * /1PARER3 * /1PARER4

/5LERLED = 1ERLKUP * /5ELFG + 1ERLKUP * /5XLFG

/5SERLED = 1ERLKUP * 5ELFG * 5XLFG

/5NOPRST = /5PURST + 1ERLKUP

P/N 1601568-001

33BA0

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DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXP MEM	D
DRAWING NO. 1601568-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

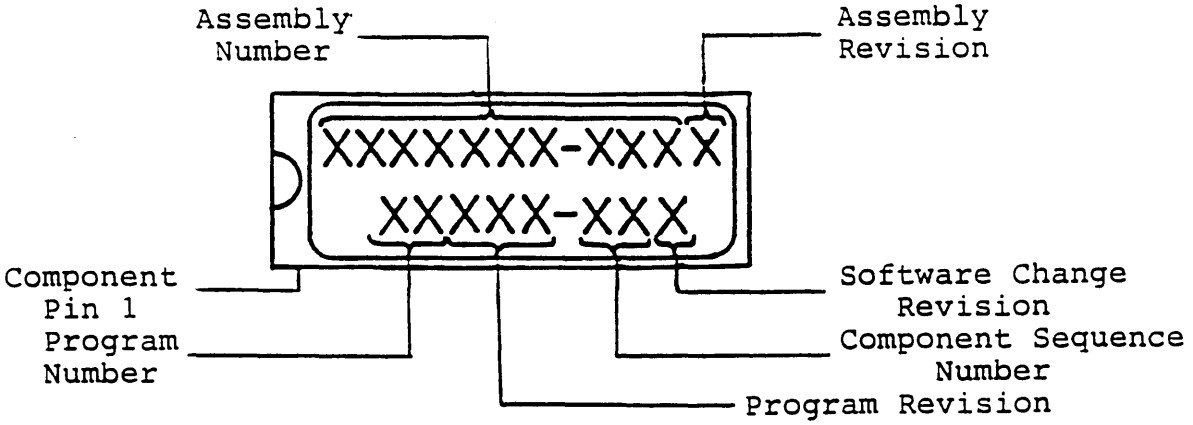
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
E	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	[signature]

Procedure:

1. Program component using data filed in software no. 33AA0-01B.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U13.
   Used on PCBA 1602522-101 Location U11.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is B.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision AA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

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PAL ASSEMBLY, EXP MEM

REV E

SIZE	DRAWING NO.	SHEET
A	1601567-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

REF NO.10, REV.1
JACK SERAFIN, 2/12/87
5PURST 5XRST 1MRST1 5MRST2 1ADCKC 1MONLN 2MENO 5BDBSY 5XONLN GND GND
GND GND GND 5XMCAE CKDY1 CKDY2 5ONLINE 5RSRST 1MSTRT 5MRSPLSE 5EXPR GND VCC

/5EXPR = /5PURST + /5MRSPLSE + /5XRST

/5MRSPLSE = 1MRST1 * 5MRST2 * CKDY2

/1MSTRT = /1MRST1 + /5MRST2 + 1ADCKC

/5RSRST = 1MONLN + /5PURST

/5ONLINE = 1MONLN * 5BDBSY + /5XONLN

/CKDY1 = 1ADCKC

/CKDY2 = CKDY1

/5XMCAE = /5ONLINE * 2MENO

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BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9254

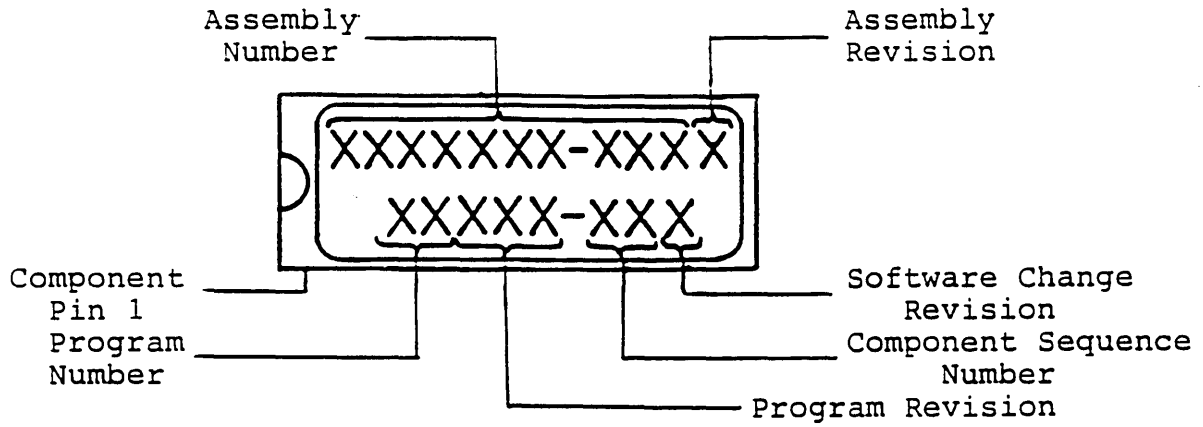
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33-A0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U12.
   Used on PCBA 1602522-101 Location U62.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision -A0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601566-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

TAS 9/25/86 6319

PAL20L8 AMPERIF CORPORATION

REF NO.9, REV.1
JACK SERAFIN, 8/25/86
1ADCEN 1ADCKC 1DRYRUN 1ONLINE 5XADEN1 5EPDATEN 1BP0 1BP1 1BP2 1BP3 1BP4 GND
6CLOCK2 5XSREN 5PARCEN 5MINSTE 5MIROTE NC NC 5IMPAE 5SRWE 5SRCS 1XCYC VCC

/5SRCS = 1SRADCEN * 1DRYRUN + 1ONLINE + /5XADEN1 + /5XSREN * /1ADCKC * /1BP0
* /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2 + /5EPDATEN * /1ADCKC
* /1BP0 * /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2

/5SRWE = /5XSREN * /1ADCKC * /1BP0 * /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2
+ /5EPDATEN * /1ADCKC * /1BP0 * /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2

/5IMPAE = GND

/5MIROTE = 1SRADCEN * 1DRYRUN + 1ONLINE + /5MINSTE + /5EPDATEN

/5PARCEN = /5EPDATEN * /1ADCKC + /5MINSTE + 1SRADCEN * 1DRYRUN * /1ADCKC
+ 1XCYC * /5XADEN1 * /1ADCKC + /5XSREN * /1ADCKC

P/N 1601566-001 33-A0

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DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXP MEM	D
DRAWING NO. 1601566-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9254

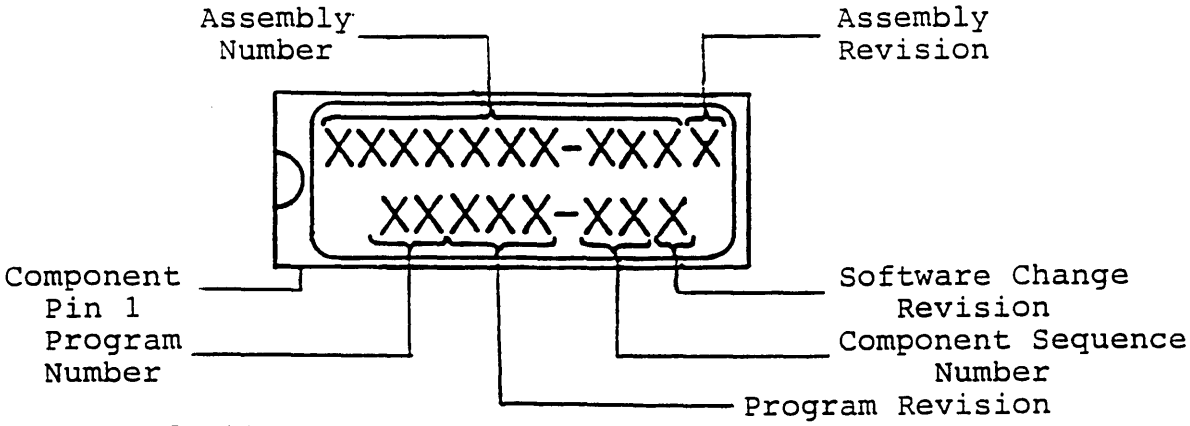
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - ECO # 2029 CR	8-4-89	MM

Procedure:

1. Program component using data filed in software no. 42AA0-01A.

2. Make from unprogrammed part number 20156600-001.

3. Used on PCBA 1601962-101,201,202 Location U136.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 42 Revision AA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

CHECKSUM = DE8D

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY,

XMCP1

REV A

SIZE	DRAWING NO.	SHEET
A	1602231-101	1 OF 3

BISHOP GRAPHICS/ACCUPRESS

```
Partno      0000-0000 ;
Date        04/APR/88 ;
Revision    01        ;
Designer    R.BUSTAMNTE;
Company     Amperif   ;
Assembly    XMC       ;
Location    U136   ;

/*****************************************************************************
 THIS PAL SET PARITY ERROR STATUS FOR ALL THE BUSSES,IT ALL PRESENT STATUS
ON THE ALU INPUT BUSS.



 *****************************************************************************
    Allowable Target Device Types:
 *****************************************************************************/

/** Re-define operators **/

$define :+: $           /* XOR operator                                      */
$define  +  #           /* OR  operator                                      */


/**  Inputs  **/

Pin 1    =   A        ;    /*                                                */
Pin 2    =  UPARERU   ;    /*                                                */
Pin 3    =  !HRCVGT2  ;    /*                                                */
Pin 4    =  UPARERL   ;    /*                                                */
Pin 5    =  !HRCVGT1  ;    /*                                                */
Pin 6    =  CTSDPE    ;    /*                                                */
Pin 7    =  !RDSPAD   ;    /*                                                */
Pin 8    =  CTSPDN    ;    /*                                                */
Pin 9    =  !CLK1     ;    /*                                                */
Pin 10   =  !CLK12    ;    /*                                                */
Pin 11   =  !CLEAR    ;    /*                                                */
Pin 18   =  !SMCSTEN  ;    /*                                                */


/**  Outputs  **/

Pin 23   =  !RSSMCB   ;    /*                                                */
Pin 22   =   UPERL    ;    /*                                                */
Pin 21   =   UPERU    ;    /*                                                */
Pin 20   =   CTSDPER  ;    /*                                                */
Pin 19   =   SPPER    ;    /*                                                */
Pin 17   =  !ALUO0    ;    /*                                                */
Pin 16   =  !ALUO1    ;    /*                                                */
Pin 15   =  !ALUO2    ;    /*                                                */
Pin 14   =  !ALUO3    ;    /*                                                */


/** Un-Used Pins **/
/*

*/


/** Declarations and Intermediate Variable Definitions **/
```

```
/**  Logic Equations  **/

 RSSMCB.D  =  SMCSTEN  ;
 RSSMCB.CK = !CLK1     ;
 RSSMCB.AR =  CLEAR    ;
 UPERL.D   = HRCVGT1 & UPARERL
           + !RSSMCB & UPERL & !CLEAR ;
 UPERL.CK  = !CLK1     ;
 UPERL.AP  =  CLEAR    ;
 UPERU.D   = HRCVGT2 & UPARERU
           + !RSSMCB & UPERU & !CLEAR ;
 UPERU.CK  = !CLK1     ;
 UPERU.AP  =  CLEAR    ;
 CTSDPER.D = CTSPDN
           + !RSSMCB & CTSDPER & !CLEAR ;
 CTSDPER.CK = !CLK1    ;
 CTSDPER.AP =  CLEAR   ;
 SPPER.D    = RDSPAD & CTSDPE
            + !RSSMCB & SPPER & !CLEAR ;
 SPPER.CK   = !CLK1    ;
 SPPER.AP   =  CLEAR   ;
 ALUO0.D    = HRCVGT1 & UPARERL
            + !RSSMCB & UPERL & !CLEAR ;
 ALUO0.CK   = !CLK1    ;
 ALUO0.AR   =  CLEAR   ;
 ALUO0.OE   =  SMCSTEN ;
 ALUO1.D    =  HRCVGT2 & UPARERU
            + !RSSMCB & UPERU & !CLEAR ;
 ALUO1.CK   = !CLK1    ;
 ALUO1.AR   =  CLEAR   ;
 ALUO1.OE   =  SMCSTEN ;
 ALUO2.D    =  CTSPDN
            + !RSSMCB & CTSDPER & !CLEAR ;
 ALUO2.CK   = !CLK1    ;
 ALUO2.AR   =  CLEAR   ;
 ALUO2.OE   =  SMCSTEN ;
 ALUO3.D    = RDSPAD & SPPER
            + !RSSMCB & SPPER & !CLEAR;
 ALUO3.CK   = !CLK1    ;
 ALUO3.AR   =  CLEAR   ;
 ALUO3.OE   =  SMCSTEN ;
```

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV.
PAL ASSEMBLY, XMCP1	A
DRAWING NO. 1602231-101	SHEET 3 OF 3

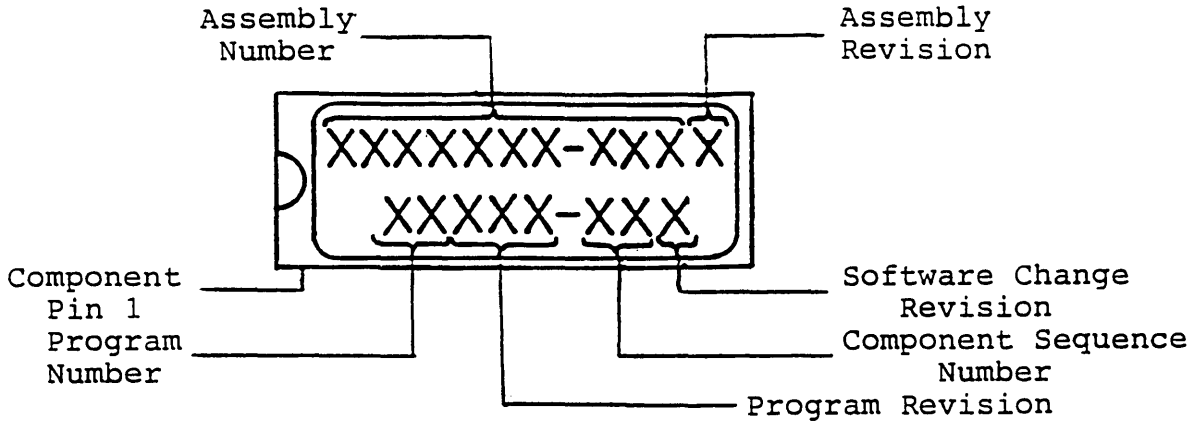
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - ECO # 2029 CR	8-4-89	MM

Procedure:

1. Program component using data filed in software no. 42-A0-01 A.

2. Make from unprogrammed part number 20156600-001.

3. Used on PCBA 1601962-101,201,202 Location U166.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 42 Revision -A0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

CHECKSUM = C517

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY,

XMCP0

REV A

SIZE	DRAWING NO.	SHEET
A	1602230-101	1 OF 3

```
Partno      0000-0000 ;
Date        05/APR/88 ;
Revision    01        ;
Designer    R.BUSTAMANTE;
Company     Amperif   ;
Assembly    XMC/PCB   ;
Location    U166       ;

/*************************************************************************
   THIS PAL DECODE AN SET HIO CONTROL TAGS. THE PAL IS PART OF THE XMC BOARD
 FOR THE NEW MULTI HOST SHARING.



 *************************************************************************
    Allowable Target Device Types: 20RA10
 *************************************************************************/


/** Re-define operators **/

$define :+: $           /* XOR operator                                  */
$define  +  #           /* OR  operator                                  */


/**  Inputs  **/

Pin 1    =  A         ;    /*                                            */
Pin 2    =  MINST21   ;    /*                                            */
Pin 3    =  MINST22   ;    /*                                            */
Pin 4    =  MINST23   ;    /*                                            */
Pin 5    =  MINST24   ;    /*                                            */
Pin 6    =  MINST25   ;    /*                                            */
Pin 7    = !HIOTCK3    ;   /*                                            */
Pin 8    = !HMODCK    ;    /*                                            */
Pin 9    =  SEQYB12   ;    /*                                            */
Pin 10   = !CLK1      ;    /*                                            */
Pin 11   = !CLEAR     ;    /*                                            */
Pin 17   =  MINST20   ;    /*                                            */
Pin 13   =   B        ;

/**  Outputs  **/

Pin 23   = !ODREQB    ;    /*                                            */
Pin 22   = !SETIDRB   ;    /*                                            */
Pin 21   = !EFREQB    ;    /*                                            */
Pin 20   = !HDRVGT    ;    /*                                            */
Pin 19   = !HIOTGT    ;    /*                                            */
Pin 18   = !HSIMGT    ;    /*                                            */
Pin 16   =  SEQAR12   ;    /*                                            */
Pin 15   = !ODREQ     ;    /*                                            */
Pin 14   = !SETIDR    ;    /*                                            */


/** Un-Used Pins **/
/*

*/


/** Declarations and Intermediate Variable Definitions **/
```

```
/**  Logic Equations  **/


ODREQB.D    =    MINST20 ;
ODREQB.CK   =   !HIOTCK3 ;
ODREQB.AR   =    CLEAR   ;
ODREQB.OE   =    HIOTGT  ;
SETIDRB.D   =    MINST21 ;
SETIDRB.CK  =   !HIOTCK3 ;
SETIDRB.AR  =    CLEAR   ;
SETIDRB.OE  =    HIOTGT  ;
EFREQB.D    =    MINST23 ;
EFREQB.CK   =   !HIOTCK3 ;
EFREQB.AR   =    CLEAR   ;
EFREQB.OE   =    HIOTGT  ;
HDRVGT.d    =   MINST20
            +    HDRVGT & !MINST21  ;
HDRVGT.CK   =   !HMODCK  ;
HDRVGT.AR   =    CLEAR   ;
HIOTGT.D    =   MINST22
            +    HIOTGT & !MINST23  ;
HIOTGT.CK   =   !HMODCK  ;
HIOTGT.AR   =    CLEAR   ;
HSIMGT.D    =    MINST24
            +    HSIMGT & !MINST25  ;
HSIMGT.CK   =   !HMODCK  ;
HSIMGT.AR   =    CLEAR   ;
SEQAR12.D   =   SEQYB12  ;
SEQAR12.CK  =   !CLK1    ;
ODREQ.D     =   MINST20  ;
ODREQ.CK    =   !HIOTCK3 ;
ODREQ.AR    =    CLEAR   ;
SETIDR.D    =   MINST21  ;
SETIDR.CK   =   !HIOTCK3 ;
SETIDR.AR   =    CLEAR   ;
```

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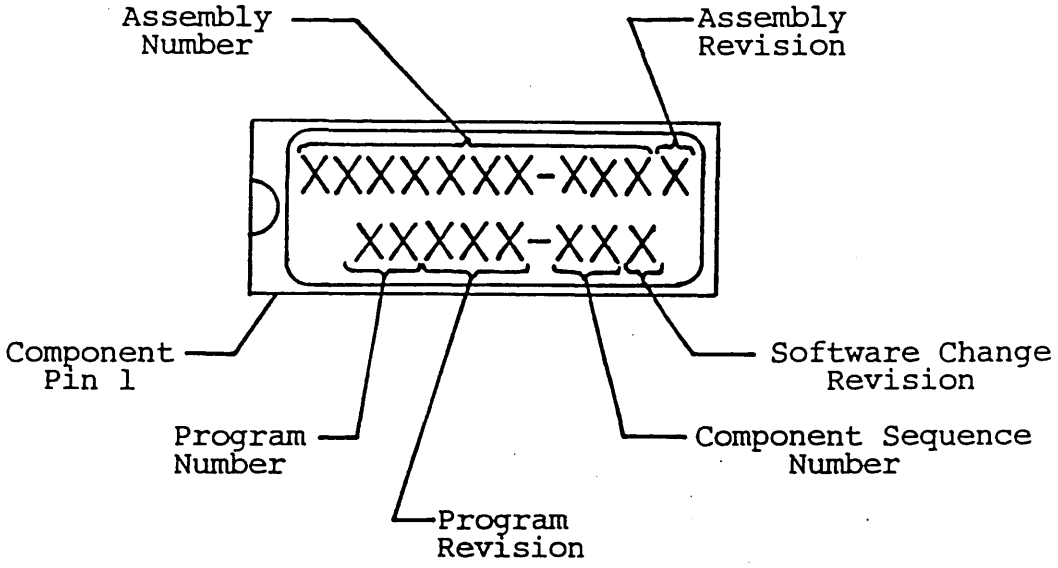
DOCUMENT TITLE	REV.
PAL ASSEMBLY, XMCP1	A
DRAWING NO. 1602230-101	SHEET 3 OF 3

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label MM	10-19-87	

Procedure:

1. Program component using data filed in software No. 36DA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location EA26



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision DA0 .
2. Make from unprogrammed part number 20051400 .
1. See separate parts list.

NOTES: Unless Otherwise Specified

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PAL ASSEMBLY, XMCIP@EA26

SIZE	DRAWING NO.	SHEET	REV
A	1601696-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PN 1601696-001
PAL16R4

SID 36DA0-01A
LOCATION EA26

```
/UA   /UB   /UC   /UD   /PA   /PB   /PC   /PC   BCT3  GND
BCT2  NC    BCT1  BCT0  /B3   MC2   /RW   /X    PE    VCC

(IF VCC)
X    = UA * PA * MC2 * B3 * /BCT3 * /BCT2 * /RW
     + UB * PB * MC2 * BCT0 * /BCT1 * BCT2 * /BCT3 * B3 * /RW
     + /UB * /PB * MC2 * BCT0 * /BCT1 * BCT2 * /BCT3 * B3 * /RW
     + UC * PC * MC2 * BCT0 * BCT1 * BCT2 * /BCT3 * /RW
     + /UC * /PC * MC2 * BCT0 * BCT1 * BCT2 * /BCT3 * /RW
     + UD * PD * MC2 * /BCT0 * /BCT1 * /BCT2 * /BCT3 * /RW
     + /UD * /PD * MC2 * /BCT0 * /BCT1 * /BCT2 * /BCT3 * /RW

(IF VCC)
/PE = /X * UA + /X * PA + /X * /MC2 + /X * /B3
     + /X * BCT2 + /X * BCT3 + /X * RW
```

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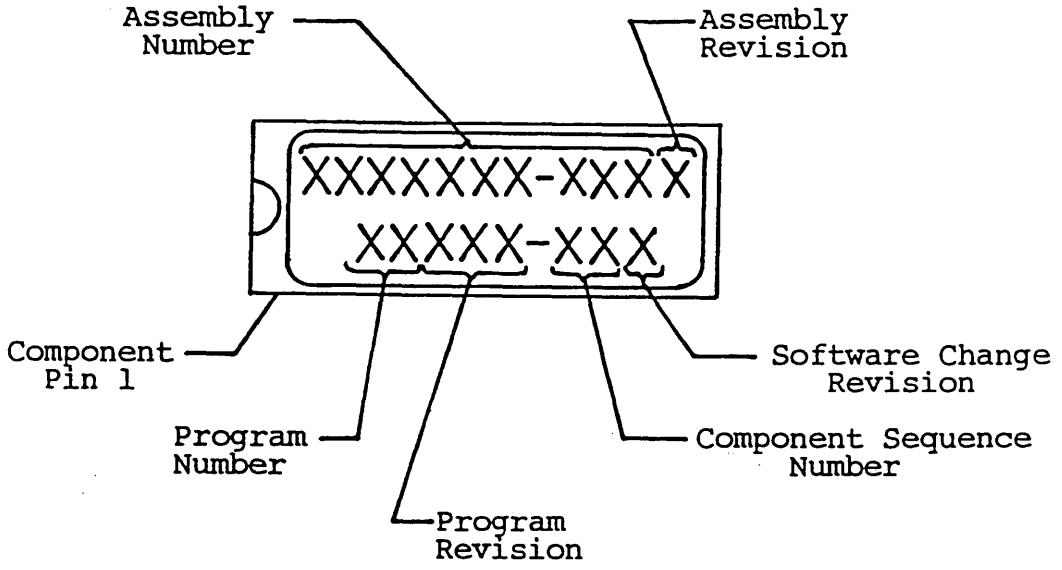
DOCUMENT TITLE	REV
PAL ASSY, XMCI @ EA26	B
DOCUMENT NUMBER 1601696-001	SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label MM	10-19-87	

Procedure:

1. Program component using data filed in software No. 36CA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location EA51



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision CA0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

NOTES: Unless Otherwise Specified

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PAL ASSEMBLY, XMCIP@EA51

SIZE	DRAWING NO.	SHEET	REV
A	1601695-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PN 1601695-001 SID 36CA0-01A
PAL16R4 LOCATION EA51

```
/CLK  /PU  /PL  /PA  /PB  /PC  /PD  /REG1  /REG2  GND
OE    UL   UU   /UD  /UC  /UB  /UA  /RW    NC     VCC

UA:   = REG1 & pu = /REG1 * UA

UB:   = REG1 * PL + /REG1 * UB

UC:   = REG2 * PU + /REG2 * UC

UD:   = REG2 * PL + /REG2 * UD

(IF VCC)
/UL   = PB * PD + PB * /REG2 + /REG1 * PD + /REG1 * /REG2

(IF VCC)
/UU   = PA * PC + PA * /REG2 + /REG1 * PC + /REG1 * /REG2
```

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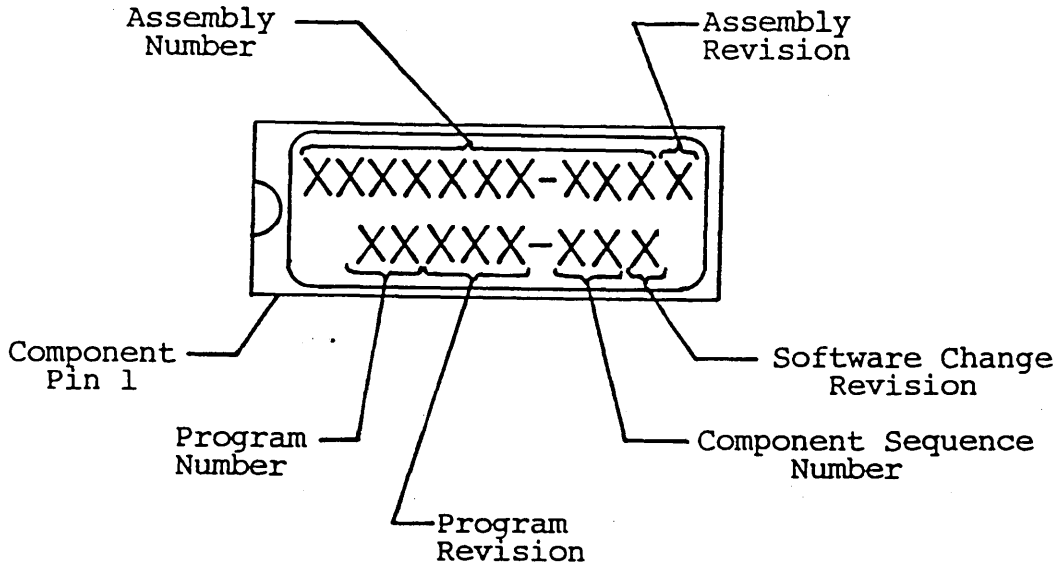
DOCUMENT TITLE: PAL ASSY, XMCI @ EA51 REV: B

DOCUMENT NUMBER: 1601695-001 SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label mm	10-19-87	

Procedure:

1. Program component using data filed in software No. 36BA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location EA37



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision BA0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

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PAL ASSEMBLY, XMCIP @EA37

SIZE	DRAWING NO.	SHEET	REV
A	1601694-001	1 OF 2	B

```
PN 1601694-001                                  SID 36BA0-01A
PAL16R4                                         LOCATION EA37


/CLK  /C    /D    /4U    /4L    BCT0  BCT1  BCT2  BCT3  GND
OE    /INC  /80   MC2    /MC1   /PD   /PC   /PDJ  /PCJ  VCC

MC1: = INC

/MC2:= /MC1

PC:   = 4L * BCT0 * /BCT1 * BCT2 * /BCT3 * MC1
      + 80 * /BCT0 * BCT1 * BCT2 * /BCT3 * MC1 * /PC
      + 4U * /C * BCT0 * BCT1 * BCT2 * /BCT3 * MC1 * /PC
      + /4U * C * BCT0 * BCT1 * BCT2 * /BCT3 * MC1 * /PC
      + PCJ
      + PC * /MC1

PD:   = D * BCT0 * BCT1 * BCT2 * /BCT3 * MC1
      + 80 * /BCT0 * /BCT1 * /BCT2 * BCT3 * MC1 * /PD
      + 80 * /BCT0 * /BCT1 * /BCT2 * /BCT3 * MC1 * /PD
      + PDJ
      + PD * /MC1
      + BCT3 * BCT2 * PD
      + /BCT1 * BCT0 * PD
      + BCT1 * /BCT0 * PD

(IF VCC)
PCJ   = /BCT0 * BCT1 * BCT2 * /BCT3 * 4U * 4L * MC1 * PC
      + /BCT0 * BCT1 * BCT2 * /BCT3 * /4U * /4L * MC1 * PC
      + BCT0 * BCT1 * BCT2 * /BCT3 * 4U * /C * MC1 * PC
      + BCT0 * BCT1 * BCT2 * /BCT3 * /4U * /C * MC1 * PC
      + /BCT3 * /BCT2 * PC
      + BCT3 * PC
      + /BCT1 * /BCT0 * PC

(IF VCC)
PBJ   = /BCT0 * /BCT1 * /BCT2 * BCT3 * 4U * 4L * MC1 * PD
      + /BCT0 * /BCT1 * /BCT2 * BCT3 * /4U * /4L * MC1 * PD
      + /BCT0 * /BCT1 * /BCT2 */BCT3 * 4U * 4L * MC1 * PD
      + /BCT0 * /BCT1 * /BCT2 * /BCT3 * /4U * /4L * MC1 * PD
      + BCT3 * BCT1 * BCT0 * PD
      + /BCT3 * /BCT2 * BCT1 * PD
      + /BCT3 * BCT2 * /BCT1 * PD
```

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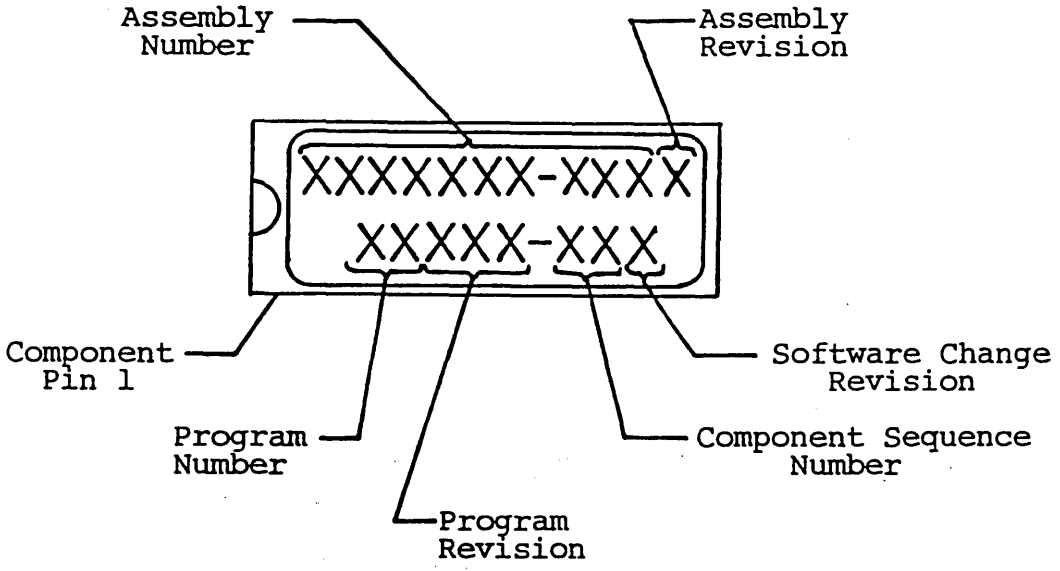
DOCUMENT TITLE	REV
PAL ASSY, XMCI @ EA37	B
DOCUMENT NUMBER 1601694-001	SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label MM	10-19-87	

Procedure:

1. Program component using data filed in software No. 36AA0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Used on 1120010-201-202 Location DL36



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision AA0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

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PAL ASSEMBLY, XMCIP@ DL36

SIZE	DRAWING NO.	SHEET	REV
A	1601693-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PN 1601693-001
PAL16R4

SID 36AA0-01A
LOCATION DL36

```
/CLK  /A   /B   /4U   /4L   BCT0  BCT1  BCT2  BCT3  GND
NC    /INC  NC   /B3   /MC1  /PB   /PA   /PBJ  /PAJ  VCC

MC1: = INC

B3:  = BCT0 * BCT1 * /BCT2 * /BCT3
     + /BCT0 * /BCT1 * BCT2 * /BCT3 * B3
     + BCT0 * /BCT1 * BCT2 * /BCT3 * B3

PA:  = 4L * /4U * BCT0 * /BCT1 * /BCT2 * /BCT3 * MC1
     + /4L * 4U * BCT0 * /BCT1 * /BCT2 * /BCT3 * MC1
     + 4L * /4U * /BCT0 * BCT1 * /BCT2 * /BCT3 * MC1 * /PA
     + /4L * 4U * /BCT0 * BCT1 * /BCT2 * /BCT3 * MC1 * /PA
     + A * BCT0 * BCT1 * /BCT2 * /BCT3 * MC1 * /PA
     + PAJ
     + PA * /MC1

PB:  = B * /4L * BCT0 * BCT1 * /BCT2 * /BCT3 * MC1
     + /B * 4L * BCT0 * BCT1 * /BCT2 * /BCT3 * MC1
     + 4L * /4U * /BCT0 * /BCT1 * BCT2 * /BCT3 * MC1 * /PB
     + /4L * 4U * /BCT0 * /BCT1 * BCT2 * /BCT3 * MC1 * /PB
     + 4U * BCT0 * /BCT1 * BCT2 * /BCT3 * MC1 * /PB
     + PBJ
     + PB * /MC1
     + BCT3 * PB

(IF VCC)
PAJ  = /BCT0 * BCT1 * /BCT2 * /BCT3 * 4U * 4L * MC1 * PA
     + /BCT0 * BCT1 * /BCT2 * /BCT3 * /4U * /4L * MC1 * PA
     + BCT0 * BCT1 * /BCT2 * /BCT3 * /A * MC1 * PA
     + BCT3 * PA
     + /BCT3 * BCT2 * PA
     + /BCT1 * /BCT0 * PA

(IF VCC)
PBJ  = /BCT0 * /BCT1 * BCT2 * /BCT3 * 4U * 4L * MC1 * PB
     + /BCT0 * /BCT1 * BCT2 * /BCT3 * /4U * /4L * MC1 * PB
     + BCT0 * /BCT1 * BCT2 */BCT3 * /4U * MC1 * PB
     + BCT1 * BCT2 * /BCT3 * PB
     + BCT1 * /BCT0 * PB
     + /BCT3 * /BCT2 * /BCT1 * PB
```

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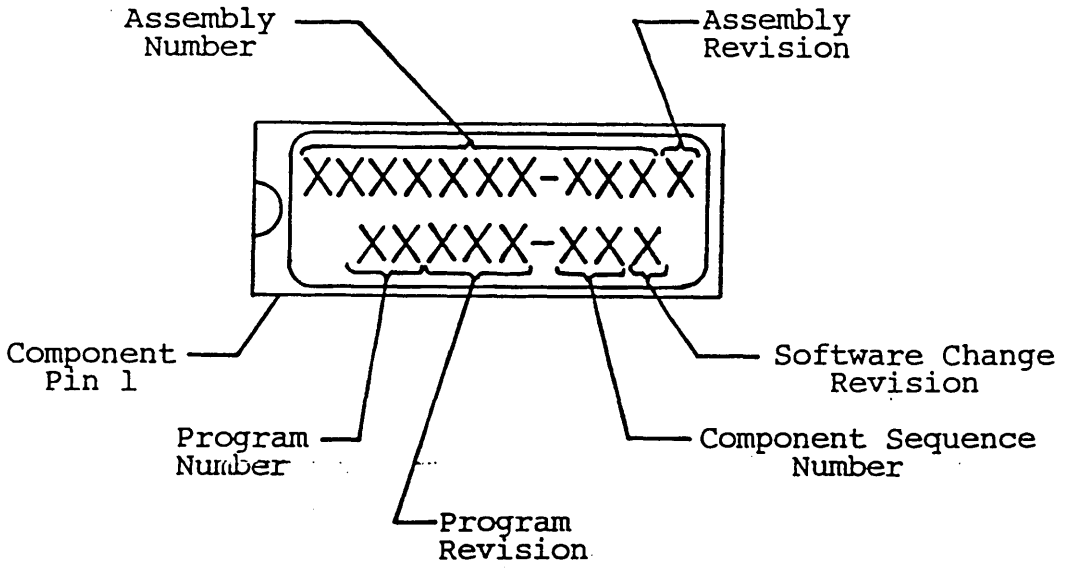
DOCUMENT TITLE	REV
PAL ASSY, XMCI @ DL36	B
DOCUMENT NUMBER 1601693-001	SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1269	1-21-87	
B	ECO 1408 Add label MM	10-19-87	

Procedure:

1. Program component using data filed in software No. 36-A0-01A .
2. Identify on adhesive-backed label per drawing below and affix label to programmed part as shown.
3. PCBA Useci on 1120010-201-202 Location DJ28



5. "SOFTWARE CHANGE Revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 36 Revision -A0 .
2. Make from unprogrammed part number 20051700 .
1. See separate parts list.

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PAL ASSEMBLY, XMCIP @ DJ28

SIZE	DRAWING NO.	SHEET	REV
A	1601692-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

PN 1601692-001
PAL16R4

SID 36-A0-01A
LOCATION DJ28

/CLK	/D0	/D1	/D2	/D3	/D4	/D5	/D6	/D7	GND
OE	/4L	/4U	/D	/C	/B	/A	/80	NC	VCC

```
A: = D7 * /D6 + /D7 * D6
B: = D5 * /D4 + /D5 * D4
C: = D3 * /D2 + /D3 * D2
D: = D1 * /D0 + /D1 * D0

4U = A * /B + /A * B
4L = C * /D + /C * D

80 = 4L * /4U + /4L * 4U
```

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DOCUMENT TITLE: PAL ASSY, XMCI @ DJ28

REV: B

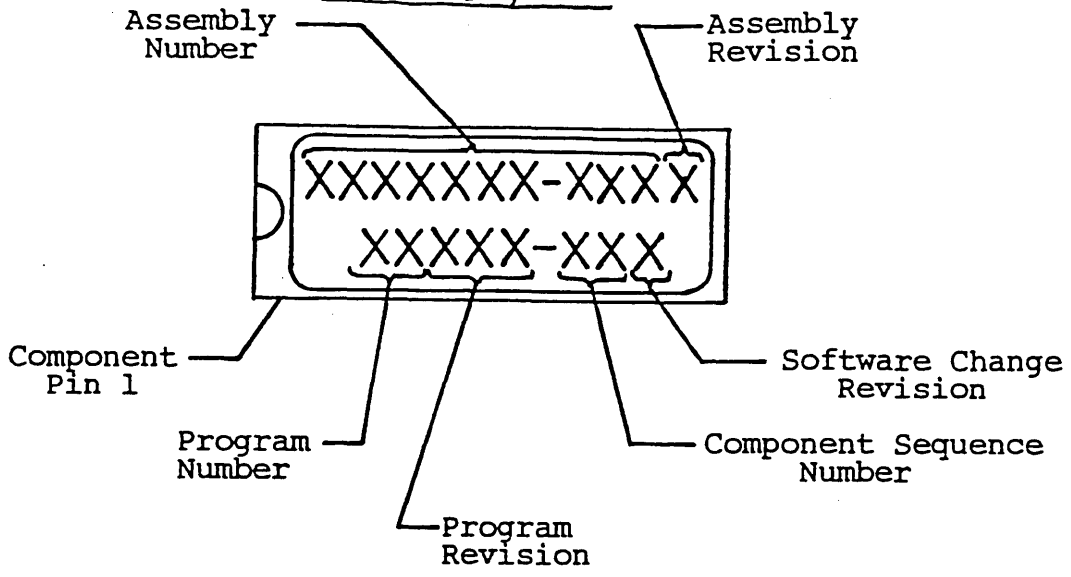
DOCUMENT NUMBER: 1601692-001

SHEET 2 OF 2

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	PROD REL SEE ECO 1270	2-23-87	CP
B	ECO1408 Add label MM	10-19-87	[illegible]

Procedure:

1. Program component using data filed in software No. 24CA0-01A .
2. Make from unprogrammed part number 20051700 .
3. PCBA Used on 1120012-301 / 1601553-201,-202 Location EA45



5. "Software change revision" is A .
4. "Component Sequence Number" is 01 .
3. "Program Number" is 24 Revision CA0 .
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY, DIFP, FIFO EMPTY CHECK (EA45)

SIZE	DRAWING NO.	SHEET	REV
A	1601662-001	1 OF 2	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

DIF FIFO EMPTY CHECK PAL

PN 1601662-001
SID 24CA0-01A

PAL16R4
LOCATION EA45

CONTROL/DRIVE SEQUENCER CHECK LOGIC

```
/C ECCI0 ECCI1 ECCI2 ECCI3 /OPCMPL /FMWRTM /DIFRST2 /CLK100 GND
/ENA /DR1CLK FIFOOR NC NC /EFIFOE /DIFSEQER TINDEX /CO VCC

DIFSEQER : = ECCI0 * ECCI1 * /ECCI2 * ECCI3 * /FMWRTM * FIFOOR *
             /DIFRST2

           + OPCMPL * FMWRTM * FIFOOR * /DIFRST2

           + EFIFOE * /DIFRST2

           + DIFSEQER * /DIFRST2

EFIOE : = ECCI0 * /ECCI1 * ECCI2 * ECCI3 * FMWRTM * TINDEX *
          /DIFRST2

        + EFIFOE * /DIFRST2

IF (VCC) CO = CLK100 * /FMWRTM
        + DR1CLK * FMWRTM
```

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV
PAL ASSY, DIF (FIFO EMPTY CHECK)	B
DOCUMENT NUMBER 1601662-001	SHEET 2 OF 2

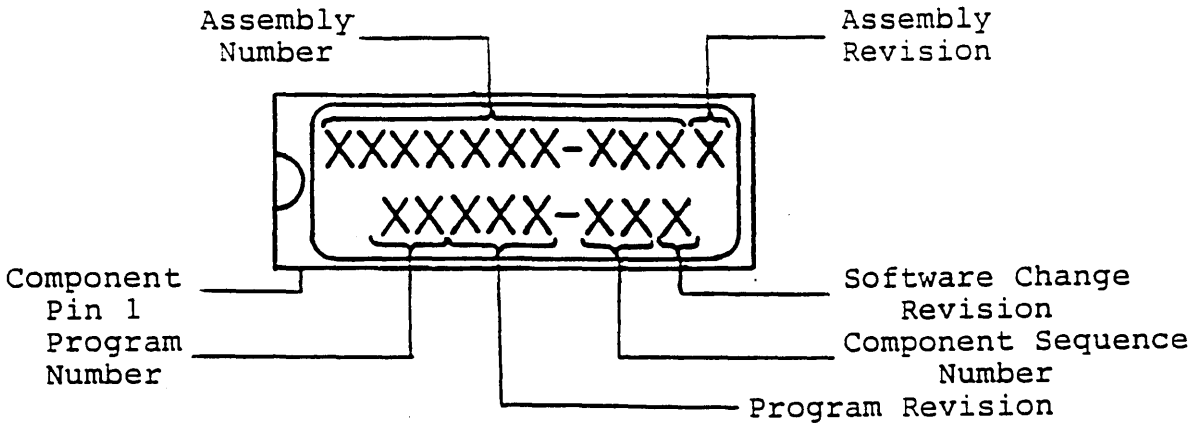
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33FA0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U18.
   Used on PCBA 1602522-101 Location U51.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision FA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	5/15/89
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OTHER	
APPROVED	

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amperif memory products

PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601572-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

3B/B

PAL20L8 AMPERIF CORPORATION

REF NO.15, REV.1
JACK SERAFIN, 8/25/86
5 EN 1ADCKC 5EPDATEN 1SRADCEN 1DRYRUN 1ONLINE 3FFF GND GND GND
GND GND GND GND NC NC NC NC 3FFFQ 5MILATE 5CADSEN 5OLLED GND VCC

/5OLLED = 5NOPEN

/5CADSEN = /5EPDATEN + 1SRADCEN * 1DRYRUN

/5MILATE = 1SRADCEN * 1DRYRUN * 1ADCKC + 1ONLINE + /5EPDATEN * 1ADCKC

/3FFFQ = /3FFF + /1DRYRUN

P/N 1601572-001 33FA0

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE PAL ASSEMBLY, EXP MEM	REV. D
DRAWING NO. 1601572-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

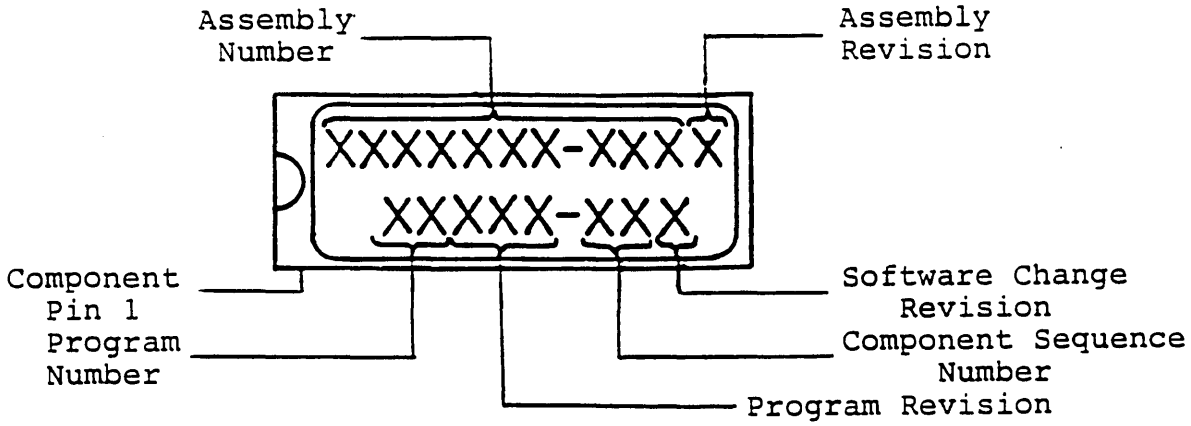
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33EA0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U17.
   Used on PCBA 1602522-101 Location U12.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision EA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

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PAL ASSEMBLY, EXP. MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601571-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

PAL20L8

AMPERIF CORPORATION

REF NO.14, REV.0
JACK SERAFIN, 6/12/86
E RUN 5XXACT 1EPLDEND 1EPENBLD 1MONLN 1MSTRT 1PUH 1PUL 5PURST 1EENSW
5XENSW GND GND GND NC NC NC NC 1ESWQ 5ESRST 1PWRUP 5DRTRIG GND VCC

/5DRTRIG = /5XDRUN + 1EPLDEND + /1EPENBLD * 5XXACT * /1MONLN * 1MSTRT

/1PWRUP = /1PUH + /1PUL

/5ESRST = 1MONLN + /5PURST + /5XXACT

/1ESWQ = /1EENSW + /5XENSW

P/N 1601571-001

33 EA0

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXP MEM	D
DRAWING NO. 1601571-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

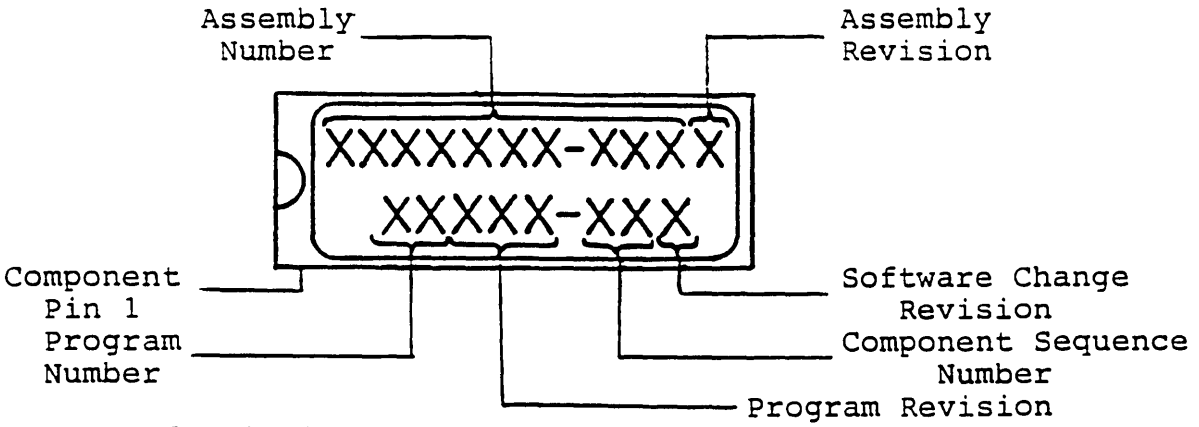
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33DA0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101, 201, 202 Location U16.
   Used on PCBA 1602522-101 Location U14.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision DA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	5/15/89
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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601570-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

667E

PAL20L8

AMPERIF CORPORATION

REF NO.13, REV.0
JACK SERAFIN, 6/12/86
RLOAD 5PURST 5MRSPLSE 1ERLKUP 5XRST 1DRUNEND 5EADRCLR 1MSTRT 1DRYRUN 3FFF
1PWRUP GND 5SRCNTEN 5EPDATEN 5EPTRIG 1EPENBLD 5XEPLD NC NC 1SRADCEN 5SADRCLR
5DRRST 1MONLN VCC

/5DRRST = 1EPRLOAD + /5MRSPLSE + /5PURST + 1ERLKUP + /5XRST + 1DRUNEND

/5SADRCLR = /5PURST + /5XRST + /5EADRCLR + 1MSTRT + 1DRYRUN * 5SRCNTEN
+ 3FFF * 1DRYRUN

/1SRADCEN = 5EPDATEN * 5SRCNTEN

/5EPTRIG = 1PWRUP * 1MONLN + 1PWRUP * 1EPENBLD + 1EPENBLD * 1MSTRT + /5XEPLD

P/N 1601570-001

33DA0

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DOCUMENT TITLE	REV.
PAL ASSEMBLY EXP MEM	D
DRAWING NO. 1601570-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

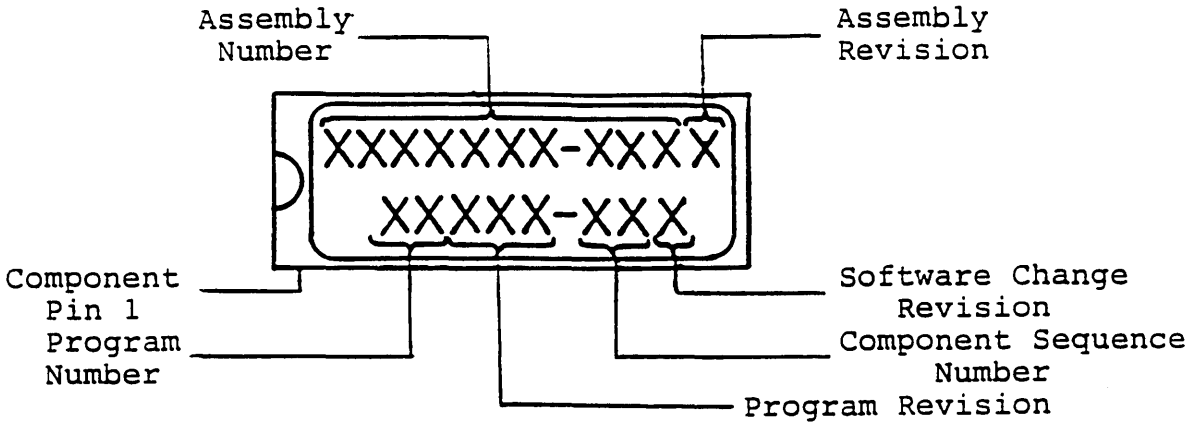
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # Z548 CR	7/25/89	[signature]

Procedure:

1. Program component using data filed in software no. 33CA0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U15.
   Used on PCBA 1602522-101 Location U15.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision CA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601569-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

RAL20L8

AMPERIF CORPORATION

REF NO.12, REV.0
J ?% SERAFIN, 6/12/86
1 ENBLD 5PWRDN 1EPRLOAD 1EPTRIG 1DRTRIG 1DRUNEND 1DRYRUN 5PURST 1MSTRT 5XRST
1EPLDEND GND 5EPADCEN 5MRSPLSE 5ELDRST NC NC 5BNDRT 5EACRST 5EADRCLR 5BDBSY
5EENLED 1ERLKUP VCC

/5EENLED = 1EPENBLD * 5BDBSY

/5BDBSY = 1EPRLOAD + 1EPTRIG + 1DRTRIG + 1DRUNEND + 1DRYRUN + /5PWRDN

/5EADRCLR = /5PURST + 1MSTRT + /5XRST + 1EPRLOAD * 5EPADCEN + 1EPLDEND

/5EACRST = /5MRSPLSE + /5XRST + 1EPLDEND + /5PURST + 1ERLKUP

/5BNDRT = /5MRSPLSE + /5XRST + 1ERLKUP + /5PURST

/5ELDRST = /5MRSPLSE + /5XRST + 1DRTRIG + /5PURST + 1ERLKUP + 1DRYRUN

P/N 1601569-001

33CA0

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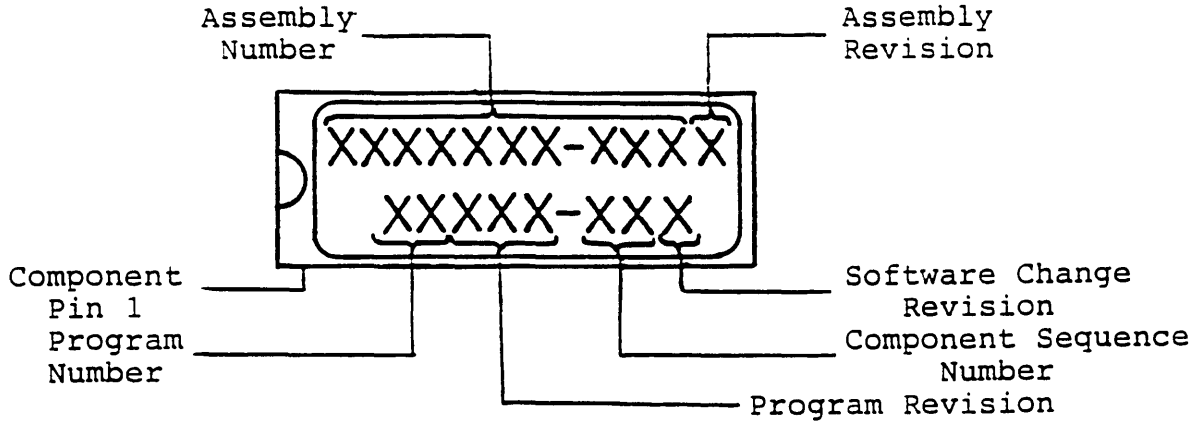
DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXP MEM	D
DRAWING NO. 1601569-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/21/89	[signature]

Procedure:

1. Program component using data filed in software no. 33BA0-01A.
2. Make from unprogrammed part number 20132100-001.
3. Used on PCBA 1601494-101,201,202 Location U14.
   Used on PCBA 1602522-101 Location U97.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.
5. "Software Change Revision" is A.
4. "Component Sequence Number" is 01.
3. "Program Number" is 33 Revision BA0.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601568-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

PAL20L8 AMPERIF CORPORATION

REF NO.11, REV.0
J^^K SERAFIN, 8/11/86
5)RCLR 5ELFG 5PRWTEN5 5XLFG 1PARER0 1PARER1 1PARER2 1PARER3 1PARER4 5PURST
GND GND GND GND NC NC NC 5NOPRST 5SERLED 5LERLED 1ERLKUP 5EBTCLR GND VCC

/5EBTCLR = /5EADRCLR + /5PRWTEN5

/1ERLKUP = /1PARER0 * /1PARER1 * /1PARER2 * /1PARER3 * /1PARER4

/5LERLED = 1ERLKUP * /5ELFG + 1ERLKUP * /5XLFG

/5SERLED = 1ERLKUP * 5ELFG * 5XLFG

/5NOPRST = /5PURST + 1ERLKUP

P/N 1601568-001

33BA0

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DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXP MEM	D
DRAWING NO. 1601568-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9254

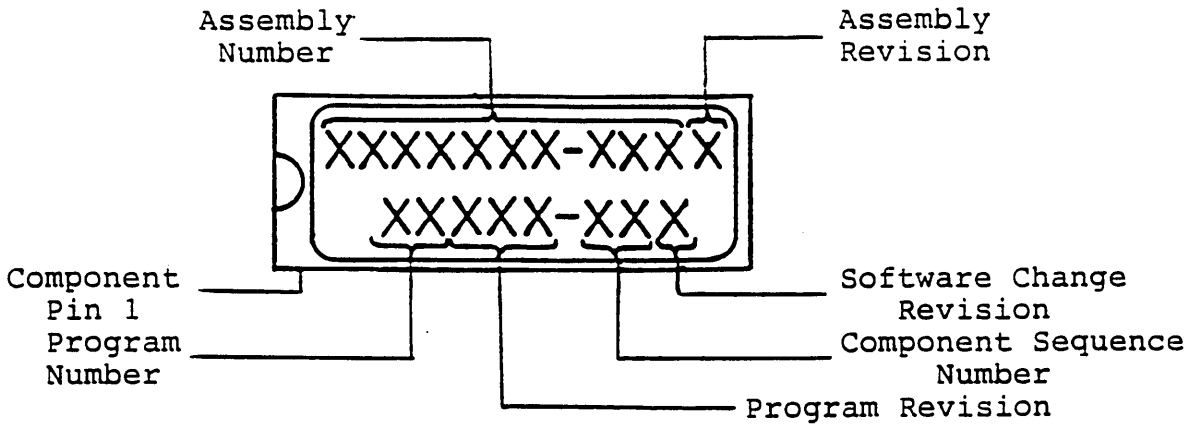
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
E	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	[signature]

Procedure:

1. Program component using data filed in software no. 33AA0-01B.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U13.
   Used on PCBA 1602522-101 Location U11.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is B.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision AA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	5/15/89
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PAL ASSEMBLY, EXP MEM

REV E

SIZE	DRAWING NO.	SHEET
A	1601567-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

REF NO.10, REV.1
JACK SERAFIN, 2/12/87
5PURST 5XRST 1MRST1 5MRST2 1ADCKC 1MONLN 2MENO 5BDBSY 5XONLN GND GND
GND GND GND 5XMCAE CKDY1 CKDY2 5ONLINE 5RSRST 1MSTRT 5MRSPLSE 5EXPR GND VCC

/5EXPR = /5PURST + /5MRSPLSE + /5XRST

/5MRSPLSE = 1MRST1 * 5MRST2 * CKDY2

/1MSTRT = /1MRST1 + /5MRST2 + 1ADCKC

/5RSRST = 1MONLN + /5PURST

/5ONLINE = 1MONLN * 5BDBSY + /5XONLN

/CKDY1 = 1ADCKC

/CKDY2 = CKDY1

/5XMCAE = /5ONLINE * 2MENO

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9254

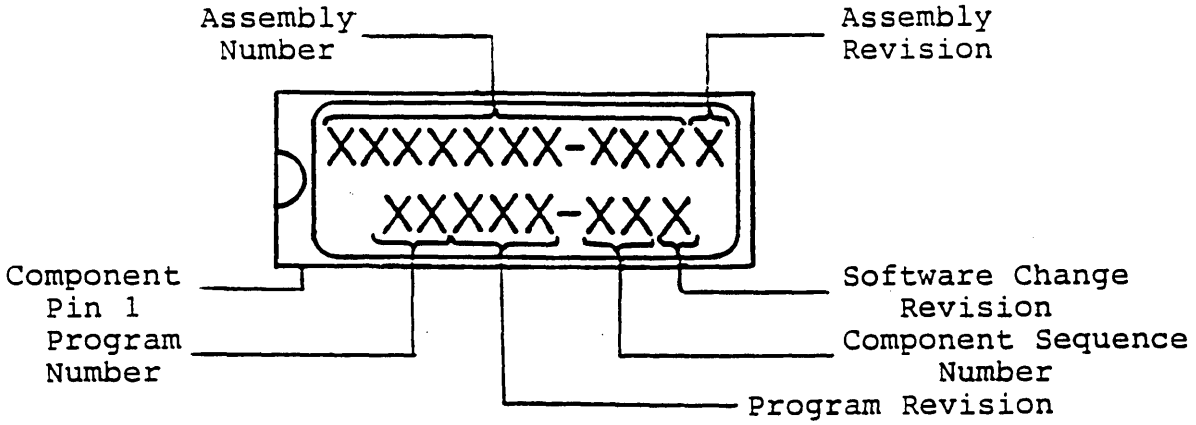
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
D	UPDATED & REDRAWN - ECO # 2548 CR	7/25/89	

Procedure:

1. Program component using data filed in software no. 33-A0-01A.

2. Make from unprogrammed part number 20132100-001.

3. Used on PCBA 1601494-101,201,202 Location U12.
   Used on PCBA 1602522-101 Location U62.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 33 Revision -A0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	5/15/89
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APPROVED	

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PAL ASSEMBLY, EXP MEM

REV D

SIZE	DRAWING NO.	SHEET
A	1601566-001	1 OF 2

BISHOP GRAPHICS/ACCUPRESS

JAS 9/25/86 6319

PAL20L8 AMPERIF CORPORATION

REF NO.9, REV.1
JACK SERAFIN, 8/25/86
1ADCEN 1ADCKC 1DRYRUN 1ONLINE 5XADEN1 5EPDATEN 1BP0 1BP1 1BP2 1BP3 1BP4 GND
6CLOCK2 5XSREN 5PARCEN 5MINSTE 5MIROTE NC NC 5IMPAE 5SRWE 5SRCS 1XCYC VCC

/5SRCS = 1SRADCEN * 1DRYRUN + 1ONLINE + /5XADEN1 + /5XSREN * /1ADCKC * /1BP0
* /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2 + /5EPDATEN * /1ADCKC
* /1BP0 * /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2

/5SRWE = /5XSREN * /1ADCKC * /1BP0 * /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2
+ /5EPDATEN * /1ADCKC * /1BP0 * /1BP1 * /1BP2 * /1BP3 * /1BP4 * /6CLOCK2

/5IMPAE = GND

/5MIROTE = 1SRADCEN * 1DRYRUN + 1ONLINE + /5MINSTE + /5EPDATEN

/5PARCEN = /5EPDATEN * /1ADCKC + /5MINSTE + 1SRADCEN * 1DRYRUN * /1ADCKC
+ 1XCYC * /5XADEN1 * /1ADCKC + /5XSREN * /1ADCKC

P/N 1601566-001 33-A0

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

DOCUMENT TITLE	REV.
PAL ASSEMBLY, EXPMEM	D
DRAWING NO. 1601566-001	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9254

ENGINEERING CHANGE REQUEST/ORDER

ECR [X] ECO [X]

ECR/ECO NO. 1760

PROJ. TITLE	HDW	SFTWR	IAI	CHANGE YES NO	CHANGE CLASS A B C D	FIELD YES NO	AMENDMENTS
CHIE(2A) (2E)	☐	☒	☐	IAL: E ☒ ☐	☒ ☐ ☐ ☐	☒ YES ☐ NO	

REQSTR/DRAWN: T. IGO (C. REYNOLDS)
DATE: 12-16-87
CHECKED BY: [signature]
DATE: 12-17-87

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST
☐ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☒ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: CACHE SYSTEMS: ① CORRECTS STACK ADJUSTMENT FOR AN UNRESETABLE FAULT AND "READ ONLY". ② CHECK FOR "READ ONLY" BEFORE PUSHING A TRACK OFF.

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
	22GA0	D	E	MICROCODE, XM16KP OP SYS
1601895-101	1601895-101	A	B	PROM ASSY, XM16KP OP SYS CODE
1601495-701	1601495-701	A	B	PCBA, PROM BD - XM16KP
1601495	N/A	A	B	CONFIGURATION LIST

CHANGES:

SEE SHEETS 2 THRU 8

INCORPORATION/DISPOSITION

INCORP. OF CHANGE DATE 12-18-87 SERIAL NO.

SPECIAL INSTRUCTION:

	USE	REWORK	SCRAP	NOTE:
IN FIELD	☐	☒	☐	
FIELD SPARES	☐	☒	☐	
FINISHED GOODS	☐	☒	☐	
FINAL ASSY	☐	☒	☐	
IN TEST	☐	☒	☐	
IN PROCESS	☐	☒	☐	
IN STOCK	☐	☒	☐	
NEXT ASSY	☐	☒	☐	
ON ORDER	☐	☒	☐	
NEXT BUY	☐	☒	☐	
OTHER	☐	☐	☐	

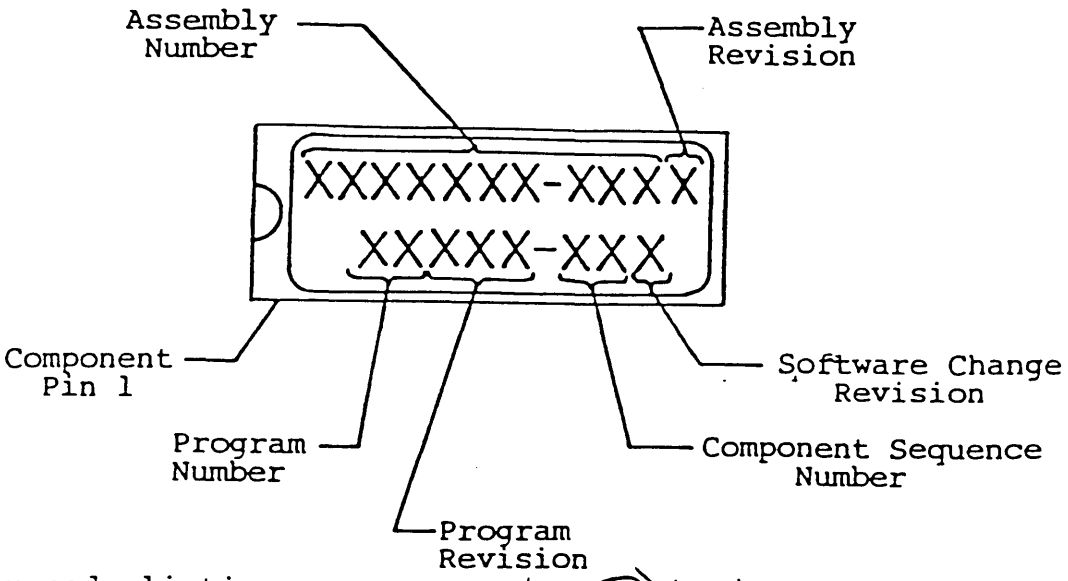
CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	[signature]	12/18/87
SFTWR	[signature]	
MARKETING	[signature]	12/18/87
MFG. ENG.	[signature]	12-18-87
QUALITY	[signature]	12/18/87
SERVICE	[signature]	12/18/87
ENG. SERV.	[signature]	12/18/87
DIR. OF ENG.		

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - SEE ECO # 1752		
B	ECO # 1760		

Procedure:

1. Program component using data filed in software No. 22GA0-01XE.
2. Make from unprogrammed part number 20131900-001.
3. Used on PCBA 1601495-701 Location U3



6. For code listing see separate printout.
5. "Software change revision" is XE.
4. "Component Sequence Number" is 01.
3. "Program Number" is 22 Revision GA0.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Reynolds	10/20/87
C[illegible]KER	
C[illegible]ER	
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PROM ASSEMBLY, XM16KP OP SYS

SIZE	DRAWING NO.	SHEET	REV
A	1601895-101	1 OF 1	B

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

DRAWING NUMBER

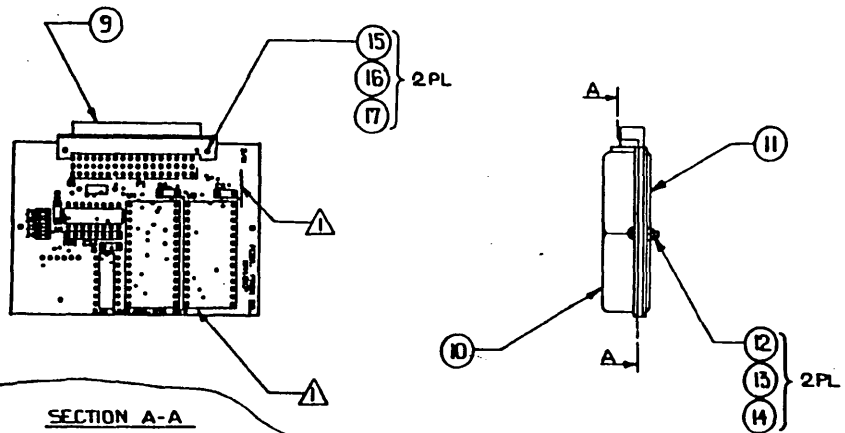
DRAWING NUMBER 1601495-701

NOTES: UNLESS OTHERWISE SPECIFIED -701

1. IDENTIFY ASSY AS PN 1601495-701, CURRENT REV LETTER AND S/N APPROX 1 YEAR BROWN.
2. FOR SCHEMATIC SEE DWG NO 1601495-201.

CHANGE: FROM -501 TO -701

AX	PROTO REL		
A	REL-ECO # 1732		
B	ECO # 1760		



SECTION A-A
(BOARD VIEW ONLY)

ADD:

REV	REWORK INSTRUCTIONS
B	REMOVE & REPLACE COMPONENT AT U3 USING PROM ASSY 1601895-101 REV B

SEE SEPARATE PL

CONFIDENTIAL DOCUMENT

amperif

PCB ASSEMBLY - XM16KP

DECK 10-15-92 | 1:1 | C | 1601495-701

DO NOT SCALE DRAWING

ECO # 1760 SHT 3 OF 8

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PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]							(FROM 1C5)		
WAS	00D7							(NOT USED)	
IS	050A	E 0	4 0	1 B	F 4	2 E	E5	SETPGE 1 & JPOP SEL31	
[redacted]									
WAS	01C5	E 0	4 0	1 B	F 4	2 E		SETPGE 1 & JPOP SEL31	
IS	0A9E	F F	F F	F B	F 0	D 7	FB	JPOP 11#D7	
[redacted]									
WAS	0737	F F	F F	F 3	3 1	1 2		BOZ RDONLYA	
IS	2B4A	F F	F F	F B	3 1	1 2	F9	CJPOP ALUZ, RDONLYA	
[redacted]							(FROM 1BCE)		
WAS	17F4							(NOT USED)	
IS	8FB8	E 0	4 0	3 1	F 4	C 0	E0	SETPGE 3 & JSR CHKAVALA	CHECK FOR WRITE DRIVE AVAIL.
[redacted]									
WAS	17F5							(NOT USED)	
IS	8FBE	4 5	0 5	0 F	0 0	1 0	EE	JSTPBIT R0, WRITPROT	IS THE DRIVE WRITE PROTECTED?

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: CACHE SYSTEMS: 1.) CORRECTS STACK ADJUSTMENT FOR AN UNRESETABLE FAULT AND "READ ONLY". 2.) CHECK FOR "READ ONLY" BEFORE PUSHING A TRACK OFF.

DATE
FINAL APPROVAL BY ENG.
NEW PROM REQD. YES
PROM NO. 01

DATE DEC. 16, 1987
INIT. BY Tom Gage
PAGE 4 OF 8
PCO # 22GA0-XXE
ECO# 1760

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
WAS	17F6							(NOT USED)	
IS	8FC4	E 0	4 0	3 B	3 C	D 7	E3	SETPGE 3 & CJPOP NALUZ, ERRETURN	YES, PUSH OFF ANOTHER
WAS	17F7							(NOT USED)	
IS	8FCA	3 7	1 E	E A	F 7	F F	E9	MOVE IREG, IREG & RTS	ELSE, RETURN
							(FROM 1D23)		
WAS	17F8								
IS	8FD0	4 5	0 5	0 F	0 0	1 0	EE	TSTRBIT R0, WRITPROT	IS THE DRIVE WRITE PROTECTED
WAS	17F9								
IS	8FD6	3 4	3 1	5 A	3 7	F F	E5	RTOR R1, R5 & CRTS ALUZ	IF NOT, RETURN
WAS	17FA								
IS	8FDC	E 0	4 0	3 B	F 4	9 4	E0	SETPGE 3 & JPOP WRITERR	ELSE, PUSH OFF ANOTHER

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. 01

DATE _____
INIT. BY _____

PCO # 22GA0-XXE
ECO# 1760

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]									
WAS	1BCE	F F	F F	F 1	F 4	E 0		JSR CHKAVALA	
IS	A6D4	E 0	4 0	2 1	F 7	F 4	E4	SETPGE 2 & JSR H#17F4	
[redacted]									
WAS	1D23	F F	F F	F A	F 7	F F		RTS	
IS	AED2	F F	F F	F E	1 7	F 8	FA	JMP H#17F8	
[redacted]									
WAS									
IS									
[redacted]									
WAS									
IS									
[redacted]									
WAS									
IS									

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. 01

DATE _____
INIT. BY _____
PAGE 6 OF 8
PCO # 22GA0-XXE
ECO # 1760

1601895-101 & 102

amperif

PROGRAM REVISION LOG

PROM I.D. 22GA0-XX- SYSTEM XM16KP CH1E OP SYS

PCO NUMBER	PCO DATE	L/F	PROM REVISION LEVEL -01	-02	-03	-04	-05	-06	-07	-08	-09	-10	-11	-12	-13	-14	-15	COMMENT
START	1732																	RELEASE
-XXA	10/20/87		A	A														
-XXB	1732 11/18/87		B															FOR SWALLOW 4.5 DRIVES! ADDS "NATIVE" BIT TO CONF BYTES FOR USE OF DDT LEVEL SR1. SWALLOW SYS ONLY - HOLD FOR NEXT CHG
-XXC	1732 12/1/87		C															①ADDITIONAL DATA COPY/ RESTORE xRB ERROR CHECKING ②CORRECTS xRB ERROR RETRY PROC
-XXD	1732 12/7/87		D															CACHE SYSTEMS: CORRECT POSSIBLE DATA CORRUPTION WHEN CHANGING FROM "WRITE-THRU" TO "BYPASS".
-XXE	1760 12/16/7		E															CACHE SYS: ①CORRECTS STACK ADJ FOR AN UNRESETTABLE FAULT AND "READ ONLY"; ②CHECK FOR "READ ONLY" BEFORE PUSHING A TRACK OFF.

COMBINED & 10 # 1760 SW7 003

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT.

REMARKS:

ADD

CORRECTION
FROM -601
TO -201

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	FIRST RELEASE	10-86	LR

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1601495-701	B	1601495-201	A	0601458-001	A	0601458-001	A	4	—		1760
1601495-701	A	1601495-201	A	0601458-001	A	0601458-001	A	4	—		1732
1601495-201	E	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1535
1601495-201	D	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1509
1601495-601	A	1601495-601	A	0601458-001	A	0601458-001	A	4	—		1600 (NP)
1601495-501	A	1601495-501	A	0601458-001	A	0601458-001	A	4	—		1542
1601495-401	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1534
1601495-401	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1479
1601495-301	D	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1452
1601495-301	C	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1427
1601495-301	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1417
1601495-301	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1406
1601495-201	C	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1383/4-87
1601495-201	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1372/
1601495-201	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1334/2-87
1601495-101	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—	HDW ADDED	1245/2-87
1601495-101	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROD REL	1135/3-86
1601495-101	AX	1601495-101	AX	0601458-001	AX	0601458-001	A	4	—	PROTOTYPE	7-86

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

SHT 8 OF 8 ECO # 1760

FORM 106-1-78

NEXT ASSY		
USED ON		
DR BY	L. RIVERA	10-86
CHK BY		
APPROVED BY		

CONFIGURATION LIST PCBA

XM16KP-D

SIZE	DWG NO.	
A	1601495	
SCALE NONE		SHEET 1 OF 1

ENGINEERING CHANGE REQUEST/ORDER

ECR ☒ ECO ☒

ECR/ECO NO. 1[illegible]

PROJ. TITLE	HDW	SFTWR	IAI	CHANGE LAL: YES NO	CHANGE CLASS A B C D	FIELD YES NO	AMENDMENTS
	☒	☐	☐	☐ ☒	☐ ☒ ☐ ☐	☐ ☒	

REQSTR/DRAWN C Clark 1-27
J Mottesheid

DATE: 1/27/88

CHECKED BY

DATE:

REASON FOR CHANGE

☒ DOM. DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☐ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☐ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: DRAWING PART LISTING FOR DWG CORR.

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
	16014995-101	B	C	XMTR KP - PROM. EV.
	-201	E	F	
	-401	B	C	
	-501	A	B	
	-601	B	E	
	-701	B	E	

REMOVE 20019513-004 QTY 2 SCREW PAN APH, 2-56 x 5/16, SWC

ADD 20019513-007 QTY 2 SCREW PAN APH, 2-56 x 1/2

INCORPORATION/DISPOSITION

	USE	REWORK	SCRAP
IN FIELD	☒	☐	☐
FIELD SPARES	☒	☐	☐
FINISHED GOODS	☒	☐	☐
FINAL ASSY	☒	☐	☐
IN TEST	☒	☐	☐
IN PROCESS	☒	☐	☐
IN STOCK	☒	☐	☐
NEXT ASSY	☒	☐	☐
ON ORDER	☐	☒	☐
NEXT BUY	☐	☒	☐
OTHER	☐	☐	☐

NOTE:

INCORP. OF CHANGE DATE 2-26-88 SERIAL NO.

SPECIAL INSTRUCTION:
MFG, COMPLIES

CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	SP	2/12/88
SFTWR		
MARKETING	JJH	2/18/88
MFG. ENG.	C Clark	2-18-88
QUALITY	A. Jamin	2/18/88
SERVICE	B. Bright	2/18/88
ENG. SERV.	[illegible]	2/19/88
DIR. OF ENG.		

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ENGINEERING CHANGE REQUEST/ORDER

ECR [X] ECO [X]

ECR/ECO NO. 1795

PROJ. TITLE	HDW	SFTWR	IAI	CHANGE YES NO	CHANGE CLASS	FIELD	AMENDMENTS
ALL CM	☐	☒	☐	LAL: H ☒ ☐	☒ A ☐ B ☐ C ☐ D	☒ YES ☐ NO	

REQSTR/DRAWN: TOM IGO (C REYNOLDS)
DATE: 1/13/88

CHECKED BY: [illegible]
DATE: 1-26-88

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☐ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☒ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: CACHE SYS: ①INHIBIT RELEASING AN XRB 'TRACK HOLD' ②RE-STORES R1 & R2. FIXES PROBLEM: ① 'READ BUFFERED RECORD' MAY NOT WORK ② FIXES SSS ERROR PAGING PROBLEM ③ CLEAR 'TRACK HOLD' FLAG IF DATA XFER IS TRUNCATED.

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
	22GA0	E (IF NOT LISTED)	H	MICROCODE, XM16KP OP SYS
1601895-101	1601895-101	B	C	PROM ASSY, XM16KP OP SYS
1601895-102	1601895-102	A	B	" " "
1601495-701	1601495-701	C	D	PCBA, PROM BD-XM16KP
1601495	N/A	C	D	CONFIGURATION LIST

900530-01C A

INCORPORATION/DISPOSITION

INCORP. OF CHANGE DATE 4-22-88 SERIAL NO.

	USE	REWORK	SCRAP	NOTE:
IN FIELD	☐	☒	☐	
FIELD SPARES	☐	☒	☐	
FINISHED GOODS	☐	☒	☐	
FINAL ASSY	☐	☒	☐	
IN TEST	☐	☒	☐	
IN PROCESS	☐	☒	☐	
IN STOCK	☐	☒	☐	
NEXT ASSY	☐	☒	☐	
ON ORDER	☐	☒	☐	
NEXT BUY	☐	☒	☐	
OTHER	☐	☐	☐	

SPECIAL INSTRUCTION: MUST BE INSTALLED CONCURRENT WITH ECO 1793.

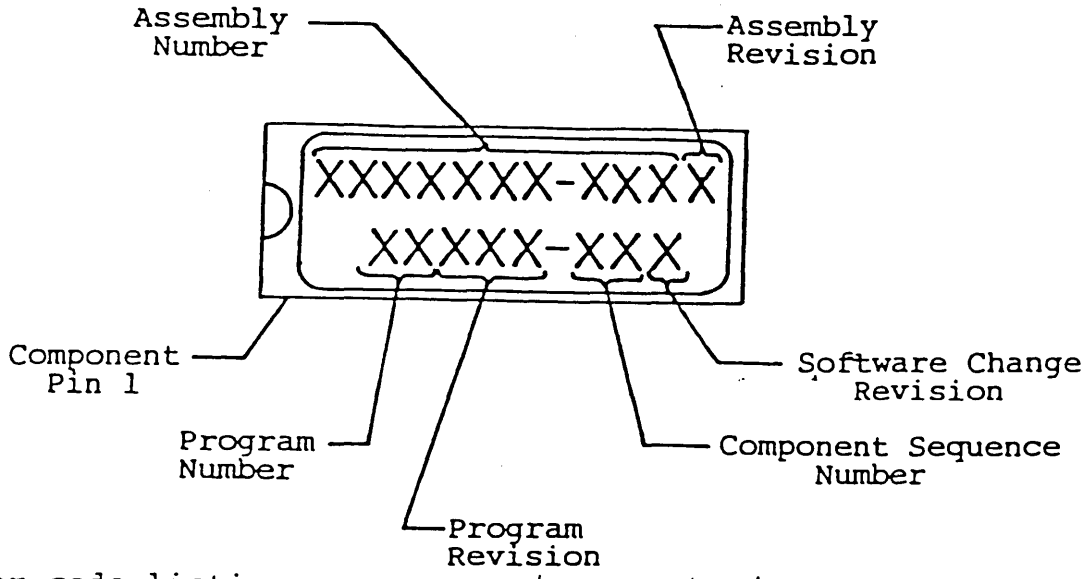
CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	GP [illegible]	2-11-88
SFTWR		
MARKETING	[illegible]	2-11-88
MFG. ENG.	[illegible]	4-20-88
QUALITY	[illegible]	2-11-88
SERVICE	[illegible]	2/11/88
ENG. SERV.	[illegible]	4/21/88
DIR. OF ENG.		

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - SEE ECO # 1732		
B	ECO # 1760 MM ECO # 1795	12-12-87	AHL

Procedure:

1. Program component using data filed in software No. 22GA0-01~~X~~ H.
2. Make from unprogrammed part number 20131900-001.
3. Used on PCBA 1601495-701 Location U3



6. For code listing see separate printout.
5. "Software change revision" is ~~X~~ H
4. "Component Sequence Number" is 01.
3. "Program Number" is 22 Revision GA0.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN C Reynolds	10/20/87
CHECKER	
APPROVED	

CONFIDENTIAL DOCUMENT
REPRODUCTION AND/OR DISCLOSURE OF THE INFORMATION CONTAINED HEREIN IS STRICTLY PROHIBITED WITHOUT PRIOR WRITTEN AUTHORIZATION BY AMPERIF CORP.

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PROM ASSEMBLY, XM16KP OP SYS

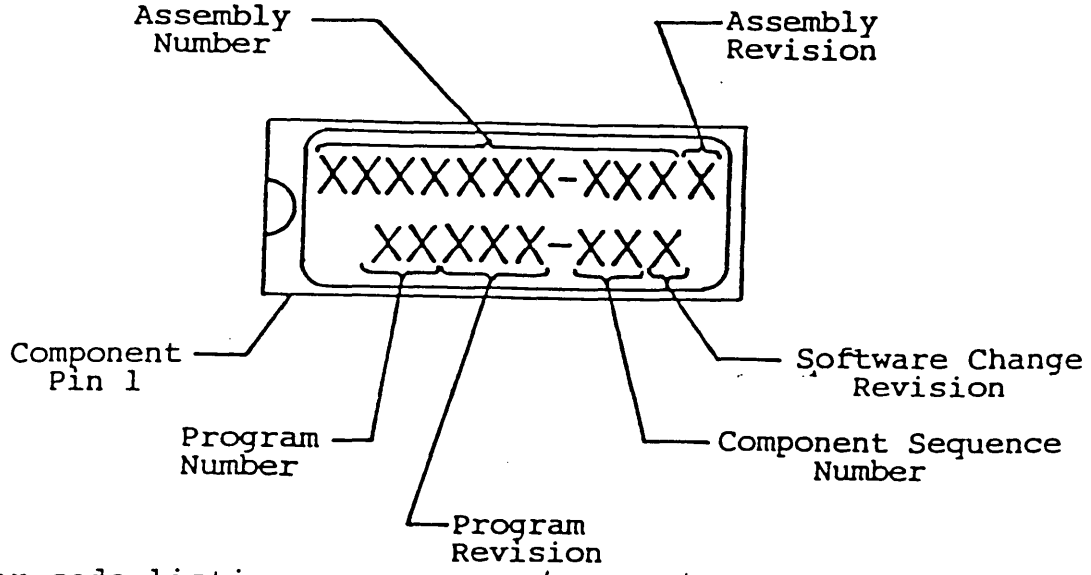
SIZE	DRAWING NO.	SHEET	REV
A	1601895-101	1 OF 1	~~X~~C

HISHOP GRAPHICS/ACCUPRESS REORDER NO. A-9253

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - SEE ECO # 1732 MM	12/15/87	[illegible]
B	ECO # 1795		

Procedure:

1. Program component using data filed in software No. 22GA0-02~~X~~G.
2. Make from unprogrammed part number 20131900-001.
3. Used on PCBA 1601495-701 Location U4



6. For code listing see separate printout.
5. "Software change revision" is ~~X~~G.
4. "Component Sequence Number" is 02.
3. "Program Number" is 22 Revision GA0.
2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.
1. See separate parts list.

NOTES: Unless Otherwise Specified

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN C Reynolds	10/20/87
CHECKER	
APPROVED	

CONFIDENTIAL DOCUMENT
REPRODUCTION AND/OR DISCLOSURE OF THE INFORMATION CONTAINED HEREIN IS STRICTLY PROHIBITED WITHOUT PRIOR WRITTEN AUTHORIZATION BY AMPERIF CORP.

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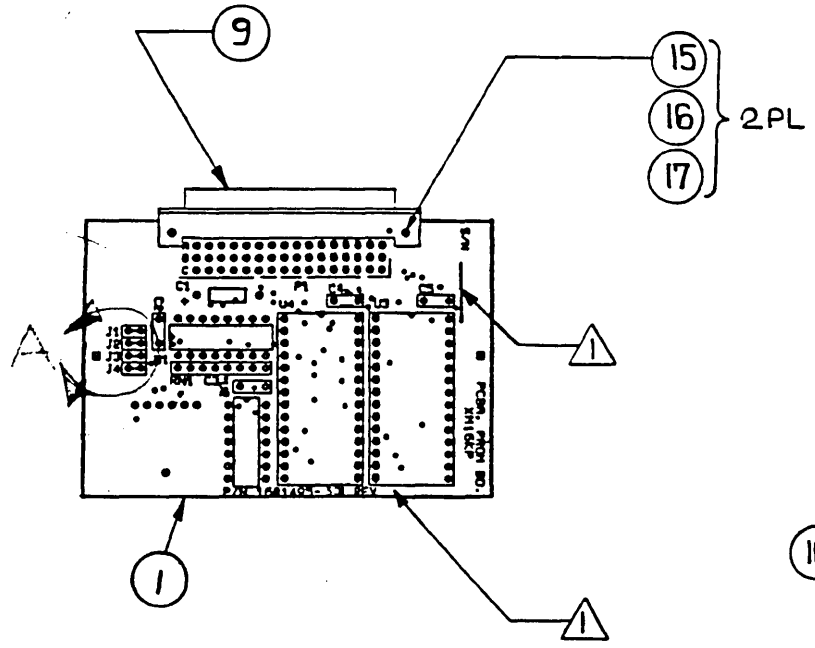
PROM ASSEMBLY, XM16KP OPSYS

SIZE	DRAWING NO.	SHEET	REV
A	1601895-102	1 OF 1	~~A~~B

HSHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9253

NOTES: UNLESS OTHERWISE SPECIFIED

1. IDENTIFY ASSY AS P/N 1601495-701 CURRENT REV LETTER AND S/N APPROX WHERE SHOWN.
2. FOR SCHEMATIC SEE DWG NO 1601495-~~701~~ —



SECTION A-A
(BOARD VIEW ONLY)

REV	REWORK INSTRUCTION ECO # 1760
B	1. REMOVE AND REPLACE COMPONENT AT U3 LOCATION USING PROM ASSY 1601895-101 REV.B
REV	REWORK ECO # 1795
C	1. REMOVE AND REPLACE COMPONENTS AT U3 AND U4 WITH 1601895-101 REV C AND 1601895-102 REV B.

ADD

1601495-701

BISHOP GRAPHICS/ACCUPRESS REORDER NO 44298

ECO 1795

SHT 4 OF 21 ~~SH 4 OF 11~~

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]							(FROM 1C2F)		
WAS	07DA							(NOT USED)	
IS	2F1C	34	12	FF	02	51	EC	ALDRAM F2,HOLDNBR	SAVE TRACK HOLD TRACK NUMBER
[redacted]									
WAS	07DB							(NOT USED)	
IS	2F22	35	34	3A	F0	08	F6	OR DB,B,MSK1 F3 & RTS HOLDTRK	SET TRACK HOLD BIT
[redacted]							(FROM 1BF8, 1BFD, 1C8C, 1C9A)		
WAS	0FFD							(NOT USED)	
IS	5FEE	37	10	FF	02	51	E4	RESETRAM HOLDNBR	CLEAR TRACK HOLD TRACK NUMBER
[redacted]									
WAS	0FFE							(NOT USED)	
IS	5FF4			FC	1C	53	F9	JMP WRITTER	
[redacted]									
WAS	1BF8	FF	FF	F1	F4	53		JSR WRITTRBR	
IS	17D0	E0	40	11	F7	F.D	E4	[illegible] 1 $ JSR WRITTD	

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: 1.) INHIBIT RELEASING AN XFB "TRACK HOLD" ON A TRACK NOT HELD BY THIS C.U.

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. -01

DATE JAN. 4, 1988
INIT. BY Tom Ogg
PAGE 5 OF 21
PCO # 22GA0-XXF
ECO # 1795

XM16K

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]									
WAS	1BFD	F F	F F	F 1	F 4	5 3		JSR WRITTRBR	
IS	A7EE	E 0	4 0	1 1	F 7	F D	E4	SETPGC 1 & JSR H#FFD	
[redacted]									
WAS	1C0C	F F	F F	F 1	F 4	5 3		JSR WRITTRBR	
IS	A848	E 0	4 0	1 1	F 7	F D	E4	SETPGC 1 & JSR H#FFD	
[redacted]									
WAS	1C12			F E	1 C	5 3		JMP WRITTRBR	
IS	A86C			F E	2 7	E B	FB	JMP H#27EB	
[redacted]									
WAS	1C2F	3 5	3 5	3 F	0 0	0 8		SETRBIT R3, HOLDTRK	
IS	A91A	E 0	4 0	0 1	F 7	D A	E0	SETPGC 0 & JSR H#7DA	
[redacted]									
WAS	1C9A	F F	F F	F 1	F 4	5 3		JSR WRITTRBR	
IS	AB9C	E 0	4 0	1 1	F 7	F D	E4	SETPGC 1 & JSR H#FFD	

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____ DATE _____
FINAL APPROVAL BY ENG. _____ INIT. BY _____
NEW PROM REQD. _____ PAGE 6 OF 21
PROM NO. -01 PCO # 22GA0-XXF
ECO # 1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32 31 24 23 16 15 09 08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]					
WAS	2013	F E 2 0 6 3		JMP SETSRB	
IS	C072	F E 2 7 E E	FB	JMP H#27EE	
[redacted]					
WAS	2022	F 1 F 0 6 2		JSR CLRWRTOP	
IS	C0CC	F 1 F 7 E D	F9	JSR H#27ED	
[redacted]					
WAS	2030	1 1 F 0 6 2		RESETR R1 & JSR CLRWRTOP	
IS	C120	1 1 F 7 E D	ED	RESETR R1 & JSR H#27ED	
[redacted]					
WAS	2061	F E 2 0 6 3		JMP SETSRB	
IS	C246	F E 2 7 E E	FB	JMP H#27EE	
[redacted]					
WAS	2074	1 1 F 0 6 2		RESETR R1 & JSR CLRWRTOP	
IS	C2B8	1 1 F 7 E D	ED	RESETR R1 & JSR H#27ED	

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. -01

DATE _____
INIT. BY _____
PAGE 7 OF 21
PCO # 22GA0-XX1
ECO # 1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32 31 24 23 16 15 09 08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
WAS	27E6	E 8		XOR AQ,B,R3,R3 & BOZ #+2	
IS	EF64	E A	FC	XOR AQ,B,R3,R3 & BOZ #+4	
WAS	27E7	E 0 4 0 3 1 F 2 8 8		SETPGE 3 & JSR DEPOSIT	
IS	EF6A	6 5 1 F 2 F 0 2 5 1	F0	XOR DB,TOUTL,RAMC,R2 & JCP HOLDNBR	THIS TRACK HELD BY THIS C.U?
WAS	27E8	F E 1 A 3 2		JMP CKPSEEK1	
IS	EF70	F 3 3 F E A	FE	BNZ #+2	NO, JUMP
WAS	27E9			(NOT USED)	
IS	EF76	E 0 4 0 3 1 F 2 8 8	E1	SETPGE 3 & JSR DEPOSIT	CLEAR TRACK HOLD FLAG
WAS	27EA				
IS	EF7C	F E 1 A 3 2	F8	JMP CKPSEEK1	CHECK NEXT ENTRY

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. -01

DATE _____
INIT. BY _____
PAGE 8 OF 21
PCO # 22GA0-XXF
ECO # 1795

YMICK

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]							(FROM 1C12)		
WAS	27EB							(NOT USED)	
IS	EF82	34	12	FF	02	51	EC	ALDRAM R2,HOLDNBR	SAVE TRACK HOLD TRACK NUMBER
[redacted]									
WAS	27EC							(NOT USED)	
IS	EF88			FE	1C	53	F9	JMP WRITFRBR	
[redacted]							(FROM 022, 2038, 2074)		
WAS	27ED							(NOT USED)	
IS	EF8E	55	35	3F	00	09	FF	RSTRBIT R3,WRITEOP+HOLDTRK	CLEAR WRITE OP./TRACK HOLD FLAGS
[redacted]							(FROM 2015, 2061)		
WAS	27EE							(NOT USED)	
IS	EF94	37	10	FF	02	51	E4	RESETRAM HOLDNBR	RESET TRACK HOLD TRACK NUMBER
[redacted]									
WAS	27EF							(NOT USED)	
IS	EF9A			FE	20	63	F9	JMP SETTRB	

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____ DATE _____

FINAL APPROVAL BY ENG. _____ INIT. BY _____

NEW PROM REQD. _____ PAGE 9 OF 21

PROM NO. -01 PCO # 22GA0-XX F

ECO # 1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
WAS	3091	43	3F	43	30	95		RESETR R4 & BOZ XRBCACHG	
IS	12366	FF	FF	F3	30	95	FF	BOZ XRBCACHG	
WAS	309F			FB	30	94		CJPOP ALUZ, XRBCACHF	
IS	123BA			F1	30	FC	FB	CJSR ALUZ, H#30FC	
WAS	30FC							(NOT USED)	
IS	125E8	35	34	4A	F2	0C	F1	OR DB, B, MSK1, F4 & RTS H#200	SET WMA WRITE ERROR
WAS									
IS									
WAS									
IS									

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: 2.) RESTORES R1 & R2 IF UNABLE TO WRITE XRB ENTRY INTO CACHE.

DATE _____ DATE _____

FINAL APPROVAL BY ENG. _____ INIT. BY _____

NEW PROM REQD. _____ PAGE 10 OF 21

PROM NO. -02 PCO # 22GA0-XXF

ECO # 1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]						-01F			
WAS	2784				04	B5		RTOR R10,R8 & JMP READ10	
IS	ED18				17	FB	EE	RTOR R10,R8 & JMP H#17FB	
[redacted]						-01F			
WAS	17FB							(NOT USED)	
IS	8FE2	B1	F0	0F	00	25	FE	WRTE HSSM,LDXMCJ & NOP H#25	PRESET MDB SM-ADDRESS
[redacted]						-01E			
WAS	17FC							(NOT USED)	
IS	8FE8	E0	40	01	F5	E6	E2	SETPGE 0 & JSR HSWAITR+1	DO IT & DELAY
[redacted]						-01E			
WAS	17FD							(NOT USED)	
IS	8FEE			FE	04	B5	F8	JMP READ10	
[redacted]						-02F			
WAS	31AA	FF	FF	F1	F3	2E		JSR SMBWRTB	
IS	129FC	E0	40	41	F3	2E	E7	SETPGE 4 & JSR SMBWRTB	

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. YES
PROM NO. -01, -02

DATE JAN. 13, 1988
INIT. BY Jon Iyer
PAGE 11 OF 21
PCO # 22GA0-XXG
ECO # 1795

CHANGE DESCRIPTION: 1) FIXES PROBLEM: 'READ BUFFERED RECORD' MAY NOT WORK UNDER SOME CONDITIONS. 2) FIXES S,S,S, ERROR PAGING PROBLEM

PCO #35DA0-D MUST BE INSTALLED WITH THIS P.C.O.

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GAØ

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32 31 24 23 16 15 09 08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]					
WAS	Ø462	F F		RESETRAM CASIISTAT	
IS	1A4C	Ø F	E5	MOVE ZERO, ZERO	
[redacted]					
WAS					
IS					
[redacted]					
WAS					
IS					
[redacted]					
WAS					
IS					
[redacted]					
WAS					
IS					

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: ③ CACHING SYSTEMS; CLEAR 'TRACK HOLD' FLAG IF DATA XFER. IS TERMINATED (IE. "READ IPL")

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. -01

DATE JAN, 27, 1988
INIT. BY Tom Joyce
PAGE 12 OF 21
PCO # 22GAØ-H
ECO# 1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22 GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32 31 24 23 16 15 09 08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]			(FROM 19F3)		
WAS	07DC			(NOT USED)	
IS	2F28	4 5 0 5 4 F 0 0 1 0	EA	TSTRBIT RA,10	NO VALID BIT STATUS?
[redacted]					
WAS	07DD			(NOT USED)	
IS	2F2E	6 0 3 4 4 3 3 7 D F	F0	XOR 1A,B,R4,R4 & BGZ *+2	YES, RESET IT; NO, JUMP
[redacted]					
WAS	07DE			(NOT USED)	
IS	2F34	3 7 3 5 3 F 0 0 1 0	EE	RDMSKB R3, SUSPEND	SUSPEND THIS ENTRY
[redacted]					
WAS	07DF			(NOT USED)	
IS	2F3A	E 6 0 0 2 F F F F F	EB	CTL FFB, ADRRST	
[redacted]					
WAS	07E0			(NOT USED)	
IS	2F40	E 0 4 0 3 1 F 2 8 8	E1	SETPGE 3 & JSR DEPOSIT	WRITE THIS ENTRY AT TOP OF STACK

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: 1.) ALLOW STATE CHANGE & PREVENT SYSTEM HANG IF XRB 'VALID' BIT IS EVER RESET.

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. -01

DATE JAN. 22, 1988
INIT. BY [signature]
PAGE 13 OF 21
PCO # 22GA01-H
ECO #1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]									
WAS	07E1							(NOT USED	
IS	2F46	55	34	4A	F0	10	F2	MASK DB,B,MSK1,R4 & RTS #10	RESET 'NO VALID BIT' & RETURN
[redacted]							(FROM 1ADC)		
WAS	07E2							(NOT USED)	
IS	2F4C	4505	4F	00	10		EA	TSTRBIT R4,10	NO VALID BIT STATUS?
[redacted]									
WAS	07E3							(NOT USED)	
IS	2F52	4514	1A	30	20		EA	AND DB,FOUTL,MSK1,R1 & CRTS ALIVE,VALI	RB NO, RETURN', CHK. VALID ENTRY
[redacted]									
WAS	07E4							(NOT USED)	
IS	2F58	6034	4F	FF	FF		F3	XOR AQ,B,R4,R4	RESET NO VALID BIT STATUS
[redacted]									
WAS	07E5							(NOT USED)	
IS	2F5E	E040	3B	F1	F.D		E0	SETPGE 3 & JSUP (LIKE STURT1	CHECK ANOTHER ENTRY

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____ DATE _____

FINAL APPROVAL BY ENG. _____ INIT. BY _____

NEW PROM REQD. _____ PAGE 14 OF 21

PROM NO. _____ PCO # 22GA0-XXH

ECO # 1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32 31 24 23 16 15 09 08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]			(FROM 1A18)		
WAS	07E6				
IS	2F64	F F F F F C 0 0 0 2	FE	LDCT 2	
[redacted]					
WAS	07E7				
IS	2F6A	4 5 0 5 4 F 0 0 1 0	EA	TSTRBIT R4,10	NO VALID BIT STATUS?
[redacted]					
WAS	07E8				
IS	2F70	6 0 3 4 4 A 3 7 F F	F1	XOR AQ,B,R4,R4 & CRTS ALU7	NO, RETURN; YES, RESET IT
[redacted]					
WAS	07E9				
IS	2F76	E 0 4 0 3 B F 2 2 2	E1	SETPGE 3 & JPUP SUBTUN02	CHECK ANOTHER ENTRY
[redacted]			(FROM 1A3C)		
WAS	07EA				
IS	2F7C	4 5 1 4 4 F 0 0 1 0	EA	AND DB,FOUTL,MSK1,R4 & NOP H#10	NO VALID BIT STATUS?

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____ DATE _____

FINAL APPROVAL BY ENG. _____ INIT. BY _____

NEW PROM REQD. _____ PAGE 15 OF 21

PROM NO. _____ PCO # 22GA0-X1H

ECO # 1795

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]									
WAS	07EB								
IS	2F82	60	05	FA	F7	FF	FD	XOR AQ,Q,R5 & CRTS ALU7	NO, RETURN; SAME UNIT?
[redacted]									
WAS	07EC								
IS	2F88	55	35	4F	00	10	FA	RSTRBIT R4,10	NEXT NO VALID BIT STATUS
[redacted]									
WAS	07ED								
IS	2F8E	E0	40	3B	F2	42	E1	SETPGE 3 & JPOP UNITCHKB	CHECK THE NEXT ENTRY
[redacted]							(FROM 1A47)		
WAS	07EE								
IS	2F94	45	05	4F	00	10	EA	TSTRBIT R4,10	NO VALID BIT STATUS?
[redacted]									
WAS	07EF								
IS	2F9A	45	04	3A	30	01	E6	AND OB,Q,MSK1,R3 & CRTS ALU2,WRITEOP	NO, RETURN; WRITE-OP?

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____ DATE _____

FINAL APPROVAL BY ENG. _____ INIT. BY _____

NEW PROM REQD. _____ PAGE 16 OF 21

PROM NO. _____ PCO # 22GA0-XXH

ECO #175

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PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]									
WAS	07F0							(NOT USED)	
IS	2FA0	55	35	4F	00	10	FA	RSTRBIT R4,10	RESET NO VALID BIT STATUS
[redacted]									
WAS	07F1							(NOT USED)	
IS	2FA6	E0	40	3B	F2	4B	E1	SETPGE 3 & JPOP H#1A4B	CHECK THE NEXT ENTRY
[redacted]									
WAS	19F3	E6	00	21	F2	88		CTL FRB,ADRRST & JSR DEPOSIT	
IS	9BB2	E0	40	01	F7	DC	E0	SETPGE 0 & JSR H#7DC	
[redacted]									
WAS	1A0C	45	14	1F	00	20		AND DB,FAULTL,MSK1,R1 & NOP VALFRB	
IS	9C48	E0	40	01	F7	E2	E1	SETPGE 0 & JSR H#7E2	
[redacted]									
WAS	1A18	FF	FF	FC	00	02		LDCT 2	
IS	9C90	E0	40	01	F7	E6	E0	SETPGE 0 & JSR H#7E6	

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____ DATE _____

FINAL APPROVAL BY ENG. _____ INIT. BY _____

NEW PROM REQD. _____ PAGE 17 OF 21

PROM NO. _____ PCO # 22GA0-XXH

ECO # 1775

amperif corporation

PROGRAM CHANGE ORDER
SYSTEM 22GA0

WAS / IS	ADD. HEX	MICRO CODE BIT POSITION 39 32	31 24	23 16	15 09	08 00	PARITY BYTE	ASSEMBLY STATEMENTS	COMMENTS
[redacted]									
WAS	1A3C	60	05	FF	FF	FF		XOR AG, G, R5	
IS	9D68	E0	40	01	F7	EA	E0	SETPGE 0 & JSR H# 7EA	
[redacted]									
WAS	1A47	45	05	3F	00	01		TSTRBIT R3, WRITEOP	
IS	9DAA	E0	40	01	F7	EE	E1	SETPGE 0 & JSR H#7EE	
[redacted]									
WAS	1AE6	37	3F	3A	F0	BA		RDREGB RAMC, R3 & RTS ILDFLG	
IS	A164	43	3F	4A	F7	FF	E9	RESETR R4 & RTS	
[redacted]									
WAS									
IS									
[redacted]									
WAS									
IS									

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE RESTRICTIONS ON THE TITLE PAGE OF THIS DOCUMENT

WAS: PROGRAM ADDR.
IS: PROM ADDR.

CHANGE DESCRIPTION: _____

DATE _____
FINAL APPROVAL BY ENG. _____
NEW PROM REQD. _____
PROM NO. _____

DATE _____
INIT. BY _____

PCO # 22GA0-XXH
ECO # 1795

1601895-101 & 102

amperif

PROGRAM REVISION LOG

PROM I.D. 22GA0-XX- SYSTEM XM16[illegible] CHIE OP SYS

PCO NUMBER	PCO DATE	L/F	PROM REVISION LEVEL -01	-02	-03	-04	-05	-06	-07	-08	-09	-10	-11	-12	-13	-14	-15	COMMENT
START -XXA	1732 10/20/87		A	A														RELEASE
-XXB	1732 11/15/87		B															FOR SMALLOC "S DRIVES: ADDS "NATIVE" BIT TO CONFIG BYTES FOR USE OF DOT LEVEL SPI. SMALLOC SYS ONLY - HOLD FOR NEXT CHG
-XXC	173[illegible] 12/1/87		C															①ADDITIONAL DATA COPY/ RESTORE XRB CRC CHECKING ②CORRECTS XRB ERROR RETRY PROC
-XXD	1732 12/7/87		D															CACHE SYSTEMS: CORRECT POSSIBLE [illegible] CONDITION [illegible] CHANGING VIA [illegible] "WRITE TAG" TO "BYPASS".
-XXE	1760 12/16/7		E															CACHE SYS: ①CORRECTS STACK ADJ FOR AN UNRESETTABLE FAULT AND "READ ONLY" ②CHECK FOR "READ ONLY" BEFORE PUSHING A TRACK OFF.
-XXF	~~1780~~ 1795 1/4/8		F	F														CACHE SYS: ① INH RELEASE XRB "TRACK HOLD" WHEN NOT HELD BY THIS CU ② RESTORES R1/R2 IF UNABLE TO WRITE XRB ENTRY TO CACHE.
-XXG	1795 11/3/88		G	G														①FIXES PROBLEM: "READ BUFFERED RECORD" MAY NOT WORK UNDER SOME CONDITIONS ②FIXES ESS ERROR PAGING PROBLEM
-XXH	1795 11/27/8		H	1														①CACH SYS - CLEAR 'TRACK HOLD' FLAG IF DATA XFER IS TRUNCATED (EG "READ IPL") ②ALLOW STATE CHG TO PREVENT SYS HANG IF XRB 'VALID' BIT IS EVER RESET.

COMBINED

ECO #1795 SHT 1 OF 21

USE OR DISCLOSURE OF THIS DATA IS SUBJECT TO THE

REMARKS:

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	FIRST RELEASE	10-86	L.R

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1601495-701	B	1601495-701	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1760 04/
1601495-701	A	1601495-701	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1732 04/
1601495-601	B	1601495-601	A	0601458-001	A	0601458-001	A	4	—		1740
1601495-201	E	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1535
1601495-201	D	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1509
1601495-601	A	1601495-601	A	0601458-001	A	0601458-001	A	4	—		1600 (4/
1601495-501	A	1601495-501	A	0601458-001	A	0601458-001	A	4	—		1542
1601495-401	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1534
1601495-401	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1479
1601495-301	D	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1452
1601495-301	C	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1427
1601495-201	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1417
1601495-301	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—		1406
1601495-201	C	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1383/4-87
1601495-201	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1372/
1601495-201	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROM CHANGE	1334/2-87
1601495-101	B	1601495-101	A	0601458-001	A	0601458-001	A	4	—	HDW ADDED	1295/2-87
1601495-101	A	1601495-101	A	0601458-001	A	0601458-001	A	4	—	PROD REL	1135/3-86
1601495-101	AX	1601495-101	AX	0601458-001	AX	0601458-001	A	4	—	PROTOTYPE	7-86

ECO # 1795

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

FORM 100-1-78

NEXT ASSY		
USED ON		
DR BY	L. RIVERA	10-86
CHK BY		
APPROVED BY		

CONFIGURATION LIST PCBA

XM16KP-D

SIZE	DWG NO.	
A	1601495	
SCALE NONE		SHEET 1 OF * 2

SHEET 26 OF 27

REMARKS:

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

ADD

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1601495-701	C	1601495-101	A	0601458-001	A	0601458-001	A	4	-	PROM CHG	1795

ECO # 1795 SHEET 21 OF 21

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

FORM 106-1-78

NEXT ASSY

USED ON

DR BY

CHK BY

APPROVED BY

CONFIGURATION LIST PCBA

XM16KP-D

SIZE A

DWG NO. 1601495

SCALE NONE

SHEET 2 OF 2

ENGINEERING CHANGE REQUEST/ORDER

ECR ☒ ECO ☐

ECR/ECO NO. 2604

PROJ. TITLE	HDW	SFTWR	IAI	CHANGE LAL:	CHANGE CLASS	FIELD	AMENDMENTS
9200 MULTI HOST	☒	☐	☐	YES ☒ NO ☐	☒ A ☐ B ☐ C ☐ D	☒ YES ☐ NO	

REQSTR/DRAWN: L. RIVERA JK 4-14-89
DATE: 4-14-89

CHECKED BY: B. Williams
DATE: 4-17-89

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☒ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☐ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: NOISE ON MINSTXX LINES BEING COUPLED & AMPLIFIED TO INSTXY LINES CAUSING XRB PARITY ERRORS IN CACHE SYSTEMS.

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
1601962-301	—	A	B	ASSY DWG. / XMC
1601962-401	1601962-401	NEW	A	PCBA, PL / XMC
1601962-302	—	A	B	ASSY DWG. / XMC
1601962-402	1601962-402	NEW	A	PCBA, PL / XMC
1601962-402	—	NEW	A	SCHEMATIC / XMC
1601962	—	G	H	CONFIGURATION LIST
59200103-FRU	—	R	S	9200-10 DUAL CTLR FRU LIST
1602159-001	—	M	N	9200 DISK CTLR CARD KIT
1602159-201	—	L	M	PCBA KIT CTLR S/N 227, 229,

INCORPORATION/DISPOSITION

INCORP. OF CHANGE DATE 4-21-89 SERIAL NO. ~~231~~, 233

SPECIAL INSTRUCTION: THIS ECO MUST BE ~~set~~ up CONCURRENT WITH ECO 2613

	USE	REWORK	SCRAP	NOTE:
IN FIELD	☐	☒	☐	FCO 9200-006
FIELD SPARES	☐	☒	☐	
FINISHED GOODS	☐	☒	☐	
FINAL ASSY	☐	☒	☐	
IN TEST	☐	☒	☐	
IN PROCESS	☐	☒	☐	
IN STOCK	☐	☒	☐	
NEXT ASSY	☐	☒	☐	
ON ORDER	☐	☒	☐	
NEXT BUY	☐	☒	☐	
OTHER ENTERED	☐	☒	☐	

CCB APPROVAL AND RESPONSIBILITY

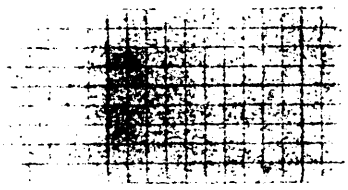
ENGINEERING	[signature]	4/20/89
SFTWR		
MARKETING	N/A	
MFG. ENG.	[signature]	4-20-89
QUALITY	A. Tamaji	4-20-89
SERVICE	[signature]	4/20/89
ENG. SERV.	[signature]	4/20/89
DIR. OF ENG.		

SHEET 1 OF 13

	ENGINEERING CHANGE REQUEST/ORDER	ECR/ECO NO. 2604

REWORK INSTRUCTIONS ON 1601962-301 REV A &
1601962-302 REV A

1. REMOVE IC @ LOC. U19, U45 & U72 (74F368).
2. INSTALL IC (74368 PN 20122400-001) @ LOC. U19, U45 & U72.
3. REIDENTIFY 1601962-301 REV A
   AS 1601962-401 REV A.
4. REIDENTIFY 1601962-302 REV A
   AS 1601962-402 REV A



NOTES: UNLESS OTHERWISE SPECIFIED

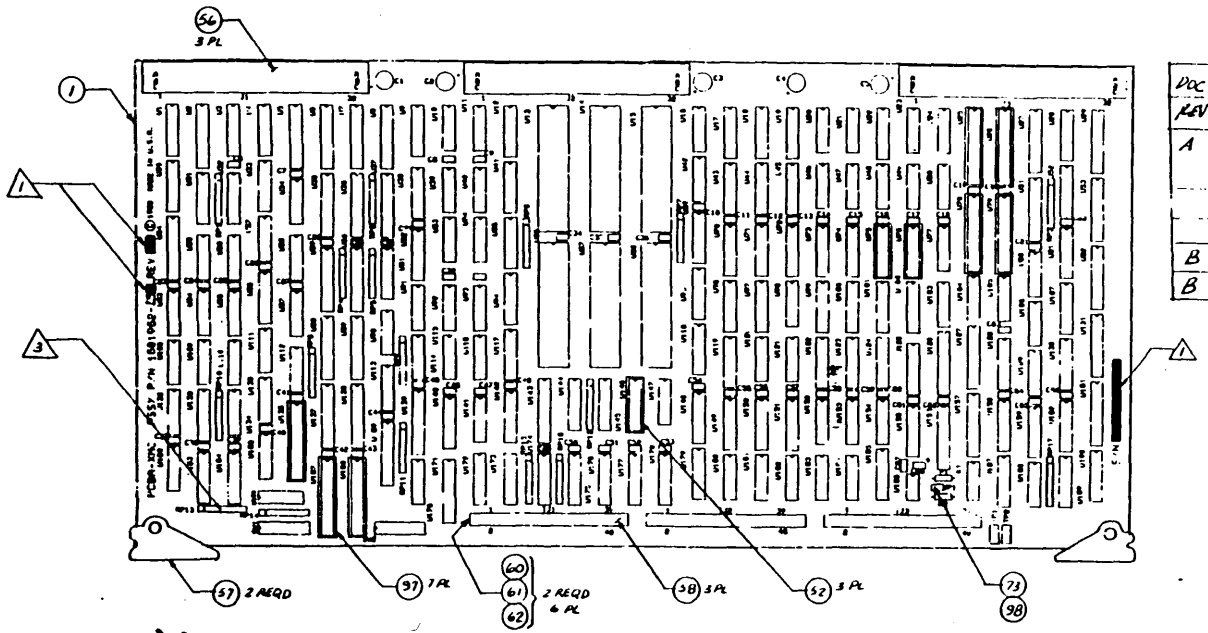
1. PERMANENTLY MARK A [illegible] LETTER AND S/N ARROW WHERE SHOWN USING WHITE EPOXY INK WITH .15 HIGH CHARACTERS
2. FOR SCHEMATIC SEE DWG NO 160 3[illegible]-101
3. INSTALL XP3 IN OPPOSITE DIRECTION WITH PIN #1 OF SILKSCREEN ON PIN SIDE OF SIP RESISTOR

APPLICABLE DASH NO. FROM TAB. Block.

ADD

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	RELEASED PER ECO 2412	10/21/87	[illegible]
	B	INC PER ECO 2604		

ADD



COMPONENT SIDE SHOWN

ADD

TABULATION

DOC REV	PART NO.	NEW REV	DESCRIPTION
A	1601962-301	A	SCHEMA INSTRUCTIONS ECO 2412
			ADD WIRE FROM U30-03
			TO: RP5-06
			REIDENTIFY AS 1601962-301 A
B	1601962-301	A	REWORK PER ECO 2412
B	1601962-901	A	REWORK PER ECO 2412 & 2604

MANUFACTURING INSTRUCTIONS
REVISION INSTRUCTIONS ECO [illegible]
ADD WIRE FROM: U30-03 TO: RP5-06
REIDENTIFY AS 1601962-301 REV A

DELETE

ECO 2604
SHT 3 OF 13

FROM -301
TO TAB

SEE SEPARATE PARTS LIST

CONFIDENTIAL DOCUMENT

PCB ASSEMBLY:	XMC
SIZE	D
DRAWING NO	1601962 (301)
REV	A
SCALE	FULL
SHEET	1 OF 1

DO NOT SCALE DRAWING

B

CLASS CODE: 28
PCBA OUTSIDE

1601962-(001) 401 OPCODE: 3 REV: A PCBA/PL,XMC
MODEL:
ECO NO: (2412) 2604
DATE OF LAST ECO: 12/19/88

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20083899	IC,CNTR,4BIT,ALS169	3	A	26	3.000	1.000	EA	P	Y	N	3.000	0	0	U107,U130 U160	00/00/00	99/99/99
20161200-001	IC,MUX,10F8,3ST,F251	3	A	27	2.000	1.000	EA	P	Y	N	2.000	0	0	U144,U145	00/00/00	99/99/99
20161300-001	IC,MUX,DUAL 10F4,3ST,F253	3	A	28	2.000	1.000	EA	P	Y	N	2.000	0	0	U124,U151	00/00/00	99/99/99
20161400-001	IC,NOR,DUAL-S,F260	3	A	29	2.000	1.000	EA	P	Y	N	2.000	0	0	U162,U188	00/00/00	99/99/99
20161500-001	IC,GEN/CHK,PRTY,9BIT,F280	3	A	30	6.000	1.000	EA	P	Y	N	6.000	0	0	U34,U58 U87,U98 U112,U121	00/00/00	99/99/99
20160000-001	IC,F/F,OCTAL-D,3ST,ALS374	3	A	31	17.000	1.000	EA	P	Y	N	17.000	0	0	U5,U6,U7 U8,U35,U36 U37,U59 U60,U88 U89,U137 U138,U139 U143,U169 U171	00/00/00	99/99/99
20159800-001	IC,MUX,DUAL 10F4,3ST,ALS253	3	A	33	2.000	1.000	EA	P	Y	N	2.000	0	0	U140,U172	00/00/00	99/99/99
20009800	IC,ENC,8INP,LS348	3	A	34	2.000	1.000	EA	P	Y	N	2.000	0	0	U74,U100	00/00/00	99/99/99
20009900	IC,RGSTR,4BIT,3ST,LS395	3	A	35	3.000	1.000	EA	P	Y	N	3.000	0	0	U12,U41 U65	00/00/00	99/99/99
20010800	IC,DRVR,QUAD,3ST,8T09	3	A	36	3.000	1.000	EA	P	Y	N	3.000	0	0	U85,U110 U152	00/00/00	99/99/99
20011200	IC,XCVR,4BIT,3ST,8T28	3	A	37	3.000	1.000	EA	P	Y	N	3.000	0	0	U9,U38 U62	00/00/00	99/99/99
20161600-001	IC,BUFF,HEX,3ST,F367	3	A	38	15.000	1.000	EA	P	Y	N	15.000	0	0	U1,U3 U4,U31 U32,U86 U101,U102 U125,U155 U173,U174 U175,U176 U178	4/07/88	99/99/99
20161700-001	IC,BUFF,INV,HEX,3ST,F368	3	A	39	15 (18).000	1.000	EA	P	Y	N	15 (18).000	0	0	U18 (U19) U44 (U45) U70,U71 (U72) U73 U95,U99 U118,U119 U133,U148 U149,U150 U177,U179	00/00/00	99/99/99

DELETE 3PL

ECO 2604 SHT 4 OF 13

ADD

20161700-001	IC, BUFF, INV, HEX, 3ST, F368	102	3.000		3.000	U19, U45, U72

NOTES: UNLESS OTHERWISE SPECIFIED

1. PERMANENTLY MARK [illegible] SN APPROX WHERE [illegible] .12 HIGH CHARACTER
2. FOR SCHEMATIC SEE DWG NO 1601962-102 FOR -302 ASSY & 1601962-902 FOR -902 ASSY
3. INSTALL XH13 IN OPPOSITE DIRECTION WITH PIN # 1 [illegible] CW PIN # 8 OF SIP RESISTOR

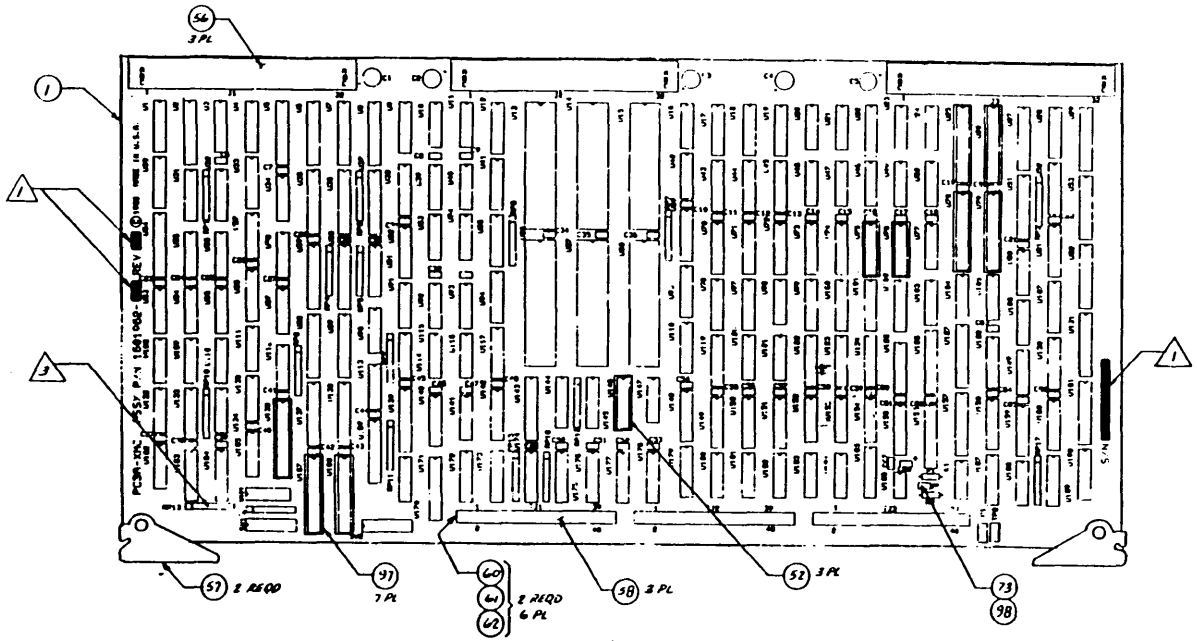
FROM TAB. BLOCK

[illegible] BLE WITH NO A REV LETTER AND [illegible] WIRE SHOWN IN MIN

ADD

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	PRODUCTION RELEASE PER ECO 2412	3-11	JW
	B	INC PER ECO 2604		

ADD A



COMPONENT SIDE SHOWN

ADD

DOC REV	TABULATION PART NO.	REV	DESCRIPTION
A	1601962-302	A	REWORK INSTRUCTION ECO 2412
—			ADD WIRE FROM: U30-03 TO: RP5-06
			REIDENTIFY AS 1601962-302 A
B	1601962-302	A	REWORK PER ECO 2412
B	1601962-902	A	REWORK PER ECO 2412 & 2604

~~A [illegible] FROM 1601962- [illegible] REV A~~
~~REWORK INSTRUCTION ECO 2412~~
~~ADD WIRE FROM: U30-03 TO: [illegible]~~
~~REIDENTIFY AS P/N 1601962-302 [illegible]~~

DELETE

ECO 2604
SHT 5 OF 13

FROM: -302
TO: TAB

SEE SEPARATE PARTS LIST

CONFIDENTIAL DOCUMENT		
	PCB ASSEMBLY XMC	
	SCALE: FULL	SIZE: D
	DO NOT SCALE DRAWING	DWG NO: 1601962 REV: B

CLASS CODE: 28
PCBA OUTSIDE

1601962-(302) 902 OPCODE: 3 REV: A PCBA/PL,XMC
MODEL:
ECO NO: (2412) 2604
DATE OF LAST ECO: 12/19/88

NEW

OP: ORDER POLICY CODE
REQ: Y-PART REQUIRED
N-PART OPTIONAL
PF: Y-PART PRINTS ON SALES ORDER
N-PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20083899	IC,CNTR,4BIT,ALS169	3	A	26	3.000	1.000	EA	P	Y	N	3.000	0	0	U107,U130 U160	00/00/00	99/99/99
20161200-001	IC,MUX,10F8,3ST,F251	3	A	27	2.000	1.000	EA	P	Y	N	2.000	0	0	U144,U145	00/00/00	99/99/99
20161300-001	IC,MUX,DUAL 10F4,3ST,F253	3	A	28	2.000	1.000	EA	P	Y	N	2.000	0	0	U124,U151	00/00/00	99/99/99
20161400-001	IC,NOR,DUAL-S,F260	3	A	29	2.000	1.000	EA	P	Y	N	2.000	0	0	U162,U188	00/00/00	99/99/99
20161500-001	IC,GEN/CHK,PRTY,9BIT,F280	3	A	30	6.000	1.000	EA	P	Y	N	6.000	0	0	U34,U58 U87,U98 U112,U121	00/00/00	99/99/99
20160000-001	IC,F/F,OCTAL-D,3ST,ALS374	3	A	31	17.000	1.000	EA	P	Y	N	17.000	0	0	U5,U6,U7 U8,U35,U36 U37,U59 U60,U88 U89,U137 U138,U139 U143,U169 U171	00/00/00	99/99/99
20159800-001	IC,MUX,DUAL 10F4,3ST,ALS253	3	A	33	2.000	1.000	EA	P	Y	N	2.000	0	0	U140,U172	00/00/00	99/99/99
20009800	IC,ENC,8INP,LS348	3	A	34	2.000	1.000	EA	P	Y	N	2.000	0	0	U74,U100	00/00/00	99/99/99
20009900	IC,RGSTR,4BIT,3ST,LS395	3	A	35	3.000	1.000	EA	P	Y	N	3.000	0	0	U12,U41 U65	00/00/00	99/99/99
20010800	IC,DRVR,QUAD,3ST,8T09	3	A	36	3.000	1.000	EA	P	Y	N	3.000	0	0	U85,U110 U152	00/00/00	99/99/99
20011200	IC,XCVR,4BIT,3ST,8T28	3	A	37	3.000	1.000	EA	P	Y	N	3.000	0	0	U9,U38 U62	00/00/00	99/99/99
20161600-001	IC,BUFF,HEX,3ST,F367	3	A	38	15.000	1.000	EA	P	Y	N	15.000	0	0	U1,U3 U4,U31 U32,U86 U101,U102 U125,U155 U173,U174 U175,U176 U178	4/07/88	99/99/99
20161700-001	IC,BUFF,INV,HEX,3ST,F368	3	A	39	(18).000	1.000	EA	P	Y	N	(18).000	0	0	U18,U19 U44,U45 U70,U71 U72,U73 U95,U99 U118,U119 U133,U148 U149,U150 U177,U179	00/00/00	99/99/99

15 15

DELETE 3PL

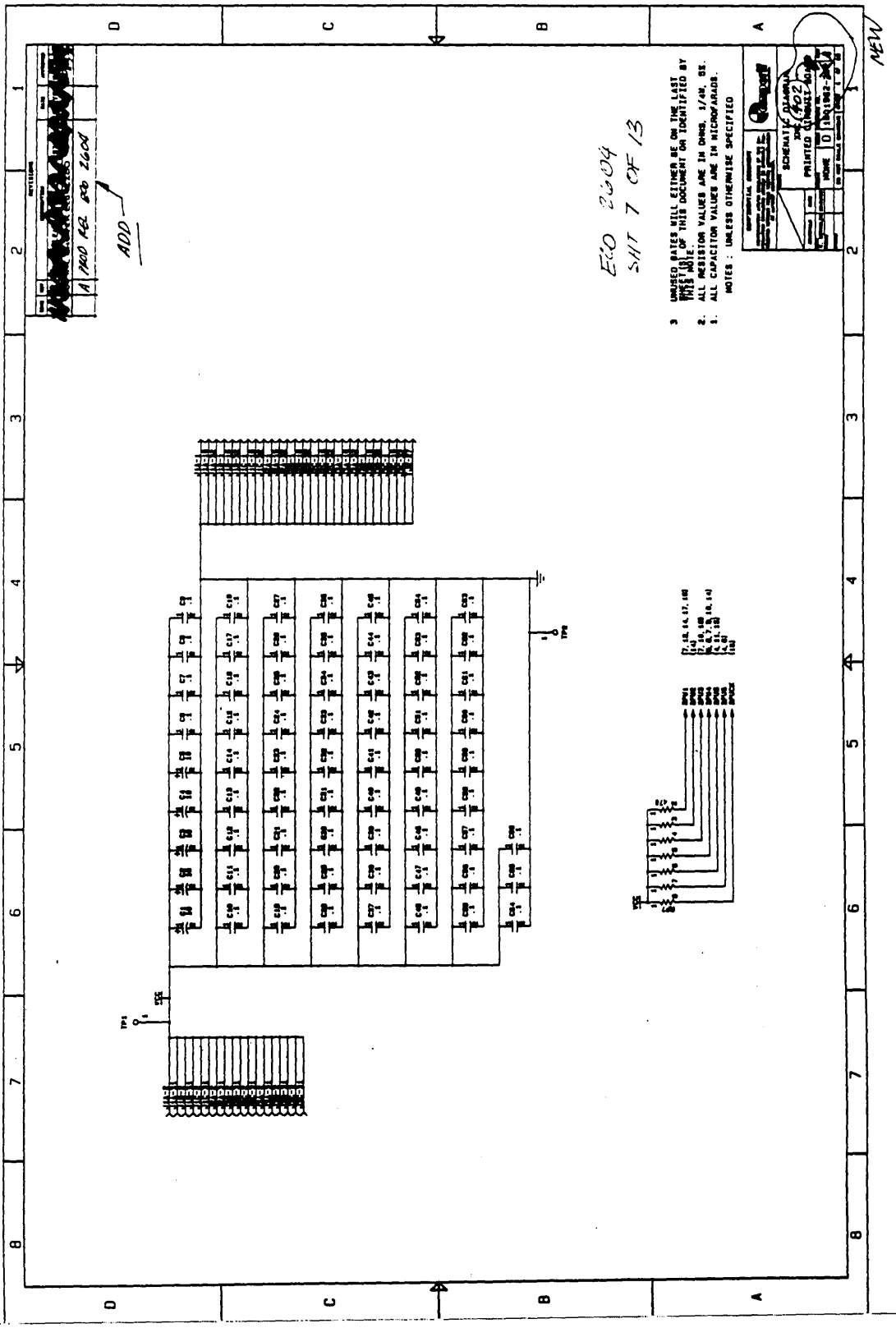
ECO 2604 SHT 6 OF 13

ADD

20122400-001	IC, BUFF, INV, HEX, 3ST, F368	99	3.000		3.000	U19, U45, U72

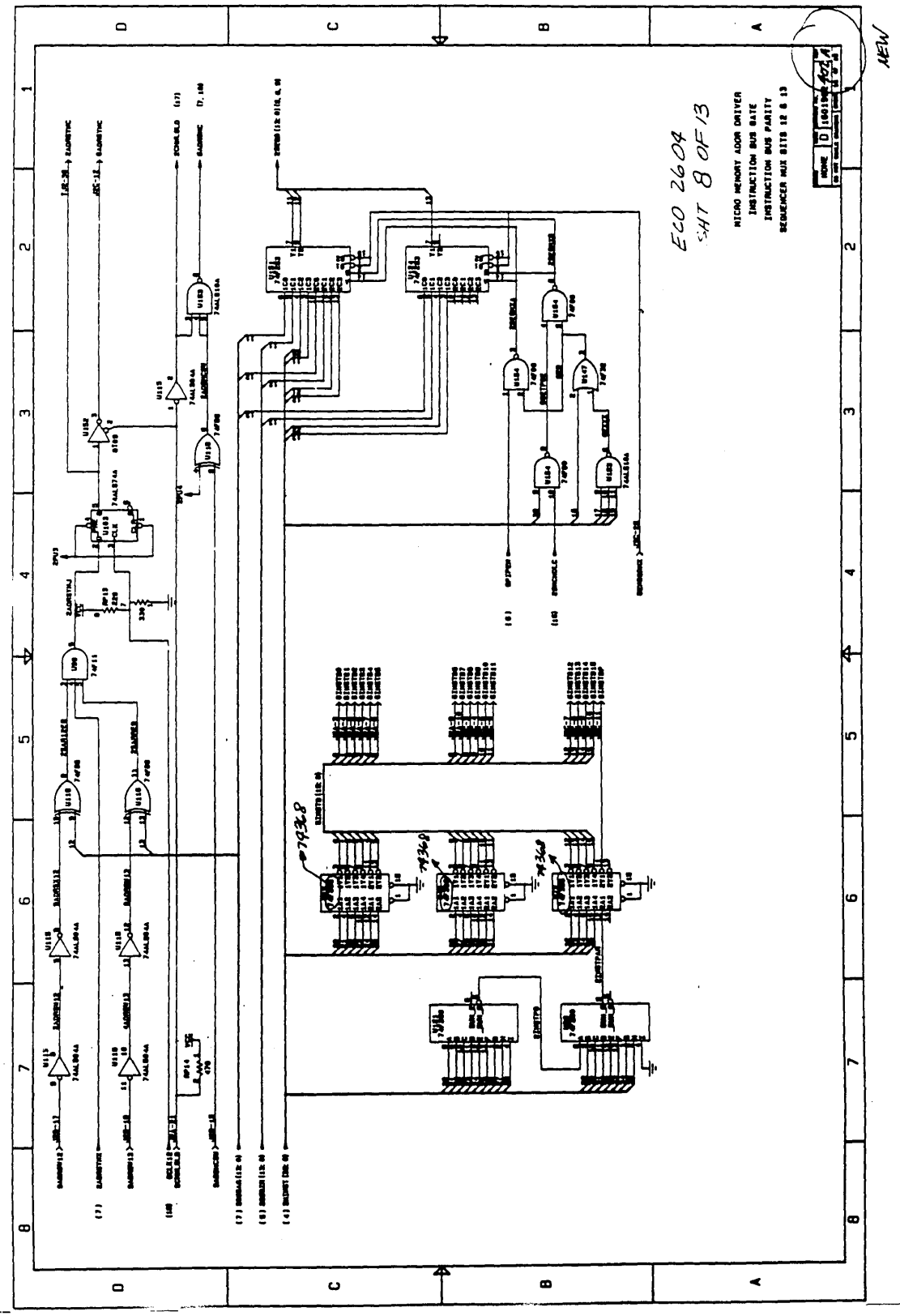
DRAWING NUMBER

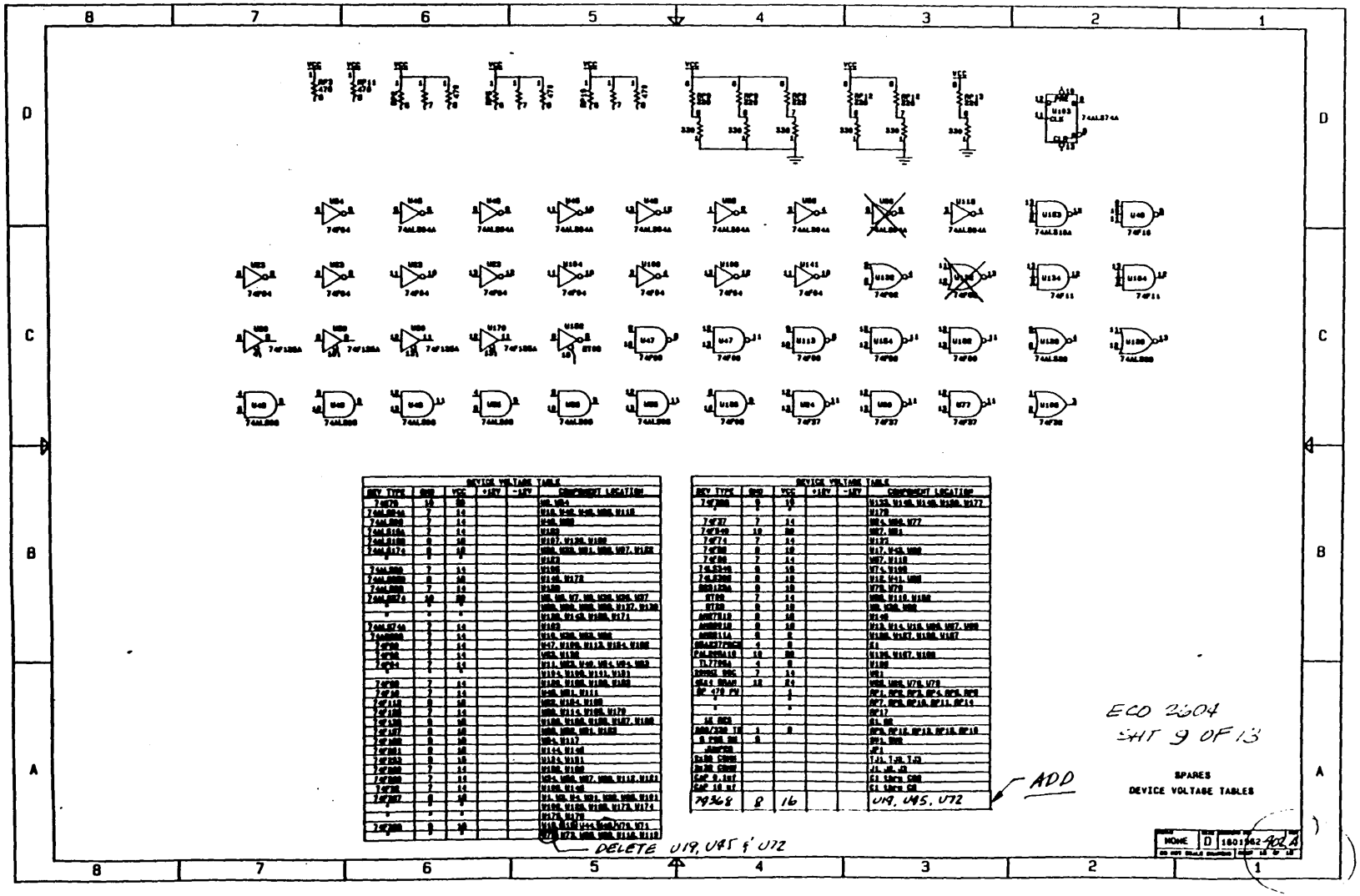
DRAWING NUMBER


ADD
ECO 23604
SHT 7 OF 13
NEW
NOTES : UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
3 UNUSED GATES WILL EITHER BE ON THE LAST PAGE/SIDE OF THIS DOCUMENT OR IDENTIFIED BY

DRAWING NUMBER

DRAWING NUMBER





DEVICE VOLTAGE TABLE

REV TYPE	GND	VCC	+12V	-12V	COMPONENT LOCATION
74F00	10	20			U45, U84
74ALS00A	7	14			U118, U140, U145, U158, U168
74ALS00	7	14			U148, U188
74ALS10A	7	14			U1103
74ALS14A	8	16			U107, U138, U188
74ALS174	8	16			U88, U103, U83, U88, U97, U138
"	"	"			U163
74ALS20	7	14			U188
74ALS32	8	16			U140, U172
74ALS38	7	14			U189
74ALS74A	10	20			U45, U46, U7, U48, U58, U88, U97
"	"	"			U88, U88, U88, U88, U137, U138
"	"	"			U138, U143, U188, U171
74ALS86A	7	14			U140
74ALS00A	7	14			U140, U88, U88, U88
74F00	7	14			U47, U188, U113, U184, U188
74F04	7	14			U83, U138
74F14	7	14			U11, U83, U40, U84, U84, U83
"	"	"			U103, U188, U131, U181
74F08	7	14			U138, U188, U188, U188
74F10	7	14			U48, U83, U113
74F20	7	14			U88, U184, U188
74F138	8	16			U88, U114, U188, U179
74F139	8	16			U138, U188, U188, U147, U188
74F157	8	16			U88, U88, U83, U183
74F158	8	16			U84, U117
74F161	8	16			U114, U140
74F253	8	16			U114, U181
74F258	8	16			U188, U188
74F260	7	14			U84, U88, U97, U88, U118, U181
74F32	7	14			U188, U140
74F367	8	16			U3, U8, U4, U83, U88, U88, U181
"	"	"			U188, U188, U188, U179, U174
"	"	"			U179, U179
74F368	8	16			U118, U118, U84, U179, U71
"	"	"			U173, U88, U88, U118, U118

DELETE U19, U45 & U72

DEVICE VOLTAGE TABLE

REV TYPE	GND	VCC	+12V	-12V	COMPONENT LOCATION
74F08	8	16			U133, U148, U148, U188, U177
"	"	"			U179
74F37	7	14			U83, U88, U77
74F240	10	20			U87, U83
74F74	7	14			U137
74F00	8	16			U47, U48, U88
74F00	7	14			U87, U118
74LS240	8	16			U74, U105
74LS240	8	16			U18, U48, U88
82S123A	8	16			U78, U78
8T98	7	14			U88, U118, U188
8T98	8	16			U8, U88, U88
AM27S18	8	16			U148
AM29818	8	16			U13, U14, U18, U88, U87, U88
AM29116	8	8			U138, U187, U188, U187
GRAC27P8C	4	8			U4
PAL20R8A	10	20			U138, U187, U188
TL7705A	4	8			U188
XXXXXX 20C	7	14			U83
XXLX XXXXX	10	24			U88, U88, U78, U78
RP 470 PU		8			RP1, RP2, RP3, RP4, RP5, RP8
"		"			RP7, RP8, RP10, RP11, RP15
"		"			RP17
NO PACK					R1, R8
2000/2200 IC	1	8			RP9, RP10, RP13, RP18, RP19
8 PIN DIP	8				RP1, RP8
JUMPER					JP1
0.1UF CERM					T11, T12, T13
10.0K CERM					J1, J8, J9
CAP 0.1UF					C1 10pfd C88
CAP 10 MF					C1 10pfd C8
74368	8	16			U19, U45, U72

ADD

ECO 2304
SHT 9 OF 13

SPARES
DEVICE VOLTAGE TABLES

SIZE	DWG NO	REV
HOME	D 1601962	202 A

NEW

1601962-202 19/19

REMARKS:

ECO 2604
SHT 10 OF 13

ADD

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
D	REDRAWN AND REVISED PER ECO # 2029	8-9-88	BRW
E	CHG PER ECO # 2118	6SEPBB	CMC
F	CHG PER ECO # 2200 RM	11-3-88	BRW
G	INC PER ECO 2412 LR	7MAR89	CMC
H	INC PER ECO 2604		

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1601962-402	A	1601962-402	A	0601764-002	A	0601764-002	A	6	—	CREATE -402/	2604
1601962-401	A	1601962-402	A	0601764-001	AX	0601764-001	AX	6	—	CREATE -401/	2604
1601962-301	A	1601962-301	A	0601764-001	AX	0601764-001	AX	6	—	CREATE -301/9200	2412
1601962-302	A	1601962-302	A	0601764-002	A	0601764-002	A	6	—	CREATE-302/9200	2412
1601962-202	E	1601962-202	B	0601764-002	A	0601764-002	A	6	—	ASSY & SCH CHG	2200
1601962-201	CX	1601962-201	BX	0601764-001	AX	0601764-001	AX	6	—	ASSY & SCH CHG	2200
1601962-202	D	1601962-202	A	0601764-002	A	0601764-002	A	6	—	ASSY CHG	2118
1601962-202	C	1601962-202	A	0601764-002	A	0601764-002	A	6	—	PROD RLS	1975
1601962-202	BX	1601962-202	AX	0601764-002	AX	0601764-002	AX	6	—	P/L CHG/PAL ASSY	2029/7-88
1601962-201	BX	1601962-201	AX	0601764-001	AX	0601764-001	AX	6	—	P/L CHG/PAL ASSY	2029/7-88
1601962-202	AX	1601962-202	AX	0601764-002	AX	0601764-002	AX	6	—	PROTO RLS	
1601962-201	AX	1601962-201	AX	0601764-001	AX	0601764-001	AX	6	—	PROTO RLS	1950/5-88
1601962-101	BX	1601962-101	CX	0601764-001	AX	0601764-001	AX	6	—	PROTOTYPE	/5-27-88
1601962-101	BX	1601962-101	BX	0601764-001	AX	0601764-001	AX	6	—	PROTOTYPE	/3-15-88
1601962-101	AX	1601962-101	AX	0601764-001	AX	0601764-001	AX	6	—	PROTOTYPE	/1-29-88

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD/ ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

NEXT ASSY

USED ON

DR BY RMarden 7-88

CHK BY

APPROVED BY

CONFIGURATION LIST
PCBA, XMC

FROM: G
TO: H

SIZE	DWG NO.	REV
A	1601962	G

SCALE

SHEET 1 OF 1

AS OF 4/14/89

CLASS CODE: 42
LARGE MECHANICAL ASSEMBLY

1602159-201 OPCODE: 3 REV: L M PCBA KIT,CONTROLLER
MODEL:
ECO NO: 2543 2604
DATE OF LAST ECO: 3/24/89

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1601962-302 402	PCBA/PL,XMC	3	A	7	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-301 401	12/16/88	99/99/99
1120010-402	PCBA,XMCIP	3	A	9	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-401	11/18/88	99/99/99
1120014-302	MDBP PCBA	3	A	10	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT. -301	2/22/89	99/99/99
1120016-803	PCBA,MPCP	3	A	11	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT P/N -802/-801	4/04/89	99/99/99
1601494-202	PCBA,XM16KP	3	B	13	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	99/99/99
1601495-951	PCBA,PROM BD-XM16KPD	3	C	14	2.000	1.000	EA	S	Y	N	2.000	0	0		12/09/88	99/99/99
1601716-502	PCBA,DIFE	3	B	16	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT P/N 1601716-501	11/18/88	99/99/99
1602015-201	PCBA,SIOA	3	D	22	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	5/05/89

ECO 2604
SHT 11 OF 13

BILL OF MATERIAL

AS OF 4/14/89

CLASS CODE: 42
LARGE MECHANICAL ASSEMBLY

1602159-001 OPCODE: 3 REV: M N 9200 DISK CONTROLLER CARD KIT
MODEL:
ECO NO: 2543 2604
DATE OF LAST ECO: 3/24/89

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1601116-005	3MB CNTLR CARD CAGE ASSY.	3	B	1	1.000	1.000	EA	M	Y	N	1.000	0	0		9/01/88	99/99/99
1602286-101	DISK I/O CARD CAGE ASSY	3	B	2	1.000	1.000	EA	M	Y	N	1.000	0	0		9/01/88	99/99/99
1602224-101	EXPANSION CARD CAGE ASSEMBLY	3	A	3	1.000	1.000	EA	M	Y	N	1.000	0	0		7/13/88	99/99/99
0601064	COVER PANEL CTLR CC	3	E	4	1.000	1.000	EA	B	Y	N	1.000	0	0	00/01-01	00/00/00	99/99/99
0601437-001	COVER,CC DISK I/O	3	B	5	2.000	1.000	EA	B	Y	N	2.000	0	0	00/02-01 00/03-01	00/00/00	99/99/99
1106012-401	PCBA,8085 CPU (CHALLENGER II)	3	G	6	1.000	1.000	EA	S	Y	N	1.000	0	0	00/00-01	00/00/00	99/99/99
1601962-502 402	PCBA/PL,XMC	3	A	7	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-501 401	12/16/88	99/99/99
1106095	AIO-A PCB ASSY	3	J	8	2.000	1.000	EA	S	Y	N	2.000	0	0	00/02-02	00/00/00	99/99/99
1120010-402	PCBA,XMCIP	3	A	9	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-401	11/18/88	99/99/99
1120014-302	MDBP PCBA	3	A	10	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT. -301	2/22/89	99/99/99
1120016-803	PCBA,MPCP	3	A	11	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT P/N -802/-801	4/04/89	99/99/99
1601138-103	PCBA,AIX	3	F	12	2.000	1.000	EA	S	Y	N	2.000	0	0	00/02-02	00/00/00	99/99/99
1601494-202	PCBA,XM16KP	3	B	13	2.000	1.000	EA	S	Y	N	2.000	0	0	00/01-02	00/00/00	99/99/99
1601495-951	PCBA,PROM BD-XM16KPD	3	C	14	2.000	1.000	EA	S	Y	N	2.000	0	0		12/09/88	99/99/99
1601715-101	PCBA ASSY,BIX-E	3	C	15	2.000	1.000	EA	S	Y	N	2.000	0	0	00/02-02	00/00/00	99/99/99
1601716-502	PCBA,DIFE	3	B	16	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT. P/N 1601716-501	11/18/88	99/99/99
0601586-001	LABEL, GROUNDING STRAPS	3	A	17	3.000	1.000	EA	B	Y	N	3.000	0	0	00/04-01 00/05-02	00/00/00	99/99/99
20119313-407	SCREW,PNHPH,10-32X1/2	3	A	18	16.000	1.000	EA	F	Y	N	16.000	0	0	FR/01-08 FR/02-04 FR/03-04	00/00/00	99/99/99
20122013-105	WSHR,FLT,#10,ZINC	3	A	19	17.000	1.000	EA	F	Y	N	17.000	0	0	FR/01-01 FR/01-08 FR/02-04 FR/03-04	00/00/00	99/99/99
20122113-005	WSHR,SPLK,#10	3	A	20	16.000	1.000	EA	F	Y	N	16.000	0	0	FR/01-08 FR/02-04 FR/03-04	00/00/00	99/99/99
1601909-101	PCBA EXXP	3	F	21	2.000	1.000	EA	S	Y	N	2.000	0	0	00/03-02	5/31/88	99/99/99

ECO 2604
SHT 12 OF 13

LI,200,2.DATABAU: AMPERIF CORPORATION DISTRIBUTION: LITO -

FRI, APR 14, 1989 BILL OF MATERIAL PAGE NO: 1

AS OF 4/14/89

CLASS CODE: 98
DOCUMENTATION ONLY !!

59200103-FRU OPCODE: 3 REV: R S 9200-10 DUAL CNTRLR FRU LIST

MODEL:

ECO NO: 2576 2604

DATE OF LAST ECO: 4/11/89

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1601495-951	PCBA,PROM BD-XM16KPD	3	C	1	.000	1.000	EA	S	Y	N	.000	0	0		12/09/88	99/99/99
1601494-202	PCBA,XM16KP	3	B	2	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1601962-302 902	PCBA/PL,XMC	3	A	3	.000	1.000	EA	S	Y	N	.000	0	0	ALT-301 901	12/16/88	99/99/99
1120010-402	PCBA,XMCIP	3	A	4	.000	1.000	EA	S	Y	N	.000	0	0	ALT-401	11/18/88	99/99/99
1120014-302	MDBP PCBA	3	A	5	.000	1.000	EA	S	Y	N	.000	0	0	ALT. -301	2/22/89	99/99/99
1120016-803	PCBA,MPCP	3	A	6	.000	1.000	EA	S	Y	N	.000	0	0	ALT P/N -802/-801	4/04/89	99/99/99
1601716-502	PCBA,DIFE	3	B	7	.000	1.000	EA	S	Y	N	.000	0	0	ALT-501	11/18/88	99/99/99
1602003-302	PCBA,OCP & P/L	3	A	8	.000	1.000	EA	S	Y	N	.000	0	0		11/11/88	99/99/99
1106012-401	PCBA,8085 CPU (CHALLENGER II)	3	G	9	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1602015-201	PCBA,SIOA	3	D	10	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	5/05/89
1602333-303	PCBA,CHNL ENABLE/DISABLE	3	B	11	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
20114801	P/S,+5,70A,400W	1	A	12	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20110901	P/S,-5V,13A,EXP,CAB	3	A	13	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
1602209-101	PCBA CTLR LOGIC B/P 3MB	3	F	14	.000	1.000	EA	B	Y	N	.000	0	0		00/00/00	99/99/99
1601840-202	PCBA BACKPLANE UNIVERSAL I/O	3	B	15	.000	1.000	EA	B	Y	N	.000	0	0	ALT. -201	4/07/89	99/99/99
1602276-203	PCBA,EXBP-DS	3	B	16	.000	1.000	EA	B	Y	N	.000	0	0		12/02/88	99/99/99
1602331-101	OPERATOR CNTRL PANEL ASSY	3	B	17	.000	1.000	EA	M	Y	N	.000	0	0		00/00/00	99/99/99
20055612	DISP,40CHAR,5X7DOT,VF	3	A	18	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
1106010-103	PCBA,LED-CHALLENGER II	3	B	19	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1106011	PCB ASSY,KEYBOARD	3	B	20	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
20105213	FAN,4.5",230VAC	3	A	21	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20105313	FAN,6",230VAC	3	A	22	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20148813-002	FAN,6.5",230VAC,1.5"THK	3	A	23	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20109411	CKT BKR,DPST,3A,230VAC	3	A	24	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20109011	CKT BKR,DPST,5A,230VAC	3	A	25	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20172811-001	CKT BRKR,DPST,1PH,30A,208V	3	A	26	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99

ECO 2604
SHT 13 OF 13

ENGINEERING CHANGE REQUEST/ORDER

ECR ☑ ECO ☑

ECR/ECO NO. 2563

PROJ. TITLE	HDW	SFTWR	IAI	CHANGE YES NO	CHANGE CLASS	FIELD	AMENDMENTS
9200	☑	☐	☐	LAL: ☐ ☑	☐ ☑ ☐ ☐ A B C D	☐ YES ☑ NO	

REQSTR/DRAWN L. RIVERA
DATE: 3-14-89

CHECKED BY
DATE: 15MAR89

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☐ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☒ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: SYSTEM WILL NOT ACCESS OR PERFORM ILO'S OR DIAGNOSTICS PROPERLY.
REA # V085206

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
1602209-101	1602209-101	D	E	PCBA/CTR LOGIC BACK-PLANE 3MB
1602209-101	——	A	B	SCHEMATIC
1602209		D	E	CONFIG LIST

REWORK INSTRUCTION:
1. ADD JUMPER WIRE FROM: DJ3A-B16 TO: DJ3A-B17 (SOLDER SIDE)
2. ADD JUMPER WIRE FROM: RJ3A-B16 TO: RJ3A-B17 (SOLDER SIDE)

INCORPORATION/DISPOSITION

INCORP. OF CHANGE DATE 5-12-89 SERIAL NO.

SPECIAL INSTRUCTION: Mfg Complies EXCEPT REV.

	USE	REWORK	SCRAP	NOTE:
IN FIELD	☐	☐	☐	
FIELD SPARES	☑	☐	☐	
FINISHED GOODS	☑	☐	☐	
FINAL ASSY	☑	☐	☐	
IN TEST	☑	☐	☐	
IN PROCESS	☑	☐	☐	
IN STOCK	☑	☐	☐	
NEXT ASSY	☑	☐	☐	
ON ORDER	☑	☐	☐	
NEXT BUY	☐	☑	☐	
OTHER	☐	☐	☐	

ENTERED

CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	gp	
SFTWR		
MARKETING	J Hankins	3-16-89
MFG. ENG.	C Carlson	3-16-89
QUALITY	S Gelfman	3-16-89
SERVICE	B. Byl	3/16/89
ENG. SERV.	D Duffy	3/17/89
DIR. OF ENG.		

REMARKS:				
	D	ASSY NOTE ADDED 2362		
	E	JUMPER ADDED 2563		

ADD

ECO 2563 SHT 2 OF 5

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
AX	PROTOTYPE	6-10-88	
A	PRODUCTION RLSE PER ECO2040	4 NOV 88	BDW
B	UPDATE ECO 2286 LR	15 DEC 88	BDW
C	UPDATE ECO 2285 LR	15 DEC 88	BDW

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1602209-101	E	1602209-10[illegible]	B	0601804-001	C	0601804-001	A	6	10	JUMPER ADDED	2563
1602209-101	D	1602209-101	A	0601804-001	C	0601804-001	A	6	10	ASSY NOTE ADDED	2362
1602209-101	C	1602209-101	A	0601804-001	C	0601804-001	A	6	10	UPDATE NOTE	2285
1602209-101	B	1602209-101	A	0601804-001	B	0601804-001	A	6	10	ASSY NOTE CHG.	2286
1602209-101	A	1602209-101	A	0601804-001	B	0601804-001	A	6	10	PRODUCTION RLSE	2040
1602209-101	AX	1602209-101	AX	0601804-001	BX	0601804-001	A	6	10	FAB NOTES CHG	
1602209-101	AX	1602209-101	AX	0601804-001	AX	0601804-001	A	6	10	PROTO	6-10-88

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

FORM 105-1-78

NEXT ASSY

USED ON

DR BY L. RIVERA 6/10/88

CHK BY

APPROVED BY

FROM: D
TO: E

CONFIGURATION LIST PCBA
CONTROLLER LOGIC BACKPLANE 3MB

SIZE A | DWG NO. 1602209 | REV E

SCALE NONE | SHEET OF 1

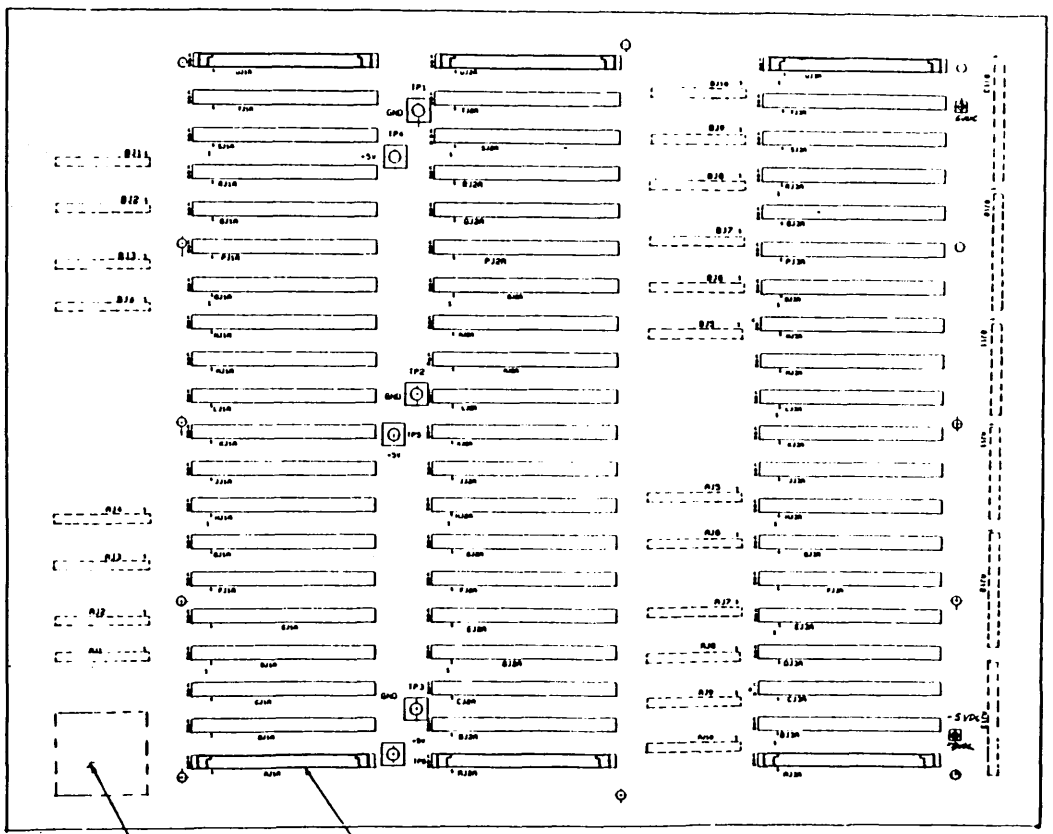
NOTES: UNLESS OTHERWISE SPECIFIED

1. PERMANENTLY MARK ASSY DASH NO., REV LETTER AND S/N ACROSS WHERE SHOWN .12 MIN HIGH CHARACTER USING WHITE EPOXY NON-CONDUCTIVE INK. REAR SIDE
2. FOR SCHEMATIC SEE DWG NO. 1605209-101
3. MODA SWEDGE SWITCH JAM LEVEL = 4 OHMS, T .036, WIDE LEAD = .75 THRU T .039 IMMEDIATELY NEW REVISIONS TO BE SHIPPED WITH ALL LOTS.
4. FOR FABRICATION DWG SEE 0601808-001
5. ALL MATERIALS AS SPECIFIED MUST BE SUPPLIED, NO SUBSTITUTIONS ARE ALLOWED.
6. APPROVED CONNECTORS ARE
   ELCO P/N 2 18955 1 0 0 1 0 0 0 0 1 1
   WINCHESTER P/N 1 0 5 6 0 - D 1 1 0
7. HEADER 40 PIN WITH EJECTOR/LATCHES
   APPROVED VENDOR & PART NO:
   AMP HEADER, 499884-9, WITH LATCHES 101310-1
   OR
   WINCHESTER 79-60 100, WITH LATCHES 101988 2

REV	DESCRIPTION	DATE	APPROVED
A	PRELIMINARY RELEASE ECO# 2080	4-15-82	
B	ADDED ECO 2260	7-1-82	
C	ASSY NOTE ADDED 2362	8-6-82	
D	ASSY NOTE ADDED 2362	8-6-82	
E	JUMPER ADDED 2563	9-13-82	

ADD →

COMPONENT SIDE SHOWN



1 ORIENT AS SHOWN CCPL

REWORK INSTRUCTION 2563

E ADD JUMPER WIRE FROM DJ3A-B16 TO UJ5A-B17 (SOLDER SIDE)
ADD JUMPER WIRE FROM RJ3A-B16 TO RJ5A-B17 (SOLDER SIDE)

ADD

ITEM	DESCRIPTION	REFERENCE DESIGNATION	PART NO	QTY
6	PCB	CONTROLLER LOGIC BACKPLANE SMB	0603804-001	1
5	STUD #8-32 x 1/2" LG	-5VDC (2 PLACES) SOLDER SIDE	PEM *KFH-832-8	2
4	HEADER 40PIN	A311, B311	AMP 102557-1	2
3	HEADER 50PIN	A312, A313, B312, B313	AMP 102557-6	4
2	HEADER 40PIN WITH EJECTOR	B31, B32, B33, B34, B35, B36, B37 B38, B39, B310, A31, A32, A33, A34, A35, A36, A37, A38, A39, A310	7	20
1	CONNECTOR 96PIN TYPE "C" PER DIN-41612 (FEMALE)	F31A, E31A, D31A, C31A, B31A, A31A, M31A, L31A, K31A, J31A, H31A, G31A, S31A, R31A, Q31A, P31A, U31A, N31A, Q32A, C32A, B32A, A32A, U31A, F31A, R32A, J32A, H32A, G32A, F32A, E32A, Q32A, P32A, D32A, N32A, M32A, L32A, B35A, A35A, U32A, T32A, S32A, R32A, H35A, G35A, F35A, E35A, D35A, C35A, D35A, R35A, M35A, J35A, K35A, J35A, U35A, T35A, S35A, R35A, U35A, P35A	6	60

5 ITEM DESCRIPTION REFERENCE DESIGNATION PART NO QTY

FROM 1 TO E

CONFIDENTIAL DOCUMENT

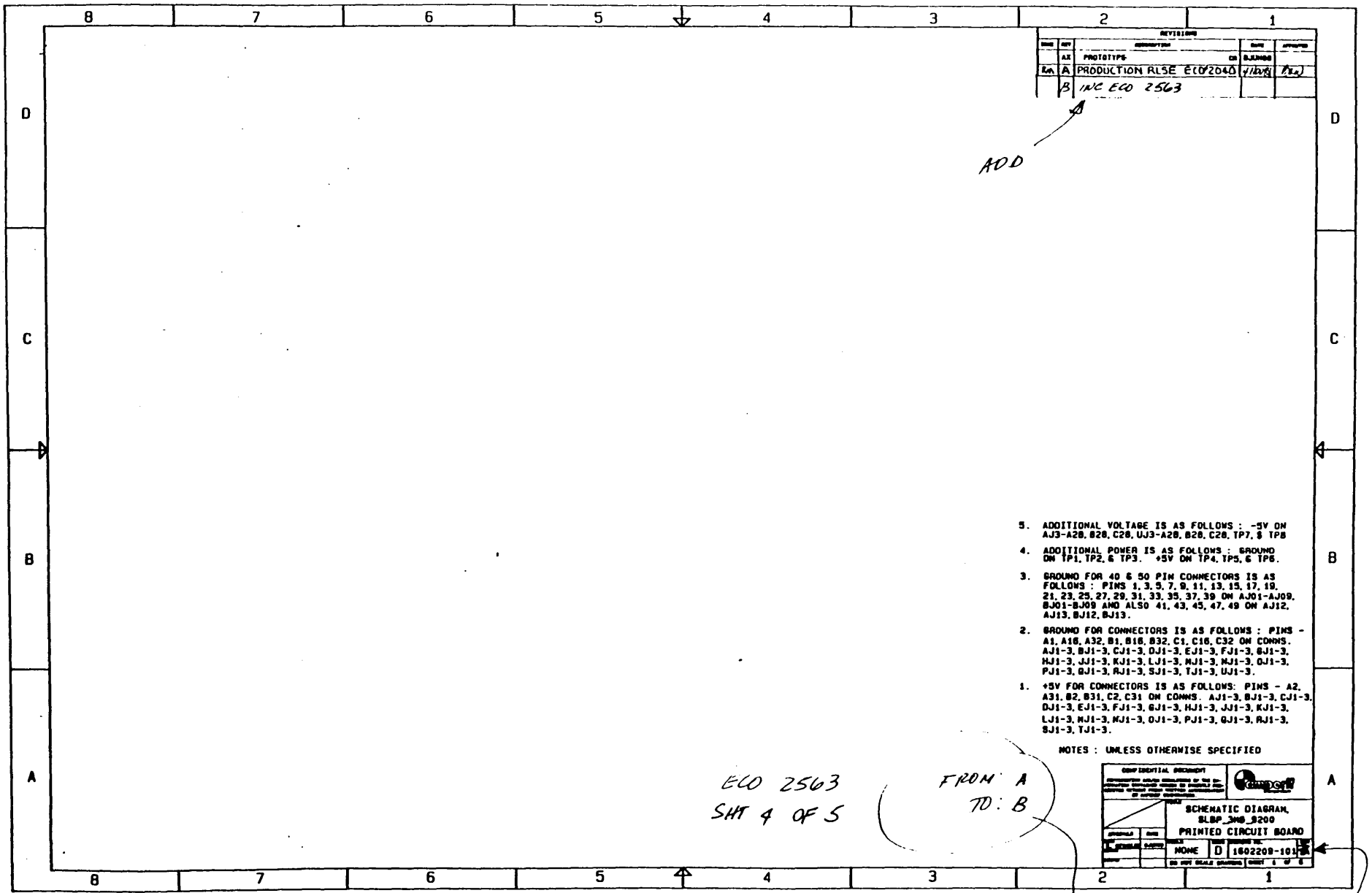
amperif

PCB ASSEMBLY: CONTROLLER LOGIC BACKPLANE SMB

SIZE D | 1605209-101 | REV E

DO NOT SCALE DRAWING | SHEET 1 OF 2

ECO 2563
SHT 3 OF 5

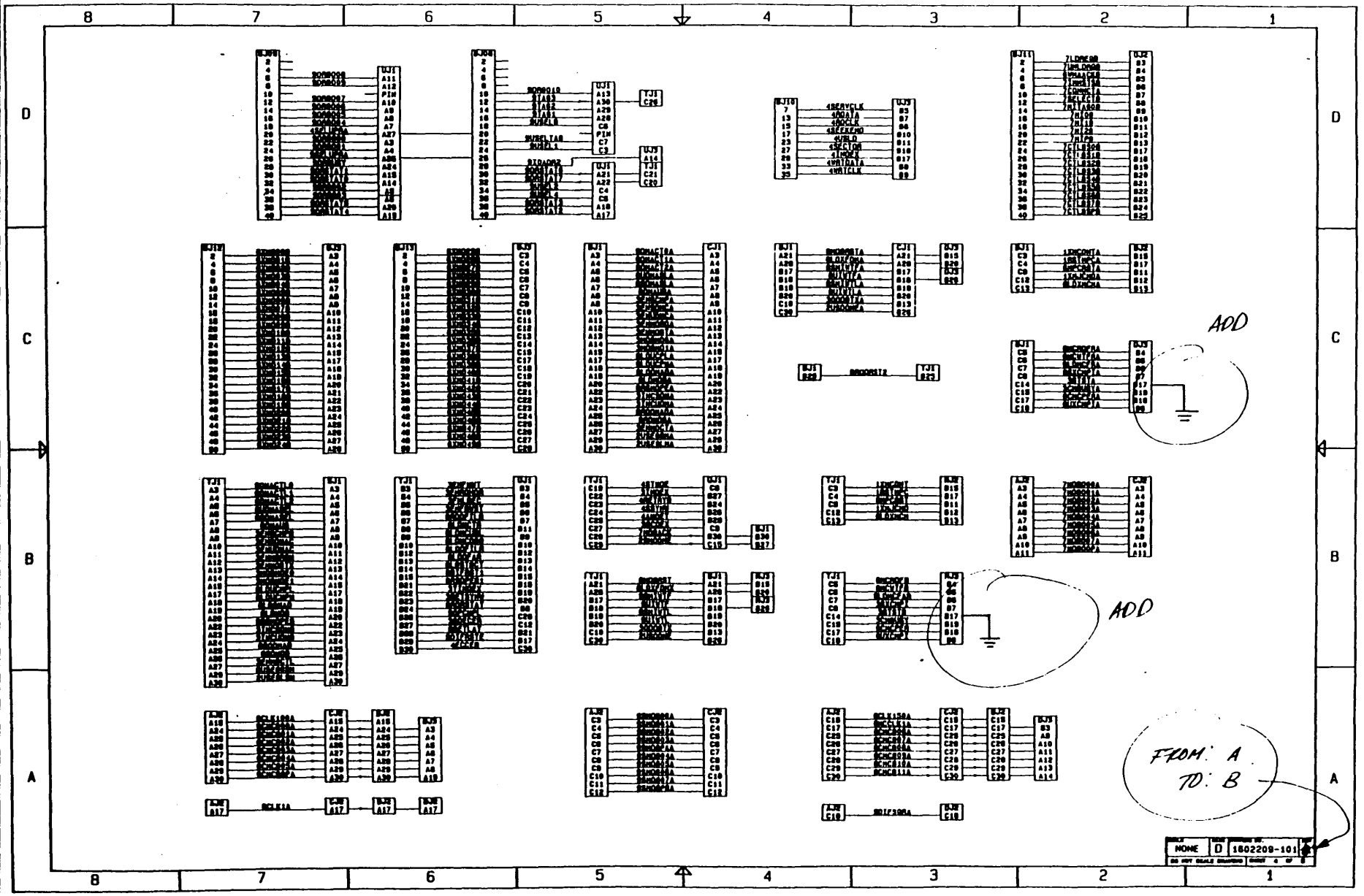

8
7
6
5
4
3
2
1
D
C
B
A
REVISIONS
AX PROTOTYPE DB 8JUN88
A PRODUCTION RLSE ECO#2040
B INC ECO 2563
ADD
5. ADDITIONAL VOLTAGE IS AS FOLLOWS : -5V ON AJ3-A28, B28, C28, UJ3-A28, B28, C28, TP7, & TP8
4. ADDITIONAL POWER IS AS FOLLOWS : GROUND ON TP1, TP2, & TP3. +5V ON TP4, TP5, & TP6.
3. GROUND FOR 40 & 50 PIN CONNECTORS IS AS FOLLOWS : PINS 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, 35, 37, 39 ON AJ01-AJ09, BJ01-BJ09 AND ALSO 41, 43, 45, 47, 49 ON AJ12, AJ13, BJ12, BJ13.
2. GROUND FOR CONNECTORS IS AS FOLLOWS : PINS - A1, A16, A32, B1, B16, B32, C1, C16, C32 ON CONNS. AJ1-3, BJ1-3, CJ1-3, DJ1-3, EJ1-3, FJ1-3, GJ1-3, HJ1-3, JJ1-3, KJ1-3, LJ1-3, MJ1-3, NJ1-3, OJ1-3, PJ1-3, QJ1-3, RJ1-3, SJ1-3, TJ1-3, UJ1-3.
1. +5V FOR CONNECTORS IS AS FOLLOWS: PINS - A2, A31, B2, B31, C2, C31 ON CONNS. AJ1-3, BJ1-3, CJ1-3, DJ1-3, EJ1-3, FJ1-3, GJ1-3, HJ1-3, JJ1-3, KJ1-3, LJ1-3, MJ1-3, NJ1-3, OJ1-3, PJ1-3, QJ1-3, RJ1-3, SJ1-3, TJ1-3.
NOTES : UNLESS OTHERWISE SPECIFIED
SCHEMATIC DIAGRAM, SLBP_3MB_9200 PRINTED CIRCUIT BOARD
NONE
D
1602209-101
ECO 2563
SHT 4 OF 5
FROM: A
TO: B

DRAWING NUMBER

1602209-101

D

5/5



ECO 2563
SHT 5 OF 5

1602209-101
D
4/5

amperif corporation

ENGINEERING CHANGE REQUEST/ORDER

ECR ☑ ECO ☒

ECR/ECO NO. 2527

PROJ. TITLE	HDW	SFTWR	LAI	CHANGE LAL: YES / NO	CHANGE CLASS A B C D	FIELD YES / NO	AMENDMENTS
ALL	☑	☐	☒	☑ / ☐	☑ ☐ ☐ ☐	☑ YES ☐ NO	

REQSTR/DRAWN: L. RIVERA AK
DATE: 2-17-89
CHECKED BY:
DATE:

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☑ PRODUCT IMPROVEMENT ☑ PRODUCTION PROBLEM ☑ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: UNTERMINATED TRI-STATE LINES CAUSED NOISE SPIKES WHICH CAUSE DATA ERRORS ON BYTE AND NIBBLE BOUNDARYS. OCCURS INTERMITTENTLY, AS A FUNCTION OF CONTROLLER & CHANNEL ACTIVITY.

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
1120014-301	1120014-301	NEW	A	PCBA, PL / MDBP
1120014-302	1120014-302	NEW	A	PCBA, PL / MDBP
1120014-302	—	NEW	A	SCHEMATIC / MDBP
1120014-	—	J	K	CONFIGURATION LIST

NOTE: REWORK ASSY 1120014-201 REV K & REIDENTIFY AS 1120014-301 REV A.
REWORK ASSY 1120014-202 REV L & REIDENTIFY AS 1120014-302 REV A.

INCORPORATION/DISPOSITION

INCORP. OF CHANGE DATE 2-22-89 SERIAL NO.

SPECIAL INSTRUCTION:

	USE	REWORK	SCRAP	NOTE:
IN FIELD	☐	☒	☐	
FIELD SPARES	☐	☒	☐	
FINISHED GOODS	☐	☒	☐	
FINAL ASSY	☐	☒	☐	
IN TEST	☐	☒	☐	
IN PROCESS	☐	☒	☐	
IN STOCK	☐	☒	☐	
NEXT ASSY	☐	☒	☐	
ON ORDER	☐	☒	☐	
NEXT BUY	☐	☒	☐	
OTHER	☐	☐	☐	

ENTERED

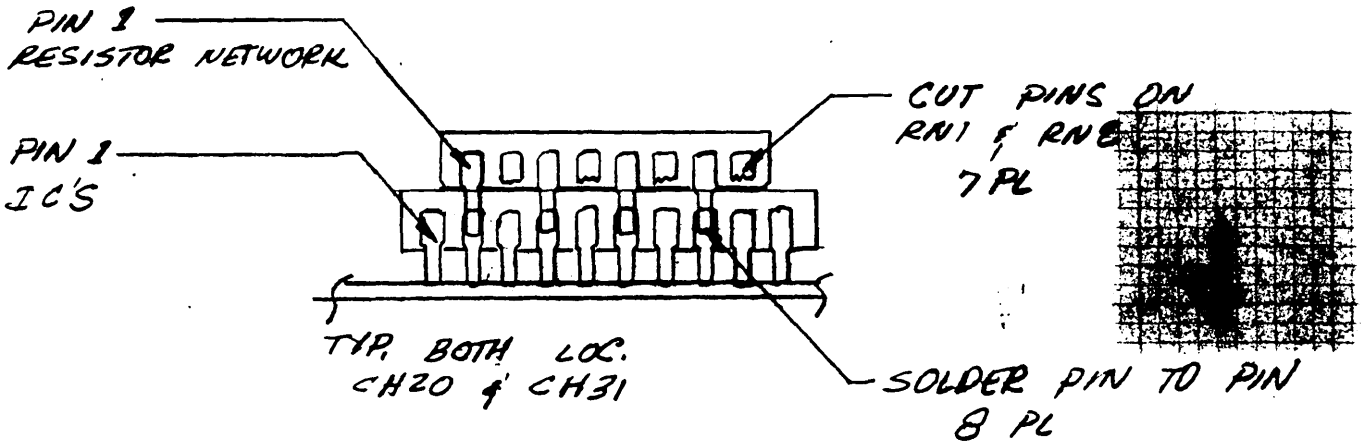
CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	[signature]	2-17-89
SFTWR		
MARKETING	[signature] Hawkins	2-21-89
MFG. ENG.	[signature] Carlson	2-21-89
QUALITY	A. Jacobs	2-21-89
SERVICE	B Bay L	2/21/89
ENG. SERV.	[signature] Smith	2/20/89
DIR. OF ENG.		

ENGINEERING CHANGE REQUEST/ORDER	ECR/ECO NO. 2527

REWORK INSTRUCTION ON ASSY P/N 1120014-201 REV K AND 1120014-202 REV L.

1. [redacted] R NETWORK DIP 16 1K OHM COM. AMPBRIF (RN1, RN2).
2. [redacted] PINS 2, 4, 6, 8, 10, 12 & 14 ON BOTH RESISTOR
3. LIFT RESISTOR LEG PIN 16 ON BOTH RESISTOR.
4. INSTALL RESISTOR RN1 @ LOC. CH20 AND RN2 @ LOC. CH31 PIGGY BACK AS SHOWN.



5. ADD JUMPER WIRE FROM: RN1-16 (LIFTED LEG)
   TO: CH20-20
6. ADD JUMPER WIRE FROM: RN2-16 (LIFTED LEG)
   TO: CH31-20
7. REWORK ASSY P/N 1120014-201 REV K & REIDENTIFY AS 1120014-301 REV A.
8. [redacted] P/N 1120014-202 REV L & REIDENTIFY [redacted] 20014-302 REV A.
9. [redacted] STRUCTIONS ON ASSY DWG. 1120014-301 1120014-302 REV A.

REMARKS:

~~H~~	~~INC ECO 2327~~	~~BR~~	
J	INC ECO 2388		
K	INC ECO 2527		

ADD

ECO 2527 SHT 3 OF 13

REVISIONS

LTR	DESCRIPTION		DATE	APPROVED
A	FIRST RELEASE		10-86	LIL
B	INC ECO # 1756/1702	EM	21 APR 87	[illegible]
C	INC ECO 1846, 1922	EM	28 JUN 88	[illegible]
E	INC ECO 1992	EM	4-NOV-88	[illegible]
F	INC ECO 2185	EM	4-NOV-88	[illegible]
G	FAB NOTE ADDED 2114	LR	11 NOV 88	[illegible]

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1120014	M	1120014	—	0120013	D	0120013	D	4	—	REWORK UPDATE	917/6-86
1120014	L	1120014	—	0120013	D	0120013	D	4	—	PROM CHG.	809/5-86
1120014	K	1120014	—	0120013	D	0120013	D	4	—	P/L CHG.	607/3-86
1120014	J	1120014	—	0120013	D	0120013	D	4	—	FAB CHG.	593/2-86
1120014	J	1120014	—	0120013	C	0120013	C	4	—	PL CHG.	543/2-86
1120014	H	1120014	—	0120013	C	0120013	C	4	—	PL CHG.	442/1-86
1120014	G	1120014	—	0120013	C	0120013	C	4	—	FAB CHG.	490/1-86
1120014	G	1120014	—	0120013	B	0120013	B	4	—	PL CHG.	432/12-85
1120014	F	1120014	—	0120013	B	0120013	B	4	—	DWG. UPDATE	353/10-85
1120014	E	1120014	—	0120013	B	0120013	B	4	—	PL CHG.	338/10-85
1120014	D	1120014	—	0120013	A	0120013	A	4	—	REWORK UPDATE	DF001/9-85
1120014	C	1120014	—	0120013	A	0120013	A	4	—	PL CHG.	284/9-85
1120014	B	1120014	—	0120013	A	0120013	A	4	—	PL CHG.	247/8-85
1120014	A	1120014	—	0120013	A	0120013	A	4	—	PL CHG.	226/8-85

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

FORM 105-1-78

NEXT ASSY

USED ON

DR BY	L. RIVERA	10/86
CHK BY		

APPROVED BY

CONFIGURATION LIST PWBA:

MDBP MULTIWIRE BOARD

K

SIZE		DWG NO.	REV
A		1120014	J
SCALE NONE			SHEET 1 OF 4

REMARKS:

ECO 2527
SHT 4 OF 13

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

ADD

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1120014-302	A	1120014-302	A	0120013-002	D	0120013-002	A	4	—	RESISTOR ADDED	2527
1120014-301	A	1120014-302	A	0120013	F	0120013-002	D	4	—	RESISTOR ADDED	2527
1120014-202	L	1120014-202	G	0120013-002	D	0120013-002	A	4	—	ADD JUMPERS	2388
1120014-201	K	1120014-201	H	0120013-	F	0120013	D	4	—	ADD JUMPERS	2388
1120014-201	J	1120014-201	G	0120013-	F	0120013	D	4	—	SCH & ASSY CHG.	2337
1120014-202	K	1120014-202	F	0120013-002	D	0120013-002	A	4	—	FAB NOTE ADDED	2114
1120014-202	K	1120014-202	F	0120013-002	C	0120013-002	A	4	—	REMOVE 2OPSKTS	2185
1120014-202	J	1120014-202	F	0120013-002	C	0120013-002	A	4	—	ASSY & SCH CHG	1992

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD/ ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

NEXT ASSY

USED ON

DR BY

CHK BY

APPROVED BY

CONFIGURATION LIST PWBA
MDBP MULTIWIRE BOARD

K

SIZE		DWG NO.	REV
A		1120014	J

SCALE NONE

SHEET 4 OF 4

AS OF 2/17/89

CLASS CODE: 28
PCBA OUTSIDE

1120014-202 302 OPCODE: 3 REV: L A PCBA.MDBP
MODEL:
ECO NO: 2388 2527
DATE OF LAST ECO: 12/12/88

UP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	UP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1601407-002	PAL ASSY,MDBP BBF01	3	C	1	1.000	1.000	EA	B	Y	N	1.000	0	0	BF01	5/08/86	99/99/99
20002500	IC,BUFR,QUAD,3ST,74125	3	A	2	1.000	1.000	EA	P	Y	N	1.000	0	0	DD01	00/00/00	99/99/99
20004800	IC,NAND,QUAD-2,S00	3	A	3	1.000	1.000	EA	P	Y	N	1.000	0	0	BB12	00/00/00	99/99/99
20005000	IC,INV,HEX,S04	3	A	4	1.000	1.000	EA	P	Y	N	1.000	0	0	AE09	00/00/00	99/99/99
20005600	IC,OR,QUAD-2,S32	3	A	5	1.000	1.000	EA	P	Y	N	1.000	0	0	BF45	00/00/00	99/99/99
20006000	IC,COMP,4BIT,S85	3	A	6	1.000	1.000	EA	P	Y	N	1.000	0	0	AC28	00/00/00	99/99/99
20006100	IC,XOR,QUAD-2,S86	3	A	7	1.000	1.000	EA	P	Y	N	1.000	0	0	DJ01	00/00/00	99/99/99
20006600	IC,DEMUX,2TO4,S139	3	A	8	1.000	1.000	EA	P	Y	N	1.000	0	0	BB20	00/00/00	99/99/99
20007000	IC,MUX,QUAD,1OF2,S157	3	A	9	1.000	1.000	EA	P	Y	N	1.000	0	0	BB01	00/00/00	99/99/99
20008500	IC,MUX,QUAD,1OF2,3ST,S257	3	A	10	1.000	1.000	EA	P	Y	N	1.000	0	0	BF27	00/00/00	99/99/99
20008800	IC,GEN,PRTY,9BIT,S280	3	A	11	2.000	1.000	EA	P	Y	N	2.000	0	0	CM12,DB12	00/00/00	99/99/99
20010800	IC,DRVR,QUAD,3ST,8T09	3	A	12	2.000	1.000	EA	P	Y	N	2.000	0	0	AE01,DF01	00/00/00	99/99/99
20014800	IC,DIP,16P,330/390,TERM	3	A	13	3.000	1.000	EA	P	Y	N	3.000	0	0	AC01,BF55 DL55	00/00/00	99/99/99
20015300	RES,DIP.14P.220/330,TERM	3	A	14	1.000	1.000	EA	P	Y	N	1.000	0	0	DL01	00/00/00	99/99/99
20015400	RES,SIP,8P,220/330,DUAL TERM.	3	A	15	7.000	1.000	EA	P	Y	N	7.000	0	0	BJ27,BJ36 BJ44,BK14 BK23,CC23 CD23	00/00/00	99/99/99
20018402-003	CAP,CE,RAD,.1UF,50V,20%	3	A	16	31.000	1.000	EA	P	Y	N	31.000	0	0	C11-C42	10/23/87	99/99/99
20018902	CAP.TANT.RAD.10UF,20%.16V	3	A	17	10.000	1.000	EA	P	Y	N	10.000	0	0	C1-C10	00/00/00	99/99/99
20019803	SKT.DIP,24P.PCMT	3	A	18	2.000	1.000	EA	P	Y	N	2.000	0	0	XBF01 XBF14	00/00/00	99/99/99
20050500	IC,SRAM,16KX1.55NS	3	A	19	40.000	1.000	EA	P	Y	N	40.000	0	0	AA42,AA53 AC42,AC53 AE42,AE53 AK31,AK42 AH53,DJ53 AH42,AK53 AM31,AM42 AM53,BB31 BB42,BB53 BD31,BD42 BD53,CH42 CH53,CK42 CK53,CM42 CM53,DB31 DB42,DB53 DD31,DD42 DD53,DF31 DF42,DF53	00/00/00	99/99/99

ECO 2527
SHT 5 OF 13

ADD

20015000	RES, DIP, 16P, 1K OHM, COM	2.000	2.000	RN1, RN2

AS OF 2/17/89

CLASS CODE: 28
PCBA OUTSIDE

1120014(201) 301 UPCODE: 0 REV: (K) A PCBA MDBP
MODEL:
ECO NO: (2388) 2527
DATE OF LAST ECO: 12/12/88

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	UP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20005100	IC,AND,QUAD-2,S08	3	A	0	1.000	1.000	EA	P	Y	N	1.000	0	0	ED12	7/03/87	99/99/99
1601407-002	PAL ASSY,MDBP @BF01	3	C	1	1.000	1.000	EA	B	Y	N	1.000	0	0	BF01	5/08/86	99/99/99
20002500	IC,BUFR,QUAD,3ST,74125	3	A	2	1.000	1.000	EA	P	Y	N	1.000	0	0	DD01	00/00/00	99/99/99
20004800	IC,NAND,QUAD-2,S00	3	A	3	1.000	1.000	EA	P	Y	N	1.000	0	0	BB12	00/00/00	99/99/99
20005000	IC,INV,HEX,S04	3	A	4	1.000	1.000	EA	P	Y	N	1.000	0	0	AE09	00/00/00	99/99/99
20005600	IC,OR,QUAD-2,S32	3	A	5	1.000	1.000	EA	P	Y	N	1.000	0	0	BF45	00/00/00	99/99/99
20006000	IC,COMP,4BIT,S85	3	A	6	1.000	1.000	EA	P	Y	N	1.000	0	0	AC28	00/00/00	99/99/99
20006100	IC,XOR,QUAD-2,S86	3	A	7	1.000	1.000	EA	P	Y	N	1.000	0	0	DJ01	00/00/00	99/99/99
20006600	IC,DEMUX,2TO4,S139	3	A	8	1.000	1.000	EA	P	Y	N	1.000	0	0	BB20	00/00/00	99/99/99
20007000	IC,MUX,QUAD,1OF2,S157	3	A	9	1.000	1.000	EA	P	Y	N	1.000	0	0	BB01	00/00/00	99/99/99
20008500	IC,MUX,QUAD,1OF2,3ST,S257	3	A	10	1.000	1.000	EA	P	Y	N	1.000	0	0	BF27	00/00/00	99/99/99
20008800	IC,GEN,PRTY,9BIT,S280	3	A	11	2.000	1.000	EA	P	Y	N	2.000	0	0	CM12,DB12	00/00/00	99/99/99
20010800	IC,DRVR,QUAD,3ST,8TO9	3	A	12	2.000	1.000	EA	P	Y	N	2.000	0	0	AE01,DF01	00/00/00	99/99/99
20014800	IC,DIP,16P,330/390,TERM	3	A	13	3.000	1.000	EA	P	Y	N	3.000	0	0	AC01,BF55 DL55	00/00/00	99/99/99
20015300	RES,DIP,14P,220/330,TERM	3	A	14	1.000	1.000	EA	P	Y	N	1.000	0	0	DL01	00/00/00	99/99/99
20015400	RES,SIP,8P,220/330,DUAL TERM.	3	A	15	7.000	1.000	EA	P	Y	N	7.000	0	0	BJ27,BJ36 BJ44,BK14 BK23,CC23 CD23	00/00/00	99/99/99
20018402	CAP,CER,RAD,.1UF,50V,20%..2 LS	3	A	16	31.000	1.000	EA	P	Y	N	31.000	0	0	C11-C42	00/00/00	99/99/99
20018902	CAP,TANT,RAD,10UF,20%,16V	3	A	17	10.000	1.000	EA	P	Y	N	10.000	0	0	C1-C10	00/00/00	99/99/99
20019803	SKT,DIP,24P,PCMT	3	A	18	2.000	1.000	EA	P	Y	N	2.000	0	0	XBF01 XBF14	00/00/00	99/99/99
20050500	IC,SRAM,16KX1,55NS	3	A	19	40.000	1.000	EA	P	Y	N	40.000	0	0	AA42,AA53 AC42,AC53 AE42,AE53 AK31,AK42 AH53,DJ53 AH42,AK53 AM31,AM42 AM53,BB31 BB42,BB53 BD31,BD42 BD53,CH42 CH53,CK42 CK53,CM42 CM53,DB31 DB42,DB53 DD31,DD42 DD53,DF31	00/00/00	99/99/99

ECO 2527
SHT 6 OF 13

ADD

20015000	RES, DIP, 16P, 1K OHM, COM	2.000	2.000	RN1, RN2

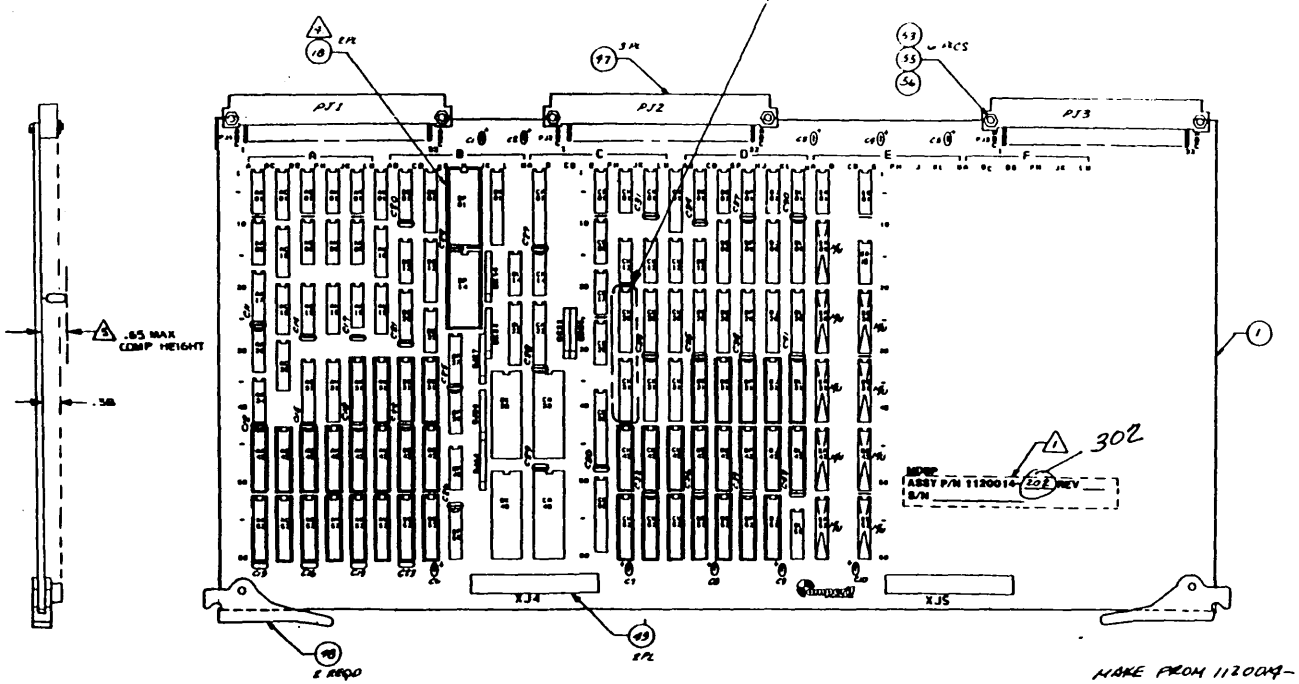
NOTES: UNLESS OTHERWISE SP

1. PERMANENTLY MARK A[illegible] ON 1120014-202 AND CURRENT REV LETTER AND IN APPROX WHERE SHOWN. FOR SCHEMATIC SEE DWG NO 1120014-302 — 302
2. DELETED
3. INSTALL 64 PIN SOLDER SOCKET (2 PL).
4. ALL COMPONENTS ARE MOUNTED AS CLOSE AS POSSIBLE TO THE PWB. MAX COMPONENT HEIGHT IS .38 EXCEPT DECOUPLING CAPACITORS MAY BE .65. IF CAPACITOR INTERFERES, BEND CAPACITOR OVER.

ADD — A | PROD REL 2527

FEB 1? 1989

SEE REWORK INSTRUCTION # 2527



COMPONENT SIDE

A	REWORK INSTRUCTION (ECO#1468)
	1. REMOVE AND REPLACE COMPONENT @ LOC AH01. SEE SEPARATE P/L FOR REPLACEMENT (IC7408)

B	REWORK INSTRUCTION (ECO#1513)

JUMPER TABLE

NO.	FROM	TO	WIRE GA	BOARD SIDE
1	DF1-02 (IC PAD)	DB1-12 (IC PAD)	30	COMPONENT
2	DB1-12 (IC PAD)	DB1-08 (IC PAD)	"	"
3	AK01-05 (IC PAD)	CE01-01 (IC PAD)	"	"

F	REWORK INSTRUCTION (ECO#1724)
	1. LIFT IC LEG @ LOC AA09-04

JUMPER TABLE

NO	FROM	TO	GA	BOARD SIDE
4	AA09-04 (IC PAD)	AA17-11 (IC PAD)	30	COMPONENT
5	AA09-04 (IC LEG)	AA17-10 (IC PAD)	30	COMPONENT
6	CE01-05 (IC LEG)	DB01-07 (IC PAD)	30	COMPONENT

G	REWORK INSTRUCTION (ECO 1902)
7	LIFT I.C. LEG @ DL01-12

H	REWORK INSTRUCTIONS ECO#1922			
JUMPER TABLE				
NO	FROM	TO	GA	BOARD SIDE
8	BD12-18	BK14-06	30	COMPONENT

J	REWORK INSTRUCTIONS (ECO# 1992)
	1. CUT & LIFT IC LEGS @ LOCATIONS AC01-07 AND AC01-09

ECO 2527
SHT 7 OF 13

MADE FROM 1120014-202 REV L

ADD REWORK INSTRUCTION ECO 2527

FROM: -202
TO: -302
FROM: REV
TO: REV A

SEE SEPARATE PARTS LIST

CONFIDENTIAL DOCUMENT

amperif

PCB ASSEMBLY:
MOBD MULTIWIRE BOARD

SCALE: FULL | SIZE: D | 1120014-202 | REV: H

BEING CHANGED BY 2388

FEB 17 1989

NOTES: UNLESS OTHERWISE SPECIFIED

MAKE FROM 1120014 REV T

A REWORK INSTRUCTIONS (ECO 1273)

1. REMOVE & REPLACE COMPONENT @ BF01 & BF14 - SEE SPL FOR NEW P/N.
2. LIFT IC LEG @ CK12-03 & DB01-02
3. LIFT IC LEG @ BK01-13 & CA01-13

JUMPER TABLE

NO.	FROM:	TO:	WIRE GA.	BOARD SIDE
1	EA01-02	EA01-05	30 (2)	COMPONENT
2	CK12-03 (IC LEG)	EA01-04		
3	CK12-03 (IC PAD)	EA01-06		
4	DB01-02 (IC PAD)	EA01-09		
5	BF27-13	EA01-10		
6	DB01-02 (IC LEG)	EA01-8		
7	BK01-13 (IC LEG)	CA01-13 (IC LEG)		
8	CA01-13 (IC LEG)	ED01-8		
9	CK01-04	DB01-10		
10	DB01-08	DB01-12		
11	BF27-12	DB01-11		
12	DB01-09	ED01-04		
13	ED01-06	ED01-09	30 (2)	COMPONENT

ETCH CUT TABLE

NO	FROM:	TO	REMARKS	BOARD SIDE
14	CE25-13	DB01-13		COMPONENT
15	BJ36-05	DB01-14		
16	ED01-04	ED01-05		
17	ED01-09	ED01-10		COMPONENT

H REWORK INSTRUCTIONS (ECO # 1992)

1. CUT & LIFT IC LEG @ LOCATIONS AC01-07, AC01-09

J REWORK INSTRUCTION (ECO # 2337)

1. ADD WIRE FROM: BD12-18 TO: BK9-6

REWORK INSTRUCTIONS (ECO 1273) (FOR BOARDS @ P4 LEVEL)

LIFT IC LEG @ WC BK01-14 & CA01-14

ETCH CUT TABLE

NO.	FROM:	TO:	REMARKS	BOARD SIDE
18	ED01-04	ED01-05		COMPONENT
19	DB01-13	CE25-13		
20	ED01-10	ED01-09		
21	BJ36-05	DB01-14		COMPONENT

JUMPER TABLE

NO.	FROM:	TO:	WIRE GA.	BOARD SIDE
22	DB01-01	DB01-13	30 (2)	COMPONENT
23	BL14-05	BK01-14 (IC LEG)		
24	BK01-14 (IC LEG)	CA01-14 (IC LEG)		
25	CA01-14 (IC LEG)	CK01-11		
26	CK01-08	ED01-10		
27	CA14-01	ED01-12		
28	CA14-02	ED01-13		
29	ED01-11	CK01-12		
30	CK01-04	CK01-10		
31	CD28	EA01-12		
32	BF36-05	EA01-13		
33	EA01-11	DF01-01		
34	DF01-03	CK01-13		
35	DF01-02	DF01-07		
36	DB01-14	DB01-15		
37	DB01-06	ED01-05	30 (2)	COMPONENT

B REWORK INSTRUCTION PER ECO # 1586

1. LIFT IC LEG ON CE 01-6

JUMPER TABLE

NO	FROM :	TO :	WIRE GA	BOARD SIDE
38	CE 01-2	CE01-6 PAD	30 (2)	COMPONENT

REVISIONS				
A	PROD RDL	ECO 1273		
B	PER	ECO # 1441		
C	PER	ECO # 1445		
D	PER	ECO # 1466		
E	PER	ECO # 1526		
G	PER	ECO # 1992		
J	PER	ECO # 2337		
A	PROD RDL	2527		

ADD

ADD REWORK INSTRUCTION # 2527

MAKE FROM 1120014-201 REV K

FROM: -201
TO: -301
FROM: REV J
TO: REV A

SEE SEPARATE PARTS LIST

ADD NOTE # 3

3. FOR SCHEMATIC SEE DWG NO. 1120014-302.

(2) JUMPERS: #30 AWG, "WIRE WRAP TYPE WIRE", SOLID CONDUCTOR INSULATED, COLOR OPTIONAL PER MFG PRACTICE. 301

(1) REIDENTIFY ASSY AS 1120014-201 CURRENT REV. LETTER AND SERIAL NO. AS SHOWN.

NOTES: UNLESS OTHERWISE SPECIFIED

ECO 2527
SHT 8 OF 13

CONFIDENTIAL DOCUMENT
REPRODUCTION AND/OR DISCLOSURE OF THE INFORMATION CONTAINED HEREIN IS STRICTLY PROHIBITED WITHOUT PRIOR WRITTEN AUTHORIZATION BY AMPERIF CORP

amperif

PCB ASSEMBLY
MDBP MULTIWIRE BOARD

APPROVALS	DATE
DRAWN JWEST	3-4-87
CHECKED B	3-12-87
APPROVED	

SCALE NONE | SIZE C | DRAWING NO 1120014-201 | REV J | DO NOT SCALE DRAWING | SHEET 1

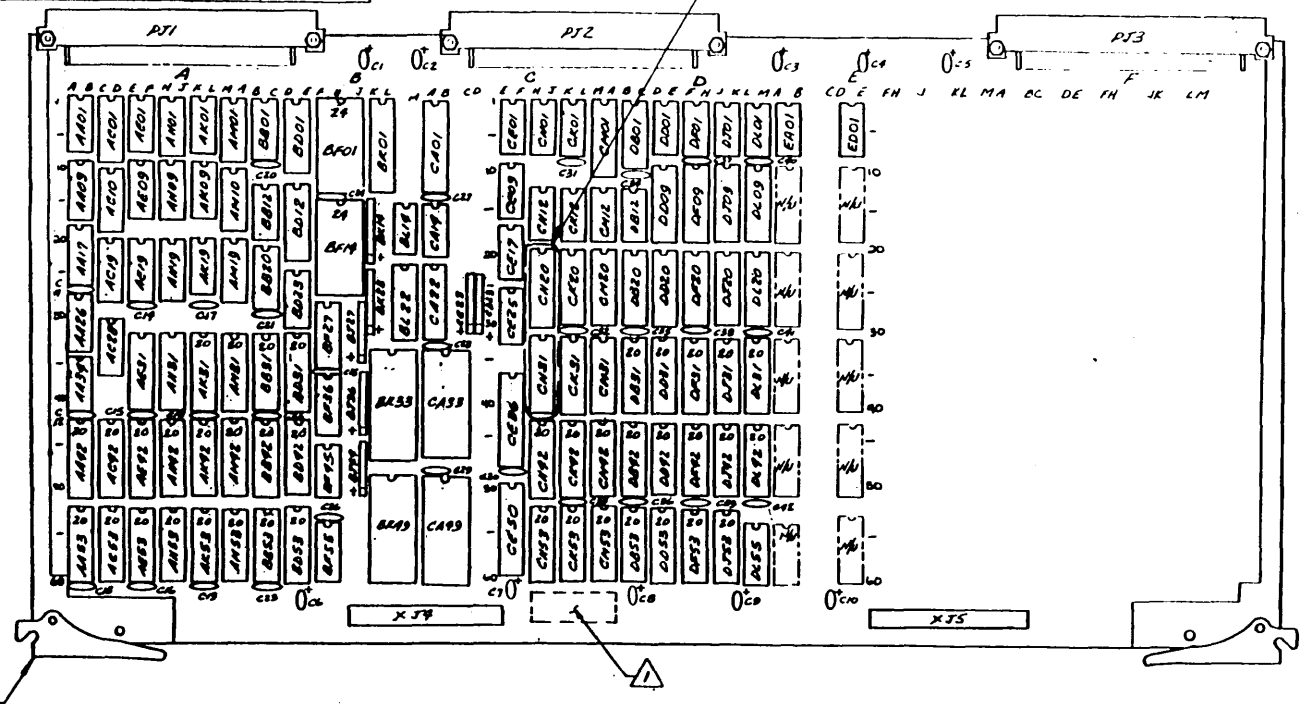
DRAW JUMPER

PART NUMBER

H	REWORK INSTRUCTIONS ECO#1922				
	JUMPER TABLE				
NO.	DEL/ADD	FROM	TO	WIRE GA	BOARD SIDE
53	ADD	BD12-18	BK14-6	20 △2	COMPONENT

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		

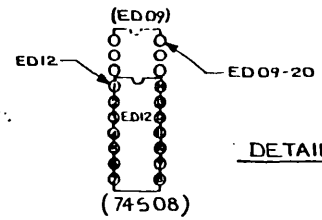
SEE REWORK INSTRUCTION # 2527



COMPONENT SIDE

C	REWORK INSTRUCTION (ECO#1441)				
	JUMPER TABLE				
NO.	DEL/ADD	FROM	TO	WIRE GA	BOARD SIDE
39	DELETE	BL14-Ø4	ED Ø1-Ø2		
40	DELETE	BL14-Ø9	ED Ø1-Ø1		
41	ADD	BD12-13	ED Ø1-Ø1	30 △2	COMPONENT
42	ADD	BD12-14	ED Ø1-Ø2	"	COMPONENT
E	REWORK INSTRUCTION ECO#1466				
49	REMOVE & REPLACE COMPONENT @ LOC. AH Ø1 SEE SEPARATE P/L FOR REPLACEMENT COMPONENT P/N 20000500 IC 7408				
F	REWORK INSTRUCTIONS ECO#1756				
	LIFT I.C. LEG @ LOC. AA Ø9-Ø4				
50	ADD	AA Ø9-Ø4 I.C. PAD	AA17-11 I.C. PAD	30 △2	COMPONENT
51	ADD	AA Ø9-Ø4 I.C. LEG	AA17-Ø2 I.C. PAD	30 △2	COMPONENT

D	REWORK INSTRUCTION (ECO#1445)			
	1. INSTALL IC (74S Ø8) ED12 @ LOC ED Ø9 (SEE DETAIL 'A')			
	2. LIFT IC LEG @ LOC CE Ø1-Ø4, CE Ø1-Ø5, AA Ø9-Ø2 AND CE Ø1-Ø6.			
	JUMPER TABLE			
NO.	ADD FROM	TO	WIRE GA	BOARD SIDE
43	CE Ø1-Ø4 (IC LEG)	DB Ø1-11	30 △2	COMPONENT
44	CE Ø1-Ø5 (IC LEG)	DB Ø1-Ø7	"	"
45	CE Ø1-Ø6 (IC LEG)	ED12-Ø1	"	"
46	CH31-Ø1	ED12-Ø2	"	"
47	AA Ø9-Ø2 (IC LEG)	ED12-Ø3	"	"
48	ED12-14	ED Ø9-2Ø	"	"
G	REWORK INSTRUCTION ECO# 1902			
52	LIFT I.C. LEG @ DL Ø1-12			



DETAIL 'A'

FROM: -201
TO: 301
FROM: REV J
TO: REV A

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PCB ASSEMBLY:
MDDP MULTIWIRE BOARD

APPROVALS	DATE
DRAWN PRIEST	5-4-87
CHECKED	

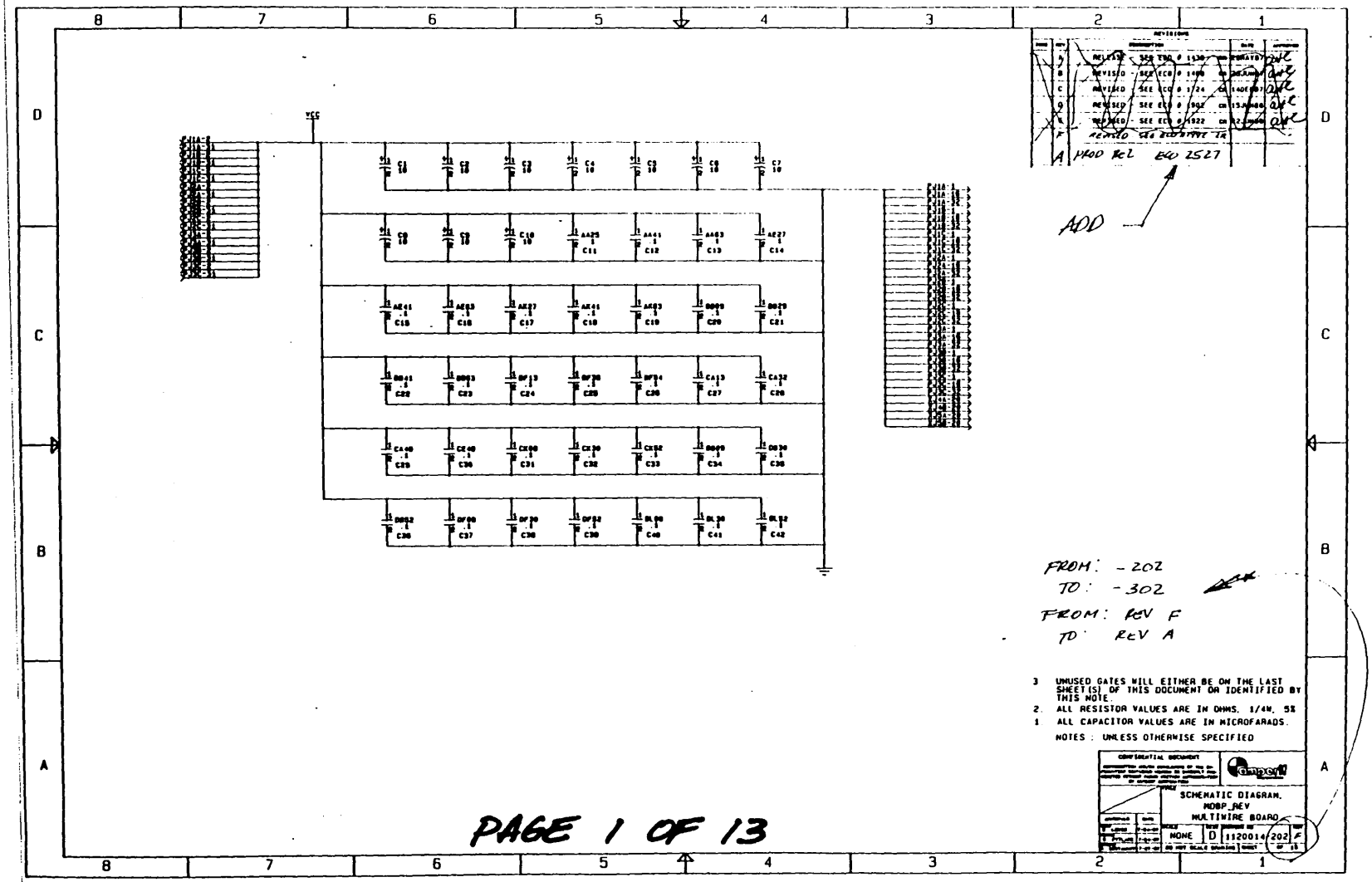
SCALE FULL | SIZE C | DRAWING NO 112000X-201 | REV U

DO NOT SCALE DRAWING | SHEET 2 OF 2

ECO 2527
SHT 9 OF 13

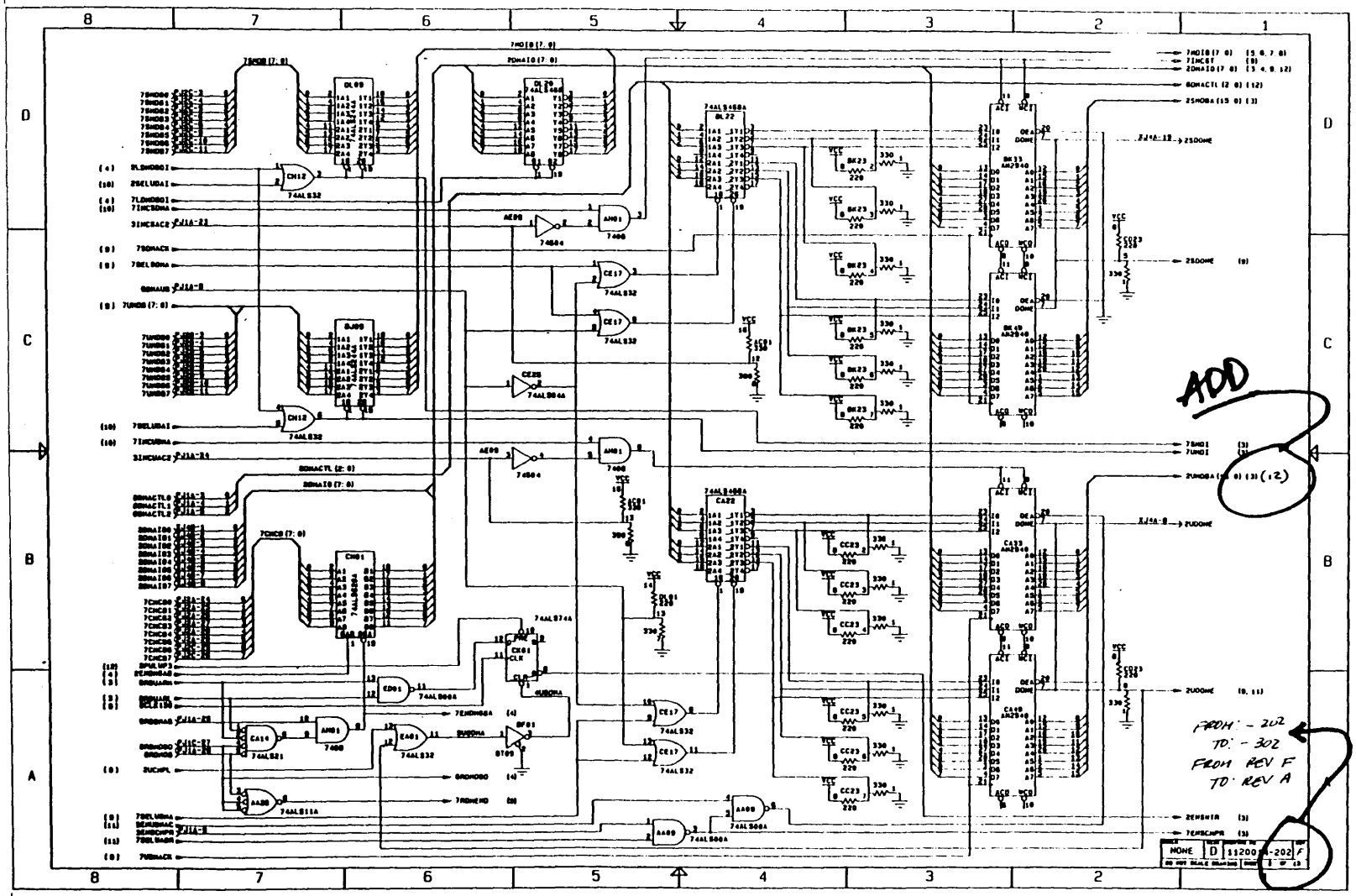
FEB 17 1989

PRELIMINARY



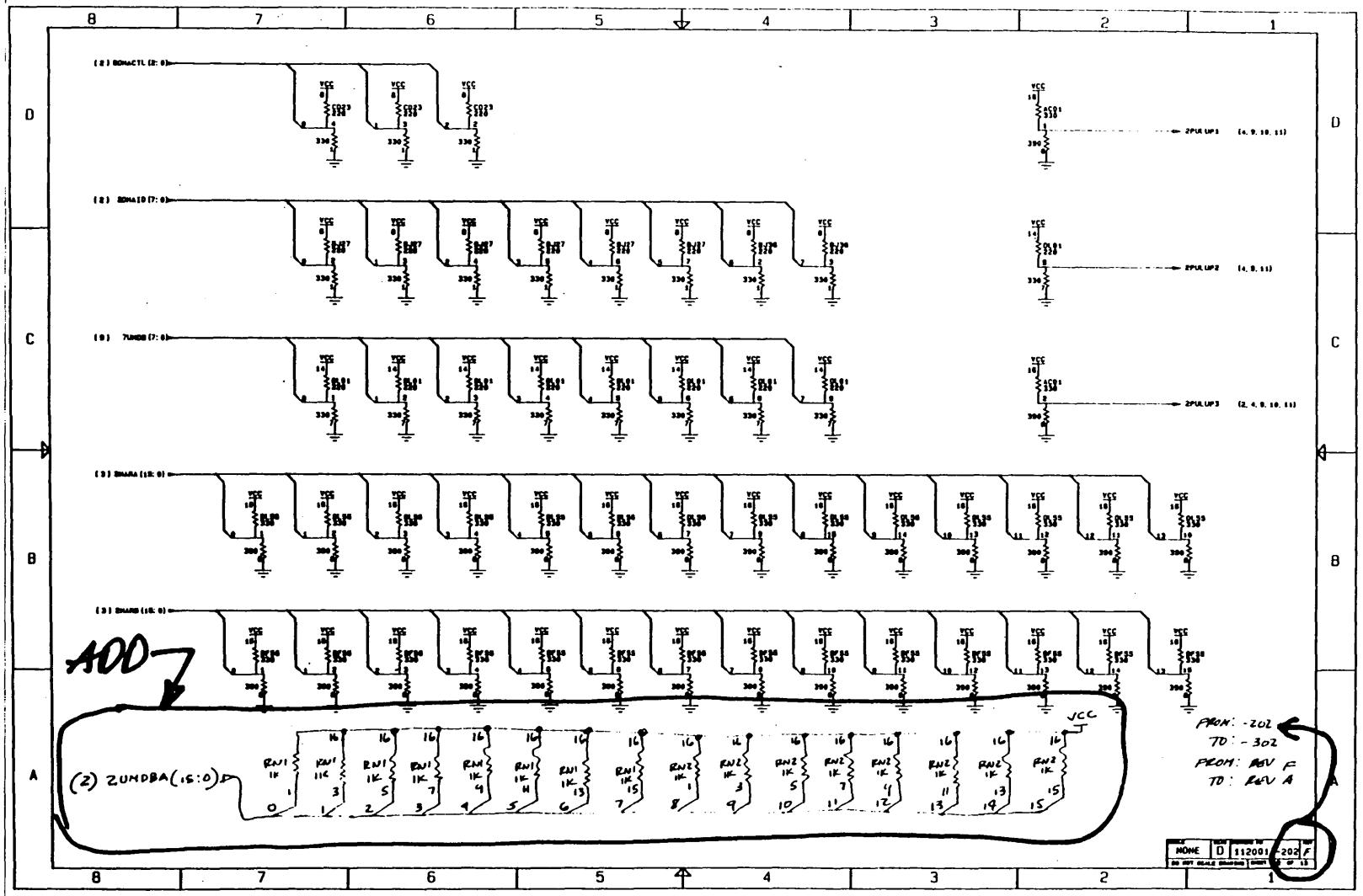
PAGE 1 OF 13

ECO 2527
SHT 10 OF 13



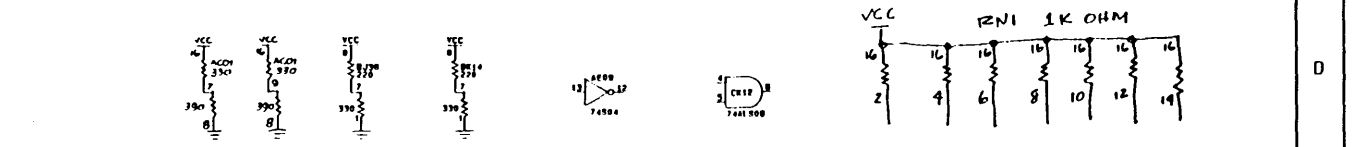
PAGE 2 OF 13

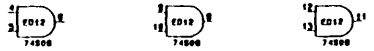
ECO 2527
SHT 11 OF 13

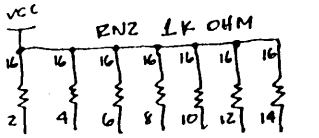


PAGE 12 OF 13

ECO 2527
SHT 12 OF 13







DEVICE VOLTAGE TABLE

DEV TYPE	GND	VCC	+12V	-12V	COMPONENT LOCATION
74S129	7	14			RP01
74S09	7	14			RP12
74S04	7	14			AC09
74S32	7	14			RP49
74S37	7	14			CE01
74S02	8	16			AC29
74S00	7	14			D-01
74S139	8	16			RP29
74S157	8	16			RP01
74S257	8	16			RP27
74S280	7	14			CH12, RP12
8T09	7	14			AC01, RP01
2107 SRAM	10	22			AA42, AA53, AC48, AC53, AE48
"	"	"			AC53, AH47, AH03, AK31, AK48
"	"	"			AK53, AM31, AM48, AM53, RP31
"	"	"			RP48, RP53, RP31, RP49, RP53
"	"	"			CH48, CH03, CK48, CK53, CH02
"	"	"			CM53, RP34, RP48, RP53, RP71
"	"	"			RP47, RP53, RP31, RP42, RP13
"	"	"			D-71, D-42, D-53, DL31, DL42
AM27S45	10	20			RP33, RP49, CA33, CA49
AM27S32	10	24			RP01, CA01
82S100	10	24			RP01, RP14
220/330 TE	8	8			D-27, D-30, RJ44, RK14, RP23
"	"	"			CC23, CD29
220/330 TE	7	14			DL01
7400	7	14			AM01
74S00	7	14			CD12
74F11	7	14			CC29
DEVTYPE	GRIM	VRIM			UK22
DEVTYPE	GRIM	VRIM			UK22

DEVICE VOLTAGE TABLE

DEV TYPE	GND	VCC	+12V	-12V	COMPONENT LOCATION
74ALS00	7	14			AA09, CD01
74ALS08	7	14			RP12
74ALS04	7	14			AA24, AM09, CE29
74ALS00	7	14			AK10, CK12
74ALS10	7	14			CM01
74ALS11	7	14			AA29
74ALS20	7	14			AK01
74ALS21	7	14			CA14
74ALS32	7	14			AK09, DL15, CE17, CH12, E401
74ALS74	7	14			AA01, CE01
74ALS112	8	16			AC10, AC15, AE10, AM01, AM10
"	"	"			RC35, D401
74ALS193	8	16			AM12
74ALS174	8	16			AA17
74ALS240	10	20			RP09, D-09, DL09
74ALS257	8	16			AM10
74ALS298	10	20			CM09, CM21
74ALS299	10	20			D-20, DL20
74ALS399	10	20			DL22, CA22
74ALS241	10	20			AE21, AM31, CK21, CM31, D009
"	"	"			RP29
74ALS374	10	20			RP01, RP12
74ALS823	10	20			CM01
74ALS260	10	20			CK20, CH20, D020, D029
74LS688	10	20			CE20, CE30
330/390 TE	8	16			AC01, RP35, DL35
1K OHM		16			RN1, RN2

ADD

FROM: -202
TO: -302
FROM: REV F
TO: REV A

NONE	D	1129014-202	F

PAGE 13 OF 13

ECO 2527
SHT 13 OF 13

ENGINEERING CHANGE REQUEST/ORDER

ECR ☒ ECO ☐

ECR/ECO NO. 2543

PROJ. TITLE	HDW	SFTWR	I&I	CHANGE LAL: YES NO	CHANGE CLASS A B C D	FIELD YES NO	AMENDMENTS
9200	☐	☒	☐	☐ ☒	☐ ☒ ☐ ☐	☒ YES ☐ NO	-

REGISTR/DRAWN: R. BUSTAMANTE, C. REYNOLDS, DATE: 2/28/89

CHECKED BY: R. WILLIAMS, DATE: 3-7-89

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☒ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☐ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: TO DETECT AND PREVENT DATA ERRORS CAUSED BY DECODE ERRORS OTHER DIF HARDWARE FAILURES. REDUCES UNDETECTED DATA ERRORS

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

	CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
		35GA0-01 to -03	NEW	A	MICROCODE, MPC OP SYS
3	1602314-101	1602314-101	NEW	A	PROM ASSY, MPC OP SYS 1 PL
3,5	1602314-102	1602314-102	NEW	A	PROM ASSY, MPC OP SYS 1 PL
3,6	1602314-103	1602314-103	NEW	A	PROM ASSY, MPC OP SYS 1 PL
7	1120016-301 to -701 *		—	—	ASSEMBLY DRAWING

9200-10

SN. 1227, 233

INCORPORATION/DISPOSITION

INCORP. OF CHANGE DATE 4-4-89 SERIAL NO. & up

SPECIAL INSTRUCTION:

	USE	REWORK	SCRAP	NOTE:
IN FIELD	☐	☒	☐	- FCO 9200-005
FIELD SPARES	☒	☐	☐	
FINISHED GOODS	☒	☐	☐	
FINAL ASSY	☒	☐	☐	
IN TEST	☐	☒	☐	
IN PROCESS	☐	☒	☐	
IN STOCK	☐	☐	☒	
NEXT ASSY	☐	☒	☐	
ON ORDER	☐	☒	☐	
NEXT BUY	☐	☒	☐	
OTHER ENT.	☐	☐	☐	

CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	GP (Acad)	3-16-89
SFTWR		
MARKETING	J. Hankins JH	3/16/89
MFG. ENG.	C. Carlson	3-23-89
QUALITY	S Seleman	3/16/89
SERVICE	B. Bug L 83	4/3/89
ENG. SERV.	J. Beras	4/3/89
DIR. OF ENG.		

ENGINEERING CHANGE REQUEST/ORDER

ECR/ECO NO. 2543

	CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
8	1120016-801	1120016-801 *	NEW	A	PCBA, MPCP & PL
11	1120016-302 to -702 *		—	—	ASSEMBLY DRAWING
12-14	1120016-802	1120016-802 *	NEW	A	PCBA, MPCP & PL
15	1120016-303 to -703 *		—	—	ASSEMBLY DRAWING
16-18	1120016-803	1120016-803 *	NEW	A	PCBA, MPCP & PL
19	1120016	—	K	L	CONFIGURATION LIST
20		1602159-001	L	M	9200 DISK CONTROLLER CARD KIT
21		1602159-201	K	L	PCBA KIT, CONTROLLER
22		5920003-FRU	N	P	9200-10 DUAL CNTRLR FRU LIST

* Renumber vellums of 1120016-TAB (3 sheets) to read 1 of 3 for (-801), 2 of 3 for (-802), and 3 of 3 for (-803).

* Update drawings per drafting standards.

* Update revision block (sht 1) to include all revisions. Remove revision blocks on sheets 2 & 3. Update all sheets to show the latest revision letter.

Remark : PCBA's 1120016-701, 1120016-702, 1120016-703

1. Remove component 1602180-301 from location CA01, replace with 1602314-101 Rev A.

2. Remove component 1602180-302 from location BK01, replace with 1602314-102 Rev A.

3. Remove component 1602180-303 from location BF01, replace with 1602314-103 Rev A.

4. Re-identify boards as follows :

1120016-701 Rev B	becomes	1120016-801 Rev A
1120016-702 Rev B	becomes	1120016-802 Rev A
1120016-703 Rev B	becomes	1120016-803 Rev A.

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PROM ASSEMBLY, MPC OP SYS

PL 1602314-101 to 103

SHEET 1 OF 1

REV. A

ITEM NO	QTY 101	QTY 102	QTY 103		AMPERIF P/N	REF DES	DESCRIPTION
1	1				20053500-002	35GA0-01A	PROM
2		1			20053500-002	35GA0-02A	PROM
3			1		20053500-002	35GA0-03A	PROM
4	1	1	1		20144913-001		LABEL

ECO # 2543

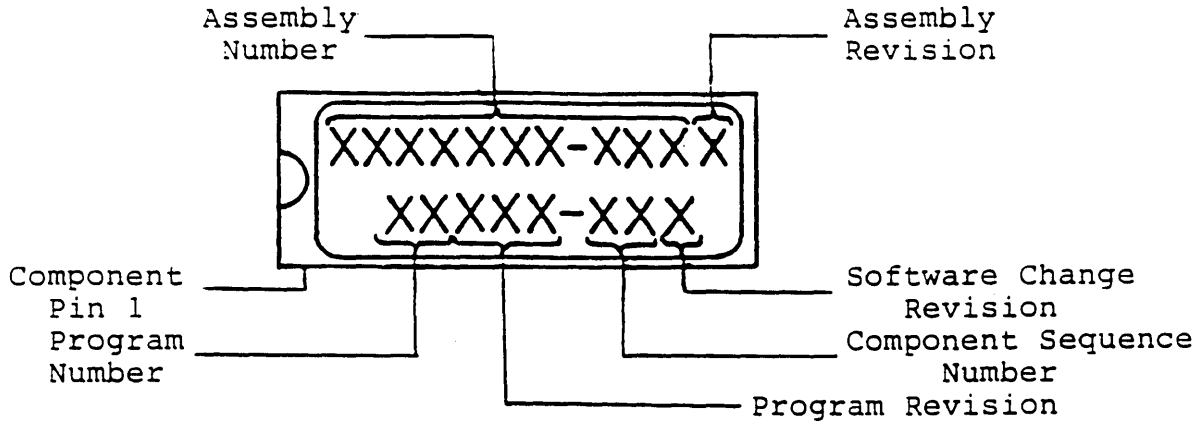
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
9	RELEASE - SEE ECO # 2543 CR		

Procedure:

1. Program component using data filed in software no. 35GA0-01A.

2. Make from unprogrammed part number 20053500-002.

3. Used on PCBA 1120016-801,802,803 Location CA01.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 01.

3. "Program Number" is 35. Revision GA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	2/28/89
CHECKER	
OTHER ECO # 2543	
APPROVED SHT 4 OF 22	

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PROM ASSEMBLY, MPC OP SYS

REV A

SIZE	DRAWING NO.	SHEET
A	1602314-101	1 OF 1

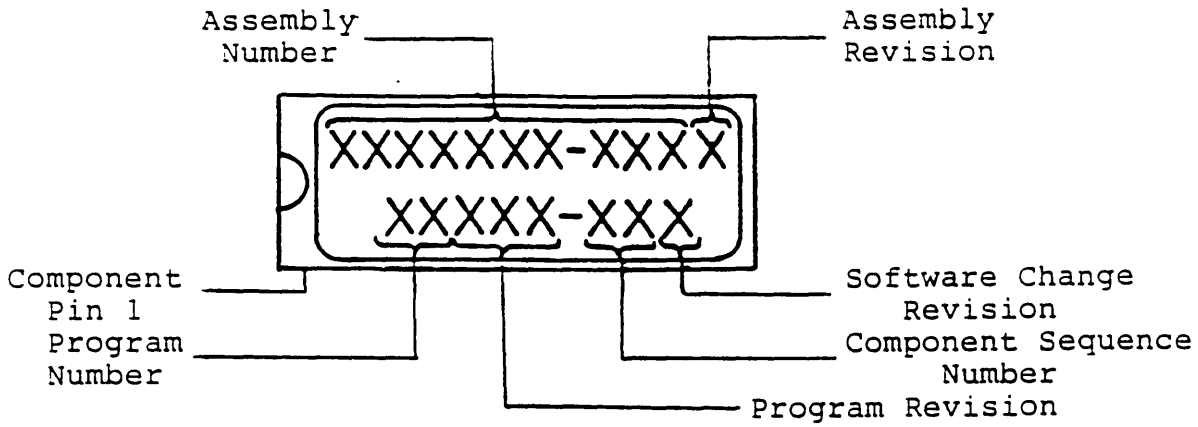
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - SEE ECO # 2543 CR		

Procedure:

1. Program component using data filed in software no. 35GA0-02A.

2. Make from unprogrammed part number 20053500-002.

3. Used on PCBA 1120016-801,802,803 Location BK01.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 02.

3. "Program Number" is 35 Revision GA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	4/28/89
CHECKER	
OTHER ECO # 2543	
APPROVED SHT 5 OF	22

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PROM ASSEMBLY, MPC OP SYS

REV A

SIZE	DRAWING NO.	SHEET
A	1602314-102	1 OF 1

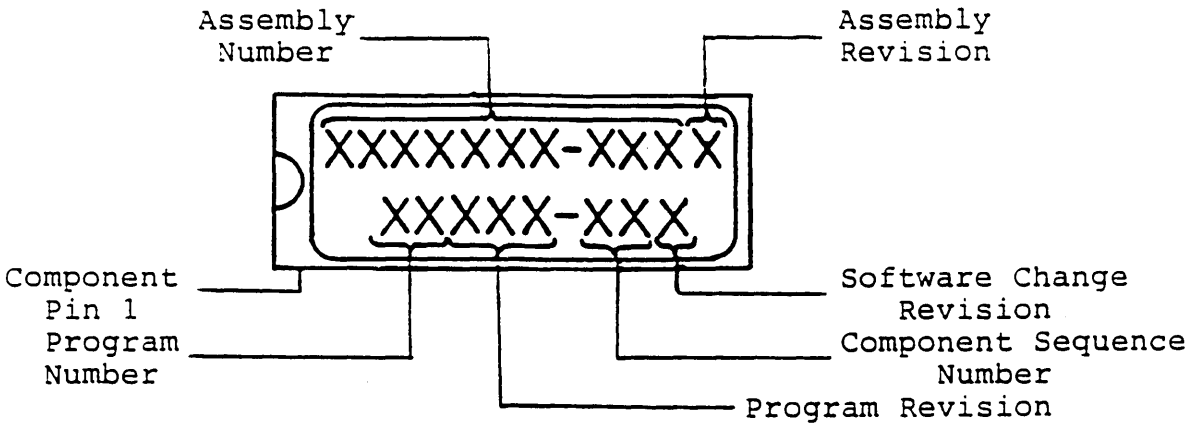
REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE - SEE ECO # 2543 CR		

Procedure:

1. Program component using data filed in software no. 35GA0-03A.

2. Make from unprogrammed part number 20053500-002.

3. Used on PCBA 1120016-801,802,803 Location BF01.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.
   Used on PCBA _____ Location _____.



6. For code listing see attached/separate listing.

5. "Software Change Revision" is A.

4. "Component Sequence Number" is 03.

3. "Program Number" is 35 Revision GA0.

2. Identify on adhesive-backed label per drawing above and affix label to programmed part as shown.

1. See separate parts list.

NOTES: Unless Otherwise Specified.

DOCUMENT RELEASE	DATE
ENGINEERING	
DRAFTSMAN Cheryl Reynolds	2/28/89
CHECKER	
OTHER ECO # 2543	
APPROVED SHT 6 OF 22	

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PROM ASSEMBLY, MPC OP SYS

REV A

SIZE	DRAWING NO.	SHEET
A	1602314-103	1 OF 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		... PER ECO ...	...	...
	C	... PER ECO ...	...	...
H		INC ECO # 2543		

DELETE WIRE FROM ... TO ...
DELETE WIRE FROM ... TO ...

WIRE TABLE

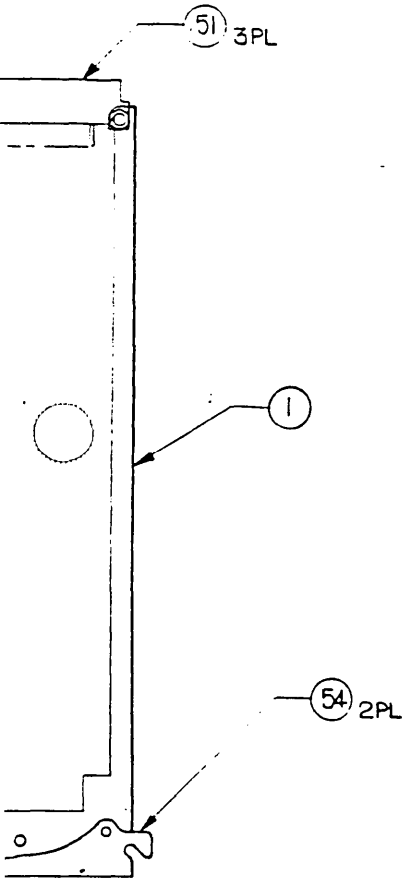
NO	FROM	TO
1	...	...

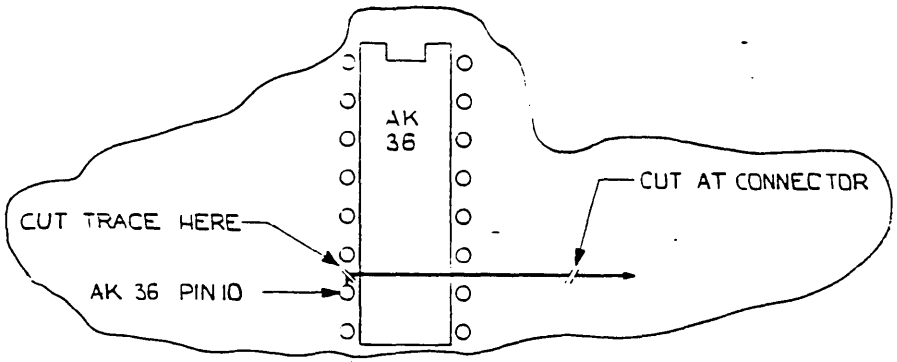
REWORK INSTRUCTION PER ECO # ...
REMOVE AND REPLACE COMPONENT AT ... LOCATION. SEE SEPARATE PL FOR NEW PN

REWORK INSTRUCTIONS PER ECO # 44
1. REWORK ONLY FOR ASSYS WITH BOARD ... REV. A. CUT TRACE PER DETAIL SHOWN.

REWORK INSTRUCTIONS PER ECO # ...
REMOVE PROMS AT LOCATION ... REPLACE WITH PROM P/N ... @ ... AND ... @ ...

FEB 28 1999





VIEWED FROM SOLDER SIDE

C	REWORK INSTRUCTIONS ECO# 1944			
1. CUT AND LIFT IC LEG @ LOCATION AK53-35				
JUMPER TABLE				
NO	CUT/ADD	FROM	TO	BOARD SIDE
2	ADD	AK28-11	AK53-35 (IC LEG)	COMPONENT
3	ADD	AK28-12	BD45-08	COMPONENT
4	ADD	AK23-3	BB01-09	COMPONENT

Assembly Revisions Not Shown : 1120016-701 or -70

From	C	to	D	ECO # 2321
From	D	to	E	ECO # 2420
From	E	to	F	ECO # 2406
From	F	to	G	ECO # 2430

ADD:

REV. STATUS	DASH NO.	DESCRIPTION	REMARKS
A	-801	PCBA, MPCP	SAME AS -701 EXCEPT LOCS. CA01, BK01, & BF01.
B	-501	PCBA, MPCP	SAME AS -301 EXCEPT COMPONENTS @ LOCS. BF01, BK01 & CA31
B	-301	PCBA, MPCP	(SHOWN- REF.)

SEE SEPARATE PL

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amperif

PCB ASSEMBLY-
MPCP MULTIWIRE BOARD

APPROVALS	DATE
...	3-1-00

SCALE NONE | SIZE D | DRAWING NO 1120016-TAB | REV C

DO NOT SCALE DRAWING | SHEET 1 OF

EAR 2543 SHT 1 OF 22

LI.200.1.DATABA01 AMPERIF CORPORATION DISTRIBUTION: CHERYLL - ENG SERVICES

TUE, FEB [illegible] 1989 BILL OF MATERIAL PAGE NO: 1

AS OF DATE

CLASS CODE: 28
PCBA OUTSIDE

801

A

1120014-201 TYPCODE: 3 REV: B PL. MPCP PCBA

MODEL:

ECN NO: 2430

DATE OF LAST ECO: 1/20/89

2543

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

ECN #

DELETE:

SHT 2 OF 2

PART NUMBER	DESCRIPTION	OP	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
0120015	MPCP MULTIWIRE BD	3	E	1	1.000	1.000	EA	B	Y	N	1.000	0	0	REV:E	00/00/00	99/99/99
1602180-201	PROM ASSY,MPC UP SYS	3	B	62	1.000	1.000	EA	B	Y	N	1.000	0	0	CA01	11/18/88	11/18/88
1602180-202	PROM ASSY,MPC UP SYS	3	A	63	1.000	1.000	EA	B	Y	N	1.000	0	0	BK01	11/18/88	11/18/88
1602180-203	PROM ASSY,MPC UP SYS	3	A	64	11.000	1.000	EA	B	Y	N	11.000	0	0	BF01	11/18/88	11/18/88
1602180-301	PROM ASSY,MPCP UP SYS	3	B	62	1.000	1.000	EA	B	Y	N	1.000	0	0	CA01	00/00/00	99/99/99
1602180-302	PROM ASSY,MPCP UP SYS	3	A	63	1.000	1.000	EA	B	Y	N	1.000	0	0	BK01	00/00/00	99/99/99
1602180-303	PROM ASSY,MPCP UP SYS	3	A	64	11.000	1.000	EA	B	Y	N	11.000	0	0	BF01	00/00/00	99/99/99
20000700	IC,INV,HEX,SCHMITT,7414	3	A	29	1.000	1.000	EA	P	Y	N	1.000	0	0	AC28	00/00/00	99/99/99
20002500	IC,BUFR,QUAD,3ST,74125	3	A	2	1.000	1.000	EA	P	Y	N	1.000	0	0	DF34	00/00/00	99/99/99
20005200	IC,NAND,TRI-3,S10	3	A	3	1.000	1.000	EA	P	Y	N	1.000	0	0	CM09	00/00/00	99/99/99
20005200	IC,NAND,QUAD-2,S37	3	A	52	1.000	1.000	EA	P	Y	N	1.000	0	0	CM01	00/00/00	99/99/99
20005900	IC,F/F,DUAL-D,S74	3	A	4	1.000	1.000	EA	P	Y	N	1.000	0	0	AH56	00/00/00	99/99/99
20006100	IC,XOR,QUAD-2,S86	3	A	5	1.000	1.000	EA	P	Y	N	1.000	0	0	DF43	00/00/00	99/99/99
20006600	IC,DEMUX,2TO4,S139	3	A	6	1.000	1.000	EA	P	Y	N	1.000	0	0	BB43	00/00/00	99/99/99
20007000	IC,MUX,QUAD,1OF2,S157	3	A	7	3.000	1.000	EA	P	Y	N	3.000	0	0	AC10,BB12 CH23	00/00/00	99/99/99
20008800	IC,GEN,PRTY,9BIT,S280	3	A	9	1.000	1.000	EA	P	Y	N	1.000	0	0	DF76	00/00/00	99/99/99
20012100	IC,M-PROC,4BIT,SLICE,2901	3	A	10	2.000	1.000	EA	P	Y	N	2.000	0	0	CA14,CA35	00/00/00	99/99/99
20014300	RES,DIP,16P,4700HM,COM	3	A	11	4.000	1.000	EA	P	Y	N	4.000	0	0	AE52,AK10 CH14,CK49	00/00/00	99/99/99
20014800	IC,DIP,16P,330/390,TERM	3	A	12	2.000	1.000	EA	P	Y	N	2.000	0	0	AC01,AK01	00/00/00	99/99/99
20015100	RES,DIP,14P,470HM,COM	3	A	13	1.000	1.000	EA	P	Y	N	1.000	0	0	CM49	00/00/00	99/99/99
20018902	CAP,TANT,RAD,100F,20%,16V	3	A	15	6.000	1.000	EA	P	Y	N	6.000	0	0	C1-C5 C6(AC39)	00/00/00	99/99/99
20019503	SKT,DIP,14P,PCMT	3	A	16	1.000	1.000	EA	P	Y	N	1.000	0	0	XCK01	00/00/00	99/99/99
20019803	SKT,DIP,24P,PCMT	3	A	17	3.000	1.000	EA	P	Y	N	3.000	0	0	XBF01 XBK01 XCA01	00/00/00	99/99/99
20041716	RES,CARB,1K,1/4W,5%	3	A	53	1.000	1.000	EA	P	Y	N	1.000	0	0	R1(AC36)	00/00/00	99/99/99
20042816	RES,CARB,4.7K,1/4W,5%	3	A	18	1.000	1.000	EA	P	Y	N	1.000	0	0	R2(CH13)	00/00/00	99/99/99
20058400	IC,LATCH,8BIT,LS259	3	A	20	5.000	1.000	EA	P	Y	N	5.000	0	0	AA19,AE19 AH10,AH19 AM10	00/00/00	99/99/99
20066899	IC,NAND,QUAD-2,ALS00	3	A	21	2.000	1.000	EA	P	Y	N	2.000	0	0	AK36,BD45	00/00/00	99/99/99
20067099	IC,INV,HEX,ALS04	3	A	22	3.000	1.000	EA	P	Y	N	3.000	0	0	AM28,BB52 CM17	00/00/00	99/99/99
20067199	IC,AND,QUAD-2,ALS08	3	A	23	4.000	1.000	EA	P	Y	N	4.000	0	0	AE36,AK28 BD53,DF18	00/00/00	99/99/99
20067299	IC,NAND,TRI-3,ALS10	3	A	24	1.000	1.000	EA	P	Y	N	1.000	0	0	AM36	00/00/00	99/99/99
20067399	IC,AND,TRI-3,ALS11	3	A	25	1.000	1.000	EA	P	Y	N	1.000	0	0	AC52	00/00/00	99/99/99
20067499	IC,NAND,DUAL-4,ALS20	3	A	26	1.000	1.000	EA	P	Y	N	1.000	0	0	AK53	00/00/00	99/99/99

[illegible] CORPORATION

AS OF ALT DATE

801

A

CLASS CODE: 28
PCBA OUTSIDE

1120016 /01 UPCODE: 3 REV: B PL, MPLP PCBA

MODEL:

ECO NO: 2430

DATE OF LAST ECO: 1/20/89

2543

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
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PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	O P	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	R E Q	P F	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20067599	IC,AND,DUAL-4,ALS21	3	A	27	1.000	1.000	EA	P	Y	N	1.000	0	0	BB01	00/00/00	99/99/99
20067899	IC,OR,QUAD-2,ALS32	3	A	28	5.000	1.000	EA	P	Y	N	5.000	0	0	AA28,AA36 AE28,AH28 DF10	00/00/00	99/99/99
20068199	IC,F/F,DUAL-D,ALS74	3	A	30	3.000	1.000	EA	P	Y	N	3.000	0	0	AA44,AA52 AE44	00/00/00	99/99/99
20068199	IC,F/F,DUAL-JK,ALS112	3	A	31	2.000	1.000	EA	P	Y	N	2.000	0	0	AK19,DF01	00/00/00	99/99/99
20068299	IC,DEMUX,3TO8,ALS138	3	A	32	9.000	1.000	EA	P	Y	N	9.000	0	0	AA01,AA10 AE01,AE10 AH01,AM19 BB34,CM3H DD43	00/00/00	99/99/99
20068799	IC,F/F,HEX-D,ALS174	3	A	33	1.000	1.000	EA	P	Y	N	1.000	0	0	AK44	00/00/00	99/99/99
20068800	IC,DRVR,OCTAL,3ST,ALS244	3	A	34	5.000	1.000	EA	P	Y	N	5.000	0	0	BB23,BD34 CK27,CK38 DD23	00/00/00	99/99/99
20068999	IC,MUX,10FB,3ST,ALS251	3	A	35	2.000	1.000	EA	P	Y	N	2.000	0	0	AH47,AM53	00/00/00	99/99/99
20069099	IC,MUX,QUAD,10F2,3ST,ALS257	3	A	36	1.000	1.000	EA	P	Y	N	1.000	0	0	CH43	00/00/00	99/99/99
20069199	IC,DRVR,OCTAL,3ST,ALS465	3	A	37	1.000	1.000	EA	P	Y	N	1.000	0	0	CM27	00/00/00	99/99/99
20069699	IC,F/F,OCTAL-D,3ST,ALS574	3	A	38	3.000	1.000	EA	P	Y	N	3.000	0	0	BD01,BD12 BD23	00/00/00	99/99/99
20069799	IC,F/F,OCTAL-D,3ST,ALS576	3	A	39	2.000	1.000	EA	P	Y	N	2.000	0	0	CE35,DD11	00/00/00	99/99/99
20069899	IC,XCVR,OCTAL,3ST,ALS620	3	A	40	1.000	1.000	EA	P	Y	N	1.000	0	0	DD12	00/00/00	99/99/99
20070099	IC,GEN,LOOK-AHEAD,S182	3	A	41	1.000	1.000	EA	P	Y	N	1.000	0	0	DD34	00/00/00	99/99/99
20071399	IC,CNTLR,M-PROG,12BIT,2910A	3	A	42	1.000	1.000	EA	P	Y	N	1.000	0	0	CD01	00/00/00	99/99/99
20071499	IC,RGSTR,QUAD-D,3ST,2918	3	A	43	1.000	1.000	EA	P	Y	N	1.000	0	0	CH34	00/00/00	99/99/99
20071599	IC,GEN,CLK,CNTLR,2925	3	A	44	1.000	1.000	EA	P	Y	N	1.000	0	0	CH01	00/00/00	99/99/99
20072199	OSC,40MHZ,14P,DIP	3	A	46	1.000	1.000	EA	P	Y	N	1.000	0	0	CK01	00/00/00	99/99/99
20084211	SW,TOG,SPDT,R/A,PCMT	3	A	47	1.000	1.000	EA	P	Y	N	1.000	0	0	SW1(BD65)	00/00/00	99/99/99
20084314	LED,R/A,RED,PCMT,.3",W/RES	3	A	48	1.000	1.000	EA	P	Y	N	1.000	0	0	L5(CJ62)	00/00/00	99/99/99
20084414	LED,R/A,GRN,PCMT,.3",W/RES	3	A	49	1.000	1.000	EA	P	Y	N	1.000	0	0	L6(CK62)	00/00/00	99/99/99
20084514	LED,R/A,YEL,PCMT,.3",W/RES	3	A	50	4.000	1.000	EA	P	Y	N	4.000	0	0	L1(CL62) L2(DA62) L3(DE62) L4(AK62)	00/00/00	99/99/99
20091008	CONN,DIN,96P,MALE,RA,.180,LEAD	3	A	51	3.000	1.000	EA	P	Y	N	3.000	0	0	PJ1,PJ2 PJ3	00/00/00	99/99/99
20091611	SW,TOG,R/A,MOM,SPDT,PCMT	3	A	52	1.000	1.000	EA	P	Y	N	1.000	0	0	SW4	00/00/00	99/99/99
20094208	CONN,HDR,2X20,MALE,R/A,SHRD	3	A	55	2.000	1.000	EA	P	Y	N	2.000	0	0	XJ4,XT5	00/00/00	99/99/99
20098499	IC,INV,OCT,3ST,LS240	3	A	56	1.000	1.000	EA	P	Y	N	1.000	0	0	AH36	00/00/00	99/99/99
20102213	EXTR,CARD,W/O LOCK	3	A	54	2.000	1.000	EA	P	Y	N	2.000	0	0		00/00/00	99/99/99

AS OF ADD DATE

CLASS CODE: 28
PCBA OUTSIDE

901

A

1121001A-001 TYPCODE: 3 REV: B PL, MPCP PCBA

MODEL:

ECO NO: 2431

DATE OF LAST ECO: 1/20/89

2543

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSULETE DATE
20119513-007	SCREW,PNHPH,2-56X1/2	3	A	59	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20121713-001	NUT,HEX,PLAIN,2-56	3	A	60	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20122113-001	WSHR,SPLK,#2	3	A	61	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20125611-001	SW,PB,SPDT,R/A,PCMT	1	A	58	1.000	1.000	EA	P	Y	N	1.000	0	0	SW3(AM65)	00/00/00	99/99/99
20136900-001	IC,CNTR,BIN,F163	3	A	8	2.000	1.000	EA	P	Y	N	2.000	0	0	CK09,CK18	00/00/00	99/99/99
20143800-001	IC,DEMUX,3TO8,LS138	3	A	65	1.000	1.000	EA	P	Y	N	1.000	0	0	AM01	00/00/00	99/99/99
20148202-001	CAP,CER,DIP,.1UF,50V,20%	3	A	14	30.000	1.000	EA	P	Y	N	30.000	0	0	C7-C36	00/00/00	99/99/99

ADD:

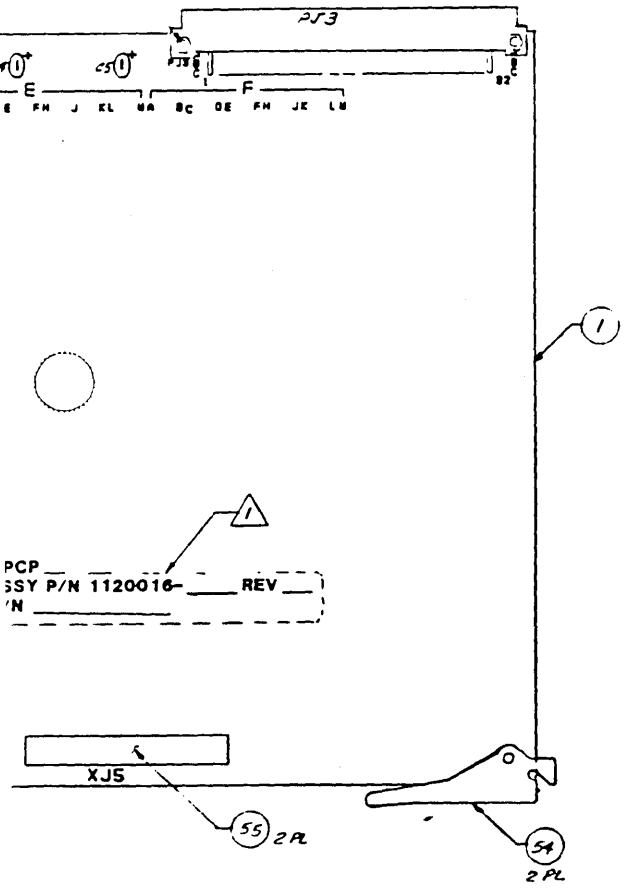
1602314-101	PROM ASSY,MPC OP SYS	62	1.000		1.000	CA01
1602314-102	PROM ASSY,MPC OP SYS	63	1.000		1.000	BK01
1602314-103	PROM ASSY,MPC OP SYS	64	1.000		1.000	BF01

EXA # 2 of 3

SHT 10 OF 22

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
E	CHG PER ECO # 1793	RM	
M	INC ECO #		

FEB 28 1989



B	REWORK INSTRUCTION ECO # 1726
	1. CUT ETCH @ LOC SW3-03 (SOLDER SIDE) SEE DETAIL A)

E	REWORK INSTRUCTION ECO # 1793
	1. REMOVE AND REPLACE COMPONENTS AT CA01, BK01, AND BF01 WITH 601894-101 REV B, 1601894-102 REV B, AND 601894-103 REV C.

C	REWORK INSTRUCTIONS ECO # 1944			
	1. CUT AND LIFT IC LEG @ LOCATION AK53-05			
	JUMPER TABLE			
NO	CUT/ADD	FROM	TO	BOARD SIDE
2	ADD	AK28-11	AK53-05 (IC LEG)	COMPONENT
3	ADD	AK28-12	BD45-08	COMPONENT
4	ADD	AK28-13	BB01-09	COMPONENT

Assembly Revisions Not Shown : 1120016-302 to -702

From	G	to	H	ECO # 2321
From	H	to	J	ECO # 2420
From	J	to	K	ECO # 2406
From	K	to	L	ECO # 2430

SEE SEPARATE PARTS LIST

ADD: 3

REV	DASH	DESCRIPTION	REMARKS
A	-802	PCBA, MPCP	SAME AS -702 EXCEPT LOCS. CA01, BK01, & BF01.
B	-502	PCBA, MPCP	SAME AS -302 EXCEPT LOCATIONS: BF01, BK01 & CA01.
F	-302	PCBA, MPCP	(SHOWN - REF.)

CONFIDENTIAL DOCUMENT
REPRODUCTION AND/OR DISCLOSURE OF THE INFORMATION CONTAINED HEREIN IS STRICTLY PROHIBITED WITHOUT PRIOR WRITTEN AUTHORIZATION BY AMPERIF CORP

amperif

PCB ASSEMBLY:
MPCP MULTIWIRE BOARD

APPROVALS	DATE
L.A.	9-87

SCALE 1:1 | SIZE D | DRAWING NO 1120016-TAB 6

302

802

CLASS CODE: 28
PCBA OUTSIDE

A

1120014-002 UPGRADE: 3 REV: H PL, MPCP PCBA
MODEL:
ECO NO: 2431
DATE OF LAST ECO: 1/20/89

2543

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
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PF: Y=PART PRINTS ON SALES ORDER
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PART NUMBER	DESCRIPTION	OP	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
0120015-002	PWB&FAB,MPCP	3	E	1	1.000	1.000	EA	B	Y	N	1.000	0	0		00/00/00	99/99/99
1602180-201	PROM ASSY,MPC OP SYS	3	B	62	1.000	1.000	EA	B	Y	N	1.000	0	0	CA01	11/18/88	11/18/88
1602180-202	PROM ASSY,MPC OP SYS	3	A	63	1.000	1.000	EA	B	Y	N	1.000	0	0	BK01	11/18/88	11/18/88
1602180-203	PROM ASSY,MPC OP SYS	3	A	64	1.000	1.000	EA	B	Y	N	1.000	0	0	BE01	11/18/88	11/18/88
1602180-301	PROM ASSY,MPCP OP SYS	3	B	62	1.000	1.000	EA	B	Y	N	1.000	0	0	CA01	00/00/00	99/99/99
1602180-302	PROM ASSY,MPCP OP SYS	3	A	63	1.000	1.000	EA	B	Y	N	1.000	0	0	BK01	00/00/00	99/99/99
1602180-303	PROM ASSY,MPCP OP SYS	3	A	64	1.000	1.000	EA	B	Y	N	1.000	0	0	BE01	00/00/00	99/99/99
20000700	IC,INV,HEX,SCHMITT,7414	3	A	29	1.000	1.000	EA	P	Y	N	1.000	0	0	AC28	00/00/00	99/99/99
20002500	IC,BUFR,QUAD,3ST,74125	3	A	2	1.000	1.000	EA	P	Y	N	1.000	0	0	DF34	00/00/00	99/99/99
20005200	IC,NAND,TRI-3,S10	3	A	3	1.000	1.000	EA	P	Y	N	1.000	0	0	CM09	00/00/00	99/99/99
20005700	IC,NAND,QUAD-2,S37	3	A	52	1.000	1.000	EA	P	Y	N	1.000	0	0	CM01	00/00/00	99/99/99
20005900	IC,F/F,DUAL-D,S74	3	A	4	1.000	1.000	EA	P	Y	N	1.000	0	0	AH56	00/00/00	99/99/99
20006100	IC,XOR,QUAD-2,S86	3	A	5	1.000	1.000	EA	P	Y	N	1.000	0	0	DF43	00/00/00	99/99/99
20006600	IC,DEMUX,2TO4,S139	3	A	6	1.000	1.000	EA	P	Y	N	1.000	0	0	BB43	00/00/00	99/99/99
20007000	IC,MUX,QUAD,1OF2,S157	3	A	7	3.000	1.000	EA	P	Y	N	3.000	0	0	AC10,BB12 CH23	00/00/00	99/99/99
20008800	IC,GEN,PRTY,9BIT,S280	3	A	9	1.000	1.000	EA	P	Y	N	1.000	0	0	DF26	00/00/00	99/99/99
20012100	IC,M-PROC,4BIT,SLICE,2901	3	A	10	2.000	1.000	EA	P	Y	N	2.000	0	0	CA14,CA35	00/00/00	99/99/99
20014300	RES,DIP,16P,470OHM,COM	3	A	11	4.000	1.000	EA	P	Y	N	4.000	0	0	AF52,AK10 CH14,CK49	00/00/00	99/99/99
20014800	IC,DIP,16P,330/390,TERM	3	A	12	2.000	1.000	EA	P	Y	N	2.000	0	0	AC01,AK01	00/00/00	99/99/99
20015100	RES,DIP,14P,470OHM,COM	3	A	13	1.000	1.000	EA	P	Y	N	1.000	0	0	CM49	00/00/00	99/99/99
20018402-003	CAP,CE,RAD,.1UF,50V,20%	3	A	14	30.000	1.000	EA	P	Y	N	30.000	0	0	C2-C36	00/00/00	99/99/99
20018902	CAP,TANT,RAD,10UF,20%,16V	3	A	15	6.000	1.000	EA	P	Y	N	6.000	0	0	C1-C5 C6(AC39)	00/00/00	99/99/99
20019503	SKT,DIP,14P,PCMT	3	A	16	1.000	1.000	EA	P	Y	N	1.000	0	0	XCK01	00/00/00	99/99/99
20019803	SKT,DIP,24P,PCMT	3	A	17	3.000	1.000	EA	P	Y	N	3.000	0	0	XBF01 XBK01 XCA01	00/00/00	99/99/99
20041216	RES,CARB,1K,1/4W,5%	3	A	53	1.000	1.000	EA	P	Y	N	1.000	0	0	R1(AC36)	00/00/00	99/99/99
20042816	RES,CARB,4.7K,1/4W,5%	3	A	18	1.000	1.000	EA	P	Y	N	1.000	0	0	R2(CH13)	00/00/00	99/99/99
20058400	IC,LATCH,8BIT,LS259	3	A	20	5.000	1.000	EA	P	Y	N	5.000	0	0	AA19,AE19 AH10,AH19 AM10	00/00/00	99/99/99
20066899	IC,NAND,QUAD-2,ALS00	3	A	21	2.000	1.000	EA	P	Y	N	2.000	0	0	AK36,BD45	00/00/00	99/99/99
20067099	IC,INV,HEX,ALS04	3	A	22	3.000	1.000	EA	P	Y	N	3.000	0	0	AM28,BB52 CM17	00/00/00	99/99/99
20067199	IC,AND,QUAD-2,ALS08	3	A	23	4.000	1.000	EA	P	Y	N	4.000	0	0	AE36,AK28 BD53,DF18	00/00/00	99/99/99
20067299	IC,NAND,TRI-3,ALS10	3	A	24	1.000	1.000	EA	P	Y	N	1.000	0	0	AM36	00/00/00	99/99/99
20067399	IC,AND,TRI-3,ALS11	3	A	25	1.000	1.000	EA	P	Y	N	1.000	0	0	AC52	00/00/00	99/99/99

CLASS CODE: 28
PCBA OUTSIDE

802 A

1120016/202 UPCODE: 3 REV: A PL, MPCP PCBA
MODEL:
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2543

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20062499	IC,NAND,DUAL-4,ALS20	3	A	26	1.000	1.000	EA	P	Y	N	1.000	0	0	AK53	00/00/00	99/99/99
20062599	IC,AND,DUAL-4,ALS21	3	A	27	1.000	1.000	EA	P	Y	N	1.000	0	0	BB01	00/00/00	99/99/99
20062899	IC,OR,QUAD-2,ALS32	3	A	28	5.000	1.000	EA	P	Y	N	5.000	0	0	AA28,AA36 AE28,AH28 DF10	00/00/00	99/99/99
20068099	IC,F/F,DUAL-D,ALS74	3	A	30	3.000	1.000	EA	P	Y	N	3.000	0	0	AA44,AA52 AE44	00/00/00	99/99/99
20068199	IC,F/F,DUAL-JK,ALS112	3	A	31	2.000	1.000	EA	P	Y	N	2.000	0	0	AK19,DF01	00/00/00	99/99/99
20068299	IC,DEMUX,3TO8,ALS138	3	A	32	9.000	1.000	EA	P	Y	N	9.000	0	0	AA01,AA10 AE01,AE10 AH01,AM19 BB34,CM38 DD43	00/00/00	99/99/99
20068799	IC,F/F,HEX-D,ALS174	3	A	33	1.000	1.000	EA	P	Y	N	1.000	0	0	AK44	00/00/00	99/99/99
20068800	IC,DRVR,OCTAL,3ST,ALS244	3	A	34	5.000	1.000	EA	P	Y	N	5.000	0	0	BB23,BD34 CK27,CK38 DD23	00/00/00	99/99/99
20068999	IC,MUX,10F8,3ST,ALS251	3	A	35	2.000	1.000	EA	P	Y	N	2.000	0	0	AH47,AM53	00/00/00	99/99/99
20069099	IC,MUX,QUAD,10F2,3ST,ALS257	3	A	36	1.000	1.000	EA	P	Y	N	1.000	0	0	CH43	00/00/00	99/99/99
20069199	IC,DRVR,OCTAL,3ST,ALS465	3	A	37	1.000	1.000	EA	P	Y	N	1.000	0	0	CM27	00/00/00	99/99/99
20069699	IC,F/F,OCTAL-D,3ST,ALS574	3	A	38	3.000	1.000	EA	P	Y	N	3.000	0	0	BD01,BD12 BD23	00/00/00	99/99/99
20069799	IC,F/F,OCTAL-D,3ST,ALS576	3	A	39	2.000	1.000	EA	P	Y	N	2.000	0	0	CE35,DD01	00/00/00	99/99/99
20069899	IC,XCVR,OCTAL,3ST,ALS620	3	A	40	1.000	1.000	EA	P	Y	N	1.000	0	0	DD12	00/00/00	99/99/99
20070099	IC,GEN,LOOK-AHEAD,S182	3	A	41	1.000	1.000	EA	P	Y	N	1.000	0	0	DD34	00/00/00	99/99/99
20071399	IC,CNTLR,M-PROG,12BIT,2910A	3	A	42	1.000	1.000	EA	P	Y	N	1.000	0	0	CD01	00/00/00	99/99/99
20071499	IC,RGSTR,QUAD-D,3ST,291B	3	A	43	1.000	1.000	EA	P	Y	N	1.000	0	0	CH34	00/00/00	99/99/99
20071599	IC,GEN,CLK,CNTLR,2925	3	A	44	1.000	1.000	EA	P	Y	N	1.000	0	0	CH01	00/00/00	99/99/99
20072199	OSC,40MHZ,14P,DIP	3	A	46	1.000	1.000	EA	P	Y	N	1.000	0	0	CK01	00/00/00	99/99/99
20084211	SW,TOG,SPDT,R/A,PCMT	3	A	47	1.000	1.000	EA	P	Y	N	1.000	0	0	SW1(BD65)	00/00/00	99/99/99
20084314	LED,R/A,RED,PCMT,.3",W/RES	3	A	48	1.000	1.000	EA	P	Y	N	1.000	0	0	L6(CK62)	00/00/00	99/99/99
20084414	LED,R/A,GRN,PCMT,.3",W/RES	3	A	49	1.000	1.000	EA	P	Y	N	1.000	0	0	L5(CJ62)	00/00/00	99/99/99
20084514	LED,R/A,YEL,PCMT, 3",W/RES	3	A	50	4.000	1.000	EA	P	Y	N	4.000	0	0	L1(CL62) L2(DA62) L3(DE62) L4(AK62)	00/00/00	99/99/99
20091008	CONN,DIN,96P,MALE,RA,.180,LEAD	3	A	51	3.000	1.000	EA	P	Y	N	3.000	0	0	PJ1,PJ2 PJ3	00/00/00	99/99/99
20094208	CONN,HDR,2X20,MALE,R/A,SHRD	3	A	55	2.000	1.000	EA	P	Y	N	2.000	0	0	XJ4,XT5	00/00/00	99/99/99
20098499	IC,INV,OCT,3ST,LS240	3	A	56	1.000	1.000	EA	P	Y	N	1.000	0	0	AH36	00/00/00	99/99/99
20102213	EXTR,CARD,W/O EJECK	3	A	54	2.000	1.000	EA	P	Y	N	2.000	0	0		00/00/00	99/99/99

802 A

CLASS CODE: 28
PCBA OUTSIDE

1120001-202 TYPCODE: 3 REV: B PC, MPCP PCBA
MODEL:
ECO NO: 2431
DATE OF LAST ECO: 1/20/89
2543

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20119513-002	SCREW,PNHPH,2-56X1/2	3	A	59	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20121713-001	NUT,HEX,PLAIN,2-56	3	A	60	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20122113-001	WSHR,SPLK,#2	3	A	61	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20125611-001	SW,PB,SPDT,R/A,PCMT	1	A	58	1.000	1.000	EA	P	Y	N	1.000	0	0	SW3(AM65)	00/00/00	99/99/99
20136900-001	IC,CNTR,BIN,F163	3	A	8	2.000	1.000	EA	P	Y	N	2.000	0	0	CK09,CK18	00/00/00	99/99/99
20143800-001	IC,DEMUX,3TO8,LS138	3	A	65	1.000	1.000	EA	P	Y	N	1.000	0	0	AM01	00/00/00	99/99/99

ECO # 2543

ADD:

1602314-101	PROM ASSY, MPC OP SYS	62	1.000		1.000	CA01
1602314-102	PROM ASSY, MPC OP SYS	63	1.000		1.000	BK01
1602314-103	PROM ASSY, MPC OP SYS	64	1.000		1.000	BF01

SHT 14 OF 22

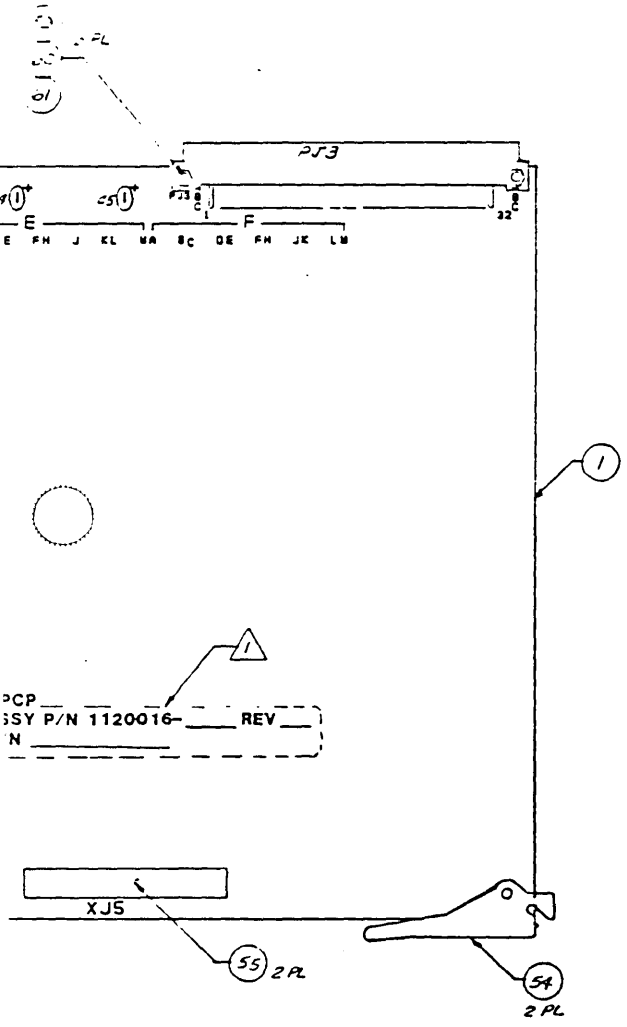
4 3 2 1

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
	A			
	B	[illegible]		
	C	[illegible]		
	H	INC ECO # 2573		

D

FEB 28 1989



C

B

Assembly Revisions Not Shown : 1120016-303 to -703

From	C	to	D	ECO # 2321
From	D	to	E	ECO # 2420
From	E	to	F	ECO # 2406
From	F	to	G	ECO # 2430

ADD: 7

SEE SEPARATE PARTS LIST

REV	DASH	DESCRIPTION	REMARKS
A	-803	PCBA, MPCP	SAME AS -703 EXCEPT LOCS. CA01, BK01, & BF01.
B	-303	PCBA, MPCP	SAME AS -303 EXCEPT COMPONENTS BF01, BA01 & CA01
B	-303	PCBA, MPCP	(SHOWN - REF.)

A

CONFIDENTIAL DOCUMENT
REPRODUCTION AND/OR DISCLOSURE OF THE INFORMATION CONTAINED HEREIN IS STRICTLY PROHIBITED WITHOUT PRIOR WRITTEN AUTHORIZATION OF AMPERIF CORP

amperif

PCB ASSEMBLY:
MPCP MULTIWIRE BOARD

APPROVALS	DATE
DRAWN L.R.	3-87
CHECKED	

SCALE 1:1 | SIZE D | DRAWING NO 1120016 - TAE | REV C

803 A

CLASS CODE: 28
PCBA OUTSIDE

1120014-203 UPCODE: 3 REV: H PL, MPCP PCBA
MODEL:
ECO NO: 2430 2543
DATE OF LAST ECO: 1/20/89

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1120015-003	MPCP,MW BD	3	C	1	1.000	1.000	EA	B	Y	N	1.000	0	0		00/00/00	99/99/99
1602180-201	PROM ASSY,MPC OP SYS	3	B	62	1.000	1.000	EA	B	Y	N	1.000	0	0	CA01	11/18/88	*11/18/88
1602180-202	PROM ASSY,MPC OP SYS	3	A	63	1.000	1.000	EA	B	Y	N	1.000	0	0	BK01	11/18/88	*11/18/88
1602180-203	PROM ASSY,MPC OP SYS	3	A	64	1.000	1.000	EA	B	Y	N	1.000	0	0	BF01	11/18/88	*11/18/88
1602180-301	PROM ASSY,MPCP OP SYS	3	B	62	1.000	1.000	EA	B	Y	N	1.000	0	0	CA01	00/00/00	99/99/99
1602180-302	PROM ASSY,MPCP OP SYS	3	A	63	1.000	1.000	EA	B	Y	N	1.000	0	0	BK01	00/00/00	99/99/99
1602180-303	PROM ASSY,MPCP OP SYS	3	A	64	1.000	1.000	EA	B	Y	N	1.000	0	0	BF01	00/00/00	99/99/99
20000700	IC,INV,HEX,SCHMITT,7414	3	A	29	1.000	1.000	EA	P	Y	N	1.000	0	0	AC28	00/00/00	99/99/99
20000250	DELETE! IC,BUFR,QUAD,3ST.74125	3	A	2	1.000	1.000	EA	P	Y	N	1.000	0	0	DF34	00/00/00	99/99/99
20005200	IC,NAND,TRI-3,S10	3	A	3	1.000	1.000	EA	P	Y	N	1.000	0	0	CM09	00/00/00	99/99/99
20005700	IC,NAND,QUAD-2,S37	3	A	52	1.000	1.000	EA	P	Y	N	1.000	0	0	CM01	00/00/00	99/99/99
20005900	IC,F/F,DUAL-D,S74	3	A	4	1.000	1.000	EA	P	Y	N	1.000	0	0	AH56	00/00/00	99/99/99
20006100	IC,XOR,QUAD-2,S86	3	A	5	1.000	1.000	EA	P	Y	N	1.000	0	0	DF43	00/00/00	99/99/99
20006600	IC,DEMUX,2TO4,S139	3	A	6	1.000	1.000	EA	P	Y	N	1.000	0	0	BB43	00/00/00	99/99/99
20007000	IC,MUX,QUAD,1OF2,S157	3	A	7	3.000	1.000	EA	P	Y	N	3.000	0	0	AC10,HA12 CH23	00/00/00	99/99/99
20008A00	IC,GEN,PRTY,9BIT,S280	3	A	9	1.000	1.000	EA	P	Y	N	1.000	0	0	DF26	00/00/00	99/99/99
20012100	IC,M-PROC,4BIT,SLICE,2901	3	A	10	2.000	1.000	EA	P	Y	N	2.000	0	0	CA14,CA35	00/00/00	99/99/99
20014300	RES,DIP,16P,470OHM,COM	3	A	11	4.000	1.000	EA	P	Y	N	4.000	0	0	AE52,AK10 CH14,CK49	00/00/00	99/99/99
20014A00	IC,DIP,16P,330/390,TERM	3	A	12	2.000	1.000	EA	P	Y	N	2.000	0	0	AC01,AK01	00/00/00	99/99/99
20015100	RES,DIP,14P,470OHM,COM	3	A	13	1.000	1.000	EA	P	Y	N	1.000	0	0	CM49	00/00/00	99/99/99
20018402-003	CAP,CE,RAD,.1UF,50V,20%	3	A	14	30.000	1.000	EA	P	Y	N	30.000	0	0	C2-C36	00/00/00	99/99/99
20018902	CAP,TANT,RAD,10UF,20%,16V	3	A	15	6.000	1.000	EA	P	Y	N	6.000	0	0	C1-C5 C6(AC39)	00/00/00	99/99/99
20019503	SKT,DIP,14P,PCMT	3	A	16	1.000	1.000	EA	P	Y	N	1.000	0	0	XCK01	00/00/00	99/99/99
20019803	SKT,DIP,24P,PCMT	3	A	17	3.000	1.000	EA	P	Y	N	3.000	0	0	XBF01 XBK01 XCA01	00/00/00	99/99/99
20041216	RES,CARB,1K,1/4W,5%	3	A	53	1.000	1.000	EA	P	Y	N	1.000	0	0	R1(AC36)	00/00/00	99/99/99
20042816	RES,CARB,4.7K,1/4W,5%	3	A	18	1.000	1.000	EA	P	Y	N	1.000	0	0	R2(CH13)	00/00/00	99/99/99
20058400	IC,LATCH,8BIT,LS259	3	A	20	5.000	1.000	EA	P	Y	N	5.000	0	0	AA19,AE19 AH10,AH19 AM10	00/00/00	99/99/99
20066899	IC,NAND,QUAD-2,ALS00	3	A	21	2.000	1.000	EA	P	Y	N	2.000	0	0	AK36,BD45	00/00/00	99/99/99
20067099	IC,INV,HEX,ALS04	3	A	22	3.000	1.000	EA	P	Y	N	3.000	0	0	AM28,BB52 CM17	00/00/00	99/99/99
20067199	IC,AND,QUAD-2,ALS08	3	A	23	4.000	1.000	EA	P	Y	N	4.000	0	0	AE36,AK28 BD53,DF18	00/00/00	99/99/99
20067299	IC,NAND,TRI-3,ALS10	3	A	24	1.000	1.000	EA	P	Y	N	1.000	0	0	AM36	00/00/00	99/99/99
20067399	IC,AND,TRI-3,ALS11	3	A	25	1.000	1.000	EA	P	Y	N	1.000	0	0	AC52	00/00/00	99/99/99

ECO # 2543

SHT 1 of 22

AS OF ACL DATE

803 A

CLASS CODE: 28
PCBA OUTSIDE

112100[illegible]-203 TYPECODE: 3 REV: B PL, MPCP PCBA
MODEL:
ECO NO: 2431
DATE OF LAST ECO: 1/20/89

2543

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20067499	IC,NAND,DUAL-4,ALS20	3	A	26	1.000	1.000	EA	P	Y	N	1.000	0	0	AK53	00/00/00	99/99/99
20067599	IC,AND,DUAL-4,ALS21	3	A	27	1.000	1.000	EA	P	Y	N	1.000	0	0	BB01	00/00/00	99/99/99
20067899	IC,OR,QUAD-2,ALS32	3	A	28	5.000	1.000	EA	P	Y	N	5.000	0	0	AA28,AA36 AE28,AH28 DF10	00/00/00	99/99/99
20068099	IC,F/F,DUAL-D,ALS74	3	A	30	3.000	1.000	EA	P	Y	N	3.000	0	0	AA44,AA52 AE44	00/00/00	99/99/99
20068199	IC,F/F,DUAL-JK,ALS112	3	A	31	2.000	1.000	EA	P	Y	N	2.000	0	0	AK19,DF01	00/00/00	99/99/99
20068299	IC,DEMUX,3TO8,ALS138	3	A	32	9.000	1.000	EA	P	Y	N	9.000	0	0	AA01,AA10 AE01,AE10 AH01,AM19 BB34,CM38 DD43	00/00/00	99/99/99
20068799	IC,F/F,HEX-D,ALS174	3	A	33	1.000	1.000	EA	P	Y	N	1.000	0	0	AK44	00/00/00	99/99/99
20068800	IC,DRVR,OCTAL,3ST,ALS244	3	A	34	5.000	1.000	EA	P	Y	N	5.000	0	0	BB23,BD34 CK27,CK38 DD23	00/00/00	99/99/99
20068999	IC,MUX,10F8,3ST,ALS251	3	A	35	2.000	1.000	EA	P	Y	N	2.000	0	0	AH47,AM53	00/00/00	99/99/99
20069099	IC,MUX,QUAD,10F2,3ST,ALS257	3	A	36	1.000	1.000	EA	P	Y	N	1.000	0	0	CH43	00/00/00	99/99/99
20069199	IC,DRVR,OCTAL,3ST,ALS465	3	A	37	1.000	1.000	EA	P	Y	N	1.000	0	0	CM27	00/00/00	99/99/99
20069699	IC,F/F,OCTAL-D,3ST,ALS574	3	A	38	3.000	1.000	EA	P	Y	N	3.000	0	0	BD01,BD12 BD23	00/00/00	99/99/99
20069799	IC,F/F,OCTAL-D,3ST,ALS576	3	A	39	2.000	1.000	EA	P	Y	N	2.000	0	0	CE35,DD01	00/00/00	99/99/99
20069899	IC,XCVR,OCTAL,3ST,ALS620	3	A	40	1.000	1.000	EA	P	Y	N	1.000	0	0	DD12	00/00/00	99/99/99
20070099	IC,GEN,LOOK-AHEAD,S182	3	A	41	1.000	1.000	EA	P	Y	N	1.000	0	0	DD34	00/00/00	99/99/99
20071399	IC,CNTLR,M-PROG,12BIT,2910A	3	A	42	1.000	1.000	EA	P	Y	N	1.000	0	0	CD01	00/00/00	99/99/99
20071499	IC,RGSTR,QUAD-D,3ST,2918	3	A	43	1.000	1.000	EA	P	Y	N	1.000	0	0	CH34	00/00/00	99/99/99
20071599	IC,GEN,CLK,CNTLR,2925	3	A	44	1.000	1.000	EA	P	Y	N	1.000	0	0	CH01	00/00/00	99/99/99
20072199	OSC,40MHZ,14P,DIP	3	A	46	1.000	1.000	EA	P	Y	N	1.000	0	0	CK01	00/00/00	99/99/99
20084211	SW,TOG,SPDT,R/A,PCMT	3	A	47	1.000	1.000	EA	P	Y	N	1.000	0	0	SW1(BD65)	00/00/00	99/99/99
20084314	LED,R/A,RED,PCMT,.3",W/RES	3	A	48	1.000	1.000	EA	P	Y	N	1.000	0	0	L6(CK62)	00/00/00	99/99/99
20084414	LED,R/A,GRN,PCMT,.3",W/RES	3	A	49	1.000	1.000	EA	P	Y	N	1.000	0	0	L5(CJ62)	00/00/00	99/99/99
20084514	LED,R/A,YEL,PCMT,.3",W/RES	3	A	50	4.000	1.000	EA	P	Y	N	4.000	0	0	L1(CL62) L2(DA62) L3(DE62) L4(AK62)	00/00/00	99/99/99
20091008	CONN,DIN,96P,MALE,RA,.180,LEAD	3	A	51	3.000	1.000	EA	P	Y	N	3.000	0	0	PJ1,PJ2 PJ3	00/00/00	99/99/99
20094208	CONN,HDR,2X20,MALE,R/A,SHRD	3	A	55	2.000	1.000	EA	P	Y	N	2.000	0	0	XJ4,XT5	00/00/00	99/99/99
20098499	IC,INV,OCT,3ST,LS240	3	A	56	1.000	1.000	EA	P	Y	N	1.000	0	0	AH36	00/00/00	99/99/99
20102213	EXTR,CARD,W/T LOCK	3	A	54	2.000	1.000	EA	P	Y	N	2.000	0	0		00/00/00	99/99/99

ECO # 2543

SHT 17 of 2

803

A

CLASS CODE: 28
PCBA OUTSIDE

112001A-203 UPCODE: 3 REV: B PL, MPCP PCBA
MODEL:
ECO NO: 2431
DATE OF LAST ECO: 1/20/89

2543

NEW

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

ECO #2543

PART NUMBER	DESCRIPTION	OP	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20119513-002	SCREW,PNHPH,2-56X1/2	3	A	59	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20121713-001	NUT,HEX,PLAIN,2-56	3	A	60	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20122113-001	WSHR,SPLK,#2	3	A	61	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20125611-001	SW,PB,SPDT,R/A,PCMT	1	A	58	1.000	1.000	EA	P	Y	N	1.000	0	0	SW3(AM65)	00/00/00	99/99/99
20136900-001	IC,CNTR,BIN,F163	3	A	8	2.000	1.000	EA	P	Y	N	2.000	0	0	CK09,CK18	00/00/00	99/99/99
20143800-001	IC,DEMUX,3TO8,LS138	3	A	65	1.000	1.000	EA	P	Y	N	1.000	0	0	AM01	00/00/00	99/99/99

1602314-101	PROM ASSY, MPC OP SYS	62	1.000		1.000	CA01
1602314-102	PROM ASSY, MPC OP SYS	63	1.000		1.000	BK01
1602314-103	PROM ASSY, MPC OP SYS	64	1.000		1.000	BF01

ADD:

SHT 18 OF 22

SHT 19
OF 22

ECO # 2543

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
K	INC ECO # 2430		
L	INC ECO # 2543		

ADD: A

ADD: A

CB ASSY & ARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK (MULTIWIRE)	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1120016-803	A	1120016-303	B	0120015-003	B	0120015-003	A	4	–	PROM CHG CREATE -803	2543
1120016-802	A	1120016-302	C	0120015-002	D	0120015-002	B	4	–	PROM CHG CREATE -802	2543
1120016-801	A	1120016-201	F	0120015	E	0120015	B	4	–	PROM CHG CREATE -801	2543
1120016-703	B	1120016-303	B	0120015-003	B	0120015-003	A	4	–	PROM CHG	2430
1120016-702	B	1120016-302	C	0120015-002	D	0120015-002	B	4	–	PROM CHG	2430
1120016-701	B	1120016-201	F	0120015-	E	0120015	B	4	–	PROM CHG	2430
1120016-703	A	1120016-303	B	0120015-003	B	0120015-003	A	4	–	PROM CHG CREATE -701	2420
1120016-702	A	1120016-302	C	0120015-002	D	0120015-002	B	4	–	PROM CHG CREATE -702	2420
1120016-701	A	1120016-201	F	0120015	E	0120015	B	4	–	PROM CHG CREATE -703	2420

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD/ ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

FORM 105-1-78

NEXT ASSY

USED ON

DR BY

CHK BY

APPROVED BY

FROM: K
TO: L

CONFIGURATION LIST PCBA:
MPCP (MULTIWIRE)

SIZE A

DWG NO. 1120016-TAB

REV K

SCALE —

SHEET 6 OF 6

11.2BU.1.DATABA01 AMPERIF CORPORATION DISTRIBUTION: CHERYLL - ENG SERVICES
DATE, FEB 1989 BILL OF MATERIAL PAGE NO: 1
AS OF ALT DATE

CLASS CODE: 42
LARGE MECHANICAL ASSEMBLY

FROM: L
TO: M

1602759-001 OPTION: 3 REV: L 9200 DISK CONTROLLER CARD KIT
MODEL:
ECO NO: 2530
DATE OF LAST ECO: 2/21/89

FROM: 2530 TO: 2543

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	OP	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1601164	COVER PANEL CTLR CC	3	E	4	1.000	1.000	EA	B	Y	N	1.000	0	0	00/01-01	00/00/00	99/99/99
0601437-001	COVER,CC DISK I/O	3	B	5	2.000	1.000	EA	B	Y	N	2.000	0	0	00/02-01 00/03-01	00/00/00	99/99/99
1601586-001	LABEL, GROUNDING STRAPS	3	A	17	3.000	1.000	EA	B	Y	N	3.000	0	0	00/04-01 00/05-02	00/00/00	99/99/99
1106012-401	PCBA,80X5 CPU (CHALLENGER II)	3	G	6	1.000	1.000	EA	S	Y	N	1.000	0	0	00/00-01	00/00/00	99/99/99
1106062-302	PCBA,XMCP	3	E	7	2.000	1.000	EA	S	Y	N	2.000	0	0	00/01-02	00/00/00*	9/01/88
1106095	AIU-A PCB ASSY	3	J	8	2.000	1.000	EA	S	Y	N	2.000	0	0	00/02-02	00/00/00	99/99/99
1120010-202	PCBA,XMCIP	3	C	9	2.000	1.000	EA	S	Y	N	2.000	0	0	00/01-02	00/00/00*	9/01/88
1120010-302	PCBA,XMCIP	3	C	9	2.000	1.000	EA	S	Y	N	2.000	0	0		9/01/88*	11/18/88
1120010-402	PCBA,XMCIP	3	A	9	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-401	11/18/88	99/99/99
1120014-202	PCBA,MDBP	3	L	10	2.000	1.000	EA	S	Y	N	2.000	0	0	00/01-02	00/00/00*	2/22/89
1120014-302	MDBP PCBA	3	A	10	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT. -301	2/22/89	99/99/99
1120016-201	MPCP MULTIWIRE BOARD ASSEMBLY	3	J	11	2.000	1.000	EA	S	Y	N	2.000	0	0	00/01-02	00/00/00*	9/01/88
1120016-503	PCBA,MPCP	3	B	11	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT. P/N -502/-501	9/01/88*	12/09/88
1120016-603	PCBA.MPCP	3	H	11	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT.P/N -602/-601	12/09/88*	12/19/88
1120016-703	PL, MPCP PCBA	3	B	11	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT P/N -702/-701	12/19/88	99/99/99
1601115	DISK I/O CC ASSY	3	P	2	1.000	1.000	EA	M	Y	N	1.000	0	0		00/00/00*	9/01/88
1601116-002	SIERRA CTLR CARD CAGE ASSEMBLY	3	AG	1	1.000	1.000	EA	M	Y	N	1.000	0	0		00/00/00*	7/06/88
1601116-003	3MB CONTROLLER CARD CAGE ASSY	3	E	1	1.000	1.000	EA	M	Y	N	1.000	0	0		7/06/88*	9/01/88
1601116-005	3MB CNTLR CARD CAGE ASSY.	3	B	1	1.000	1.000	EA	M	Y	N	1.000	0	0		9/01/88	99/99/99
1601138-103	PCBA,AIX	3	F	12	2.000	1.000	EA	S	Y	N	2.000	0	0	00/02-02	00/00/00	99/99/99
1601141	EXPANSION CARD CAGE ASSEMBLY	3	G	3	1.000	1.000	EA	M	Y	N	1.000	0	0		00/00/00*	7/13/88
1601494-202	PCBA,XM16KP	3	B	13	2.000	1.000	EA	S	Y	N	2.000	0	0	00/01-02	00/00/00	99/99/99
1601495-701	PCBA,PROM BD-XM16KP	3	G	14	2.000	1.000	EA	S	Y	N	2.000	0	0	00/13-02	00/00/00*	9/01/88
1601495-951	PCBA, PROM BD., XM16KP-D	3	A	14	2.000	1.000	EA	S	Y	N	2.000	0	0		9/01/88*	12/09/88
1601495-951	PCBA,PROM BD-XM16KPD	3	B	14	2.000	1.000	EA	S	Y	N	2.000	0	0		12/09/88	99/99/99
1601715-101	PCBA ASSY,BIX-E	3	C	15	2.000	1.000	EA	S	Y	N	2.000	0	0	00/02-02	00/00/00	99/99/99
1601716-202	PCBA,DIFE	3	D	16	2.000	1.000	EA	S	Y	N	2.000	0	0	00/01-02	00/00/00*	7/15/88
1601716-402	PCBA.DIFE	3	A	16	2.000	1.000	EA	S	Y	N	2.000	0	0		7/15/88*	11/18/88
1601716-502	PCBA,DIFE	3	B	16	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT. P/N 1601716-501	11/18/88	99/99/99
1601909-101	PCBA EXXP	3	F	21	2.000	1.000	EA	S	Y	N	2.000	0	0	00/03-02	5/31/88	99/99/99
1601962-202	PCBA,XMC	3	E	7	2.000	1.000	EA	S	Y	N	2.000	0	0		9/01/88*	12/16/88
1601962-302	PCBA/PL,XMC	3	A	7	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-301	12/16/88	99/99/99
1602224-101	EXPANSION CARD CAGE ASSEMBLY	3	A	3	1.000	1.000	EA	M	Y	N	1.000	0	0		7/13/88	99/99/99
1602286-101	DISK I/O CARD CAGE ASSY	3	H	2	1.000	1.000	EA	M	Y	N	1.000	0	0		9/01/88	99/99/99

ECO #2543

SHT 2 OF 2

FROM: 703
TO: 803

FROM: -702/-701
TO: -802/-801

AS OF ALT. DATE

FROM: JK
TO: KL

CLASS CODE: 42
LARGE MECHANICAL ASSEMBLY

16112159-201 TYPECODE: 3 REV: A PCBA KIT,CONTROLLER
MODEL:
ECO NO: 2530
DATE OF ENG. RELEASED: 2/21/89

FROM: 2530 TO: 2543

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

ECO # 2543

PART NUMBER	DESCRIPTION	OP	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	REQ	PF	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1120010-302	PCBA,XMCIP	3	C	9	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	11/18/88
1120010-402	PCBA,XMCIP	3	A	9	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-401	11/18/88	99/99/99
1120014-202	PCBA,MDBP	3	L	10	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	2/22/89
1120014-302	MDBP PCBA	3	A	10	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT. -301	2/22/89	99/99/99
1120016-503	PCBA,MPCP	3	B	11	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	12/09/88
1120016-603	PCBA,MPCP	3	B	11	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT.P/N -602/-601	12/09/88	12/19/88
1120016-703	PL, MPCP PCBA	3	B	11	2.000	1.000	EA	S	Y	N	2.000	0		ALT P/N -702/-701	12/19/88	99/99/99
1601494-202	PCBA,XM16KP	3	B	13	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	99/99/99
1601495-931	PCBA, PROM BD., XM16KP-D	3	A	14	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	12/09/88
1601495-951	PCBA,PROM BD-XM16KPD	3	B	14	2.000	1.000	EA	S	Y	N	2.000	0	0		12/09/88	99/99/99
1601716-402	PCBA,DIFE	3	A	16	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	11/18/88
1601716-502	PCBA,DIFE	3	B	16	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT P/N 1601716-501	11/18/88	99/99/99
1601962-202	PCBA,XMC	3	E	7	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	12/16/88
1601962-302	PCBA/PL,XMC	3	A	7	2.000	1.000	EA	S	Y	N	2.000	0	0	ALT-301	12/16/88	99/99/99
1602015-201	PCBA,SIOA	3	D	22	2.000	1.000	EA	S	Y	N	2.000	0	0		00/00/00	99/99/99

FROM: 703
TO: 803

FROM: -702/-701
TO: -802/-801

SHT 21 OF 22

FROM: M
TO: N

CLASS CODE: 9A
DOCUMENTATION ONLY !!

9200-1103-FRU UPCODE: 3 REV M 9200-1103 DUAL ENTRIER FRU LIST
MODEL:
ECO NO: 2530
DATE OF LAST ECO: 2/21/89

FROM: 2530 TO: 2543

ECO # 2543

UP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	O P	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SC	R E Q	P F	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
1106010-103	PCBA,LED-CHALLENGER II	3	B	19	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1106011	PCB ASSY,KEYBOARD	3	B	20	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1106012-401	PCBA,80H5 CPU (CHALLENGER II)	3	G	9	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1120010-302	PCBA,XMCIP	3	C	4	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	11/18/88
1120010-402	PCBA,XMCIP	3	A	4	.000	1.000	EA	S	Y	N	.000	0	0	ALT-401	11/18/88	99/99/99
1120014-202	PCBA,MDBP	3	L	5	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	2/22/89
1120014-302	MDBP PCBA	3	A	5	.000	1.000	EA	S	Y	N	.000	0	0	ALT. -301	2/22/89	99/99/99
1120016-503	PCBA,MPCP	3	B	6	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	12/09/88
1120016-603	PCBA,MPCP	3	B	6	.000	1.000	EA	S	Y	N	.000	0	0	ALT.P/N -602/-601	12/09/88	12/19/88
1120016-703	PL, MPCP PCBA	3	B	6	.000	1.000	EA	S	Y	N	.000	0	0	ALT P/N -702/-701	12/19/88	99/99/99
1601494-202	PCBA,XM16KP	3	B	2	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1601495-931	PCBA, PROM BD., XM16KP-D	3	A	1	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	12/09/88
1601495-951	PCBA,PROM BD-XM16KPD	3	B	1	.000	1.000	EA	S	Y	N	.000	0	0		12/09/88	99/99/99
1601716-402	PCBA,DIFE	3	A	7	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	11/18/88
1601716-502	PCBA,DIFE	3	B	7	.000	1.000	EA	S	Y	N	.000	0	0	ALT-501	11/18/88	99/99/99
1601840-101	BACKPLANE,3370 CC	3	B	15	.000	1.000	EA	B	Y	N	.000	0	0		00/00/00	11/11/88
1601840-201	PCBA BACKPLANE UNIVERSAL I/O	3	E	15	.000	1.000	EA	B	Y	N	.000	0	0		11/11/88	99/99/99
1601962-202	PCBA,XMC	3	E	3	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	12/16/88
1601962-302	PCBA/PL,XMC	3	A	3	.000	1.000	EA	S	Y	N	.000	0	0	ALT-301	12/16/88	99/99/99
1602003-202	PCBA,DCP	3	B	8	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	11/11/88
1602003-302	PCBA,DCP & P/L	3	A	8	.000	1.000	EA	S	Y	N	.000	0	0		11/11/88	99/99/99
1602015-201	PCBA,SIOA	3	D	10	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
1602209-101	PCBA CTLR LOGIC B/P 3MB	3	D	14	.000	1.000	EA	B	Y	N	.000	0	0		00/00/00	99/99/99
1602276-202	EXBP-DS BACKPLANE	3	C	16	.000	1.000	EA	B	Y	N	.000	0	0		00/00/00	12/02/88
1602276-203	PCBA,EXBP-DS	3	H	16	.000	1.000	EA	B	Y	N	.000	0	0		12/02/88	99/99/99
1602331-101	OPERATOR CNTRL PANEL ASSY	3	B	17	.000	1.000	EA	M	Y	N	.000	0	0		00/00/00	99/99/99
1602333-303	PCBA,CHNL ENABLE/DISABLE	3	B	11	.000	1.000	EA	S	Y	N	.000	0	0		00/00/00	99/99/99
20055612	DISP,40CHAR,5X7DOT,VF	3	A	18	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20105213	FAN,4.5",230VAC	3	A	21	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20105313	FAN,6",230VAC	3	A	22	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20109011	CKT BKR,DPST,5A,230VAC	3	A	25	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20109411	CKT BKR,DPST,3A,230VAC	3	A	24	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20110911	P/S,-5V,13A,EXP,CAB	3	A	13	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20114801	P/S,+5,70A,400W	1	A	12	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20148813-002	FAN,6.5",230VAC,1.5"THK	3	A	23	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99
20172811-001	CKT BRKR,DPST,1PH,30A,208V	3	A	26	.000	1.000	EA	P	Y	N	.000	0	0		00/00/00	99/99/99

FROM: 703
TO: 803

FROM: -702/-701
TO: -802/-801

SHT 22 OF 22

amperif corporation

ENGINEERING CHANGE REQUEST/ORDER

ECR ☑ ECO ☒

ECR/ECO NO. 2440

PROJ. TITLE	HDW	SFTWR	IAI	CHANGE LAL:	CHANGE CLASS A B C D	FIELD	AMENDMENTS
9200/L.F.	☑	☐	☐	YES ☑ NO ☐	☑ ☐ ☐ ☐	☑ YES ☐ NO	

REQSTR/DRAWN: L. RIVERA
DATE: 1-16-89

CHECKED BY: [signature]
DATE: 16 Jan 89

REASON FOR CHANGE

☐ DWG CORRECTION ☐ PURCHASE PROBLEM ☐ COST REDUCTION ☐ CUSTOMER REQUEST

☐ PRODUCT IMPROVEMENT ☐ PRODUCTION PROBLEM ☑ DESIGN ERROR ☐ OTHER

EXPLAIN REASON FOR CHANGE: AT HIGH MARGIN CLOCK DRIVER COULD NOT DRIVE LOAD CAUSING ECC UNCORRECT AND CORRECTABLE DATA HITS.

COST IMPACT	CHANGE COST EVALUATION ☐ YES ☐ NO ☐ ATTACHED	EST'D BY

ENGR DISPOSITION OF ECR: APPROVED ☐ YES ☐ NO

EXPLAIN REASON FOR REJECTION _____

PROJ. ENG. PROJ. MGR. DATE

CHANGE AGAINST DWG NO.	CHANGE AGAINST PART NO	REVISION FROM	REVISION TO	DRAWING TITLE
1601716-501	1601716-501	A	B	PCBA, P/L / DIFE
1601716-502	1601716-502	A	B	PCBA, P/L / DIFE
1601716-502	—	A	B	SCHEMATIC: DIFE
1601716	—	J	K	CONFIGURATION LIST

CHANGE U86 74F00 PIN 20145200-001 TO: 74F37 PIN 20154400-001

INCORPORATION/DISPOSITION

	USE	REWORK	SCRAP	NOTE:
IN FIELD	☐	☒	☐	FCO 9200-002
FIELD SPARES	☐	☒	☐	
FINISHED GOODS	☐	☒	☐	
FINAL ASSY	☐	☒	☐	
IN TEST	☐	☒	☐	
IN PROCESS	☐	☒	☐	
IN STOCK	☐	☒	☐	
NEXT ASSY	☐	☒	☐	
ON ORDER	☐	☒	☐	
NEXT BUY	☐	☒	☐	
OTHER	☐	☐	☐	

INCORP. OF CHANGE DATE 1-17-89 SERIAL NO. 207

SPECIAL INSTRUCTION:

CCB APPROVAL AND RESPONSIBILITY

ENGINEERING	[signature]	1-16-89
SFTWR		
MARKETING	[signature]	1-17-89
MFG. ENG.	[signature]	1-16-89
QUALITY	A. Fuerzi	1-17-89
SERVICE	B. Bujl	1/16/89
ENG. SERV.	[signature]	1/17/89
DIR. OF ENG.		

[illegible] DATAHALL AMPERIF CORPORATION

[illegible] 3.

BILL OF MATERIAL

AS OF 1/03/89

PAGE NO: 3

[illegible]: B

PCBA OUTSIDE

OPTION: 3 REV: A PCBA,DIFF

MODEL:

[illegible]: 2440

DATE OF LAST ECO: 11/15/88

UP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	U P	RV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SL	R E Q	P F	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
[illegible]	IC,DRVR,OCTAL,3ST,LS367	3	A	46	3.000	1.000	EA	P	Y	N	3.000	0	0	U16,U93 U102	00/00/00	99/99/99
[illegible]	IC,CNTR,BIN,SYNC,AS869	3	A	47	3.000	1.000	EA	P	Y	N	3.000	0	0	U115,U124 U150	00/00/00	99/99/99
[illegible]	IC,RAM,DUAL,16X4,CMOS	3	A	48	2.000	1.000	EA	P	Y	N	.000	0	0	U84,U103	00/00/00	99/99/99
20071999	IC,PROC,BURST-ERROR,9521-1	3	A	49	1.000	1.000	EA	P	Y	N	1.000	0	0	U74	00/00/00	99/99/99
[illegible]	IC,CNTR,4BIT,ALS169	3	A	50	2.000	1.000	EA	P	Y	N	2.000	0	0	U80,U108	00/00/00	99/99/99
20083999	IC,F/F,4BIT,DUAL-D,3ST,ALS876	3	A	51	1.000	1.000	EA	P	Y	N	1.000	0	0	U1	00/00/00	99/99/99
[illegible]	CONN,DIN,96P,MALE,RA,.100,LEAD	3	A	52	3.000	1.000	EA	P	Y	N	3.000	0	0	P11-P13	00/00/00	99/99/99
20094208	CONN,HDR,2X20,MALE,R/A,SHRD	3	A	53	2.000	1.000	EA	P	Y	N	2.000	0	0	XJ4,XJ5	00/00/00	99/99/99
[illegible]	RES,SIP,10P,2K OHM,COM	3	A	88	2.000	1.000	EA	P	Y	N	2.000	0	0	RP15,RP13	00/00/00	99/99/99
20096699	RES,SIP,10P,160OHM,COM	3	A	87	2.000	1.000	EA	P	Y	N	2.000	0	0	RP14,RP17	00/00/00	99/99/99
[illegible]	IC,NAND,QUAD-2,SCHMITT,ST132	3	A	54	1.000	1.000	EA	P	Y	N	1.000	0	0	U69	00/00/00	99/99/99
20102213	EXTR,CARD,W/O LOCK	3	A	75	2.000	1.000	EA	P	Y	N	2.000	0	0		00/00/00	99/99/99
[illegible]	SCREW,PNHPH,2-56X1/2	3	A	76	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20121713-001	NUT,HEX,PLAIN,2-56	3	A	77	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
[illegible]	WSHR,STAR,INT,#2,TYPE	3	A	78	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20129100-001	IC, RCVR,TRI,ECL,DIP	3		57	1.000	1.000	EA	P	Y	N	1.000	0	0	U45	00/00/00	99/99/99
[illegible]	IC, DRVR,QUAD,ECL,DIP	3		60	1.000	1.000	EA	P	Y	N	1.000	0	0	U78	00/00/00	99/99/99
20132308-001	RES,SIP,8P,220HM,ISO	3	A	85	1.000	1.000	EA	P	Y	N	1.000	0	0	RP10	00/00/00	99/99/99
[illegible]	JUMPER,WIRE,.1"	3	A	0	10.000	1.000	EA	F	Y	N	10.000	0	0	JPA1-1-2 JPA2-1-2 JPA3-1-2 JPA4-1-2 JPA5-2-3 JPA6-2-3 JPB1-1-2 JPB2-1-2 JPB3-1-3 JPB4-1-2	00/00/00	99/99/99
[illegible]	IC,CNTR,BIN,F163	3	A	64	1.000	1.000	EA	P	Y	N	1.000	0	0	U117	00/00/00	99/99/99
20138400-001	IC,DELAY,5NS/TAP,ACTIVE	3	A	55	1.000	1.000	EA	P	Y	N	1.000	0	0	U68	00/00/00	99/99/99
[illegible]	IC,AND,QUAD-2,AS08	3	A	0	1.000	1.000	EA	P	Y	N	1.000	0	0	U67	00/00/00	99/99/99
20138800-001	IC,74F112,FF,DUAL-JK	3	A	63	2.000	1.000	EA	P	Y	N	2.000	0	0	U31,U109	00/00/00	99/99/99
[illegible]	IC,NOR,QUAD-2,AS32	3	A	68	1.000	1.000	EA	P	Y	N	1.000	0	0	U78	00/00/00	99/99/99
20139000-001	IC,F/F,OCTAL-D,3ST,AS574	3	A	90	2.000	1.000	EA	P	Y	N	2.000	0	0	U76,U121	00/00/00	99/99/99
[illegible]	RES,SIP,8P,56 OHM,ISO	3	A	0	2.000	1.000	EA	P	Y	N	2.000	0	0	RP9,RP11	00/00/00	99/99/99
20144316-001	RES,SIP,8P,100OHM,ISO	3	A	86	2.000	1.000	EA	P	Y	N	2.000	0	0	RP8,RP12	00/00/00	99/99/99
[illegible]	IC,REGSTR,8BIT,F299	3	A	70	2.000	1.000	EA	P	Y	N	2.000	0	0	U52,U65	00/00/00	99/99/99
20145200-001	IC,NAND,QUAD-2,F00	3	A	69	12.000	1.000	EA	P	Y	N	12.000	0	0	U88,U129	00/00/00	99/99/99
[illegible]	IC,NOR,QUAD-2,F02	3	A	71	1.000	1.000	EA	P	Y	N	1.000	0	0	U30	00/00/00	99/99/99

1 - DELETE

[illegible] IC, 74FS7 1.000 1.000 U86

ADD

ECO 2440
SHT 2 OF 3

CLASS CODE: [illegible]
PCBA OUTSIDE

[illegible] OPTION: 3 REV: A PCBA,DIFF

MODEL:
ECO NO: 2440
DATE OF LAST ECO: 11/15/88

OP: ORDER POLICY CODE
REQ: Y=PART REQUIRED
N=PART OPTIONAL
PF: Y=PART PRINTS ON SALES ORDER
N=PART DOES NOT PRINT ON SO

PART NUMBER	DESCRIPTION	O P	REV	ITEM NO.	QTY PER ASSEMBLY	YIELD FACTR	UM	SE	REQ	P F	DEFAULT QUANTITY	DAYS OFF SET	SEQ	REFERENCE DESIGNATOR	EFFECTIV DATE	OBSOLETE DATE
20002599	IC,DRVR,OCTAL,3ST,LS467	3	A	46	3.000	1.000	EA	P	Y	N	3.000	0	0	U16,U93 U102	00/00/00	99/99/99
20003999	IC,CNTR,BIN,SYNC,ASH69	3	A	47	3.000	1.000	EA	P	Y	N	3.000	0	0	U115,U124 U130	00/00/00	99/99/99
20021899	IC,RAM,DUAL,16X4,29202	3	A	48	2.000	1.000	EA	P	Y	N	.000	0	0	U84,U103	00/00/00	99/99/99
20021999	IC,PROC,BURST-ERROR,9521-1	3	A	49	1.000	1.000	EA	P	Y	N	1.000	0	0	U74	00/00/00	99/99/99
20083899	IC,CNTR,4BIT,ALS169	3	A	50	2.000	1.000	EA	P	Y	N	2.000	0	0	U80,U108	00/00/00	99/99/99
20083999	IC,F/F,4BIT,DUAL-D,3ST,ALS876	3	A	51	1.000	1.000	EA	P	Y	N	1.000	0	0	U1	00/00/00	99/99/99
20091008	CONN,DIN,96P,MALE,RA,.100,LEAD	3	A	52	3.000	1.000	EA	P	Y	N	3.000	0	0	PJ1-PJ3	00/00/00	99/99/99
20094208	CONN,HDR,2X20,MALE,R/A,SHRD	3	A	53	2.000	1.000	EA	P	Y	N	2.000	0	0	XJ4,XJ5	00/00/00	99/99/99
20096599	RES,SIP,10P,750 OHM,COM	3	A	88	2.000	1.000	EA	P	Y	N	2.000	0	0	RP15,RP13	00/00/00	99/99/99
20096699	RES,SIP,10P,1600HM,COM	3	A	87	2.000	1.000	EA	P	Y	N	2.000	0	0	RP14,RP17	00/00/00	99/99/99
20098699	IC,NAND,QUAD-2,SCHMITT,S132	3	A	54	1.000	1.000	EA	P	Y	N	1.000	0	0	U69	00/00/00	99/99/99
20102213	EXTR,CARD,W/O LOCK	3	A	75	2.000	1.000	EA	P	Y	N	2.000	0	0		00/00/00	99/99/99
20119513-002	SCREW,PNHPH,2-56X1/2	3	A	76	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20121713-001	NUT,HEX,PLAIN,2-56	3	A	77	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20122313-001	WSHR,STAR,INT,#2,CRES	3	A	78	6.000	1.000	EA	F	Y	N	6.000	0	0		00/00/00	99/99/99
20129100-001	IC, RCVR,TRI,ELL,DIP	3		57	1.000	1.000	EA	P	Y	N	1.000	0	0	U45	00/00/00	99/99/99
20129200-001	IC, DRVR,QUAD,ELL,DIP	3		60	1.000	1.000	EA	P	Y	N	1.000	0	0	U70	00/00/00	99/99/99
20132308-001	RES,SIP,8P,22OHM,ISO	3	A	85	1.000	1.000	EA	P	Y	N	1.000	0	0	RP10	00/00/00	99/99/99
20135513-001	JUMPER,WIRE,.1"	3	A	0	10.000	1.000	EA	F	Y	N	10.000	0	0	JPA1-1-2 JPA2-1-2 JPA3-1-2 JPA4-1-2 JPA5-2-3 JPA6-2-3 JPB1-1-2 JPB2-1-2 JPB3-1-3 JPB4-1-2	00/00/00	99/99/99
20136900-001	IC,CNTR,BIN,F163	3	A	64	1.000	1.000	EA	P	Y	N	1.000	0	0	U117	00/00/00	99/99/99
20138400-001	IC,DELAY,5NS/TAP,ACTIVE	3	A	55	1.000	1.000	EA	P	Y	N	1.000	0	0	U68	00/00/00	99/99/99
20138700-001	IC,AND,QUAD-2,AS08	3	A	11	1.000	1.000	EA	P	Y	N	1.000	0	0	U67	00/00/00	99/99/99
20138800-001	IC,74F112,FF,DUAL-JK	3	A	63	2.000	1.000	EA	P	Y	N	2.000	0	0	U31,U109	00/00/00	99/99/99
20138900-001	IC,OR,QUAD-2,AS32	3	A	68	1.000	1.000	EA	P	Y	N	1.000	0	0	U78	00/00/00	99/99/99
20139000-001	IC,F/F,OCTAL-D,3ST,AS574	3	A	90	2.000	1.000	EA	P	Y	N	2.000	0	0	U76,U121	00/00/00	99/99/99
20141616-101	RES,SIP,8P,56 OHM,ISO	3	A	11	2.000	1.000	EA	P	Y	N	2.000	0	0	RP9,RP11	00/00/00	99/99/99
20144316-001	RES,SIP,8P,100OHM,ISO	3	A	86	2.000	1.000	EA	P	Y	N	2.000	0	0	RP8,RP12	00/00/00	99/99/99
20144600-001	IC,REGSTR,8BIT,F299	3	A	70	2.000	1.000	EA	P	Y	N	2.000	0	0	U62,U65	00/00/00	99/99/99
20145200-001	IC,NAND,QUAD-2,F00	3	A	69	1.000	1.000	EA	P	Y	N	1.000	0	0	U86,U129	00/00/00	99/99/99
20145300-001	IC,NOR,QUAD-2,F02	3	A	71	1.000	1.000	EA	P	Y	N	1.000	0	0	U30	00/00/00	99/99/99

DELETE

20154400-001 IC, 74F37 1.000 1.000 U86

ADD

ECO 2440
SHT 3 OF 9

REMARKS:

ADD J

ECO 2290
SH 4 OF 9

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	FIRST RELEASE	6-87	L.R.
F	ECO 1857, 1765, 1763, 1584	13JUL88	ANC
G	ECO 1914 RM	7-NOV 88	[illegible]
H	UPDATE ECO 2259		
J	UPDATE ECO 2452		

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1601716-302	B/B	1601716-302	D	0601629-002	A	0601629-002	A	6	—	FROM CHANGE	1914
1601716-301	A/B	1601716-302	D	0601629-001	AX	0601629-001	A	6	—	FROM CHANGE	1914
1601716-401	A/B	1601716-402	A	0601629-001	AX	0601629-001	A	6	—	FROM CHANGE	1914
1601716-402	A/B	1601716-402	A	0601629-002	A	0601629-002	A	6	—	FROM CHANGE	1914
1601716-302	A	1601716-302	C	0601629-002	A	0601629-002	A	6	—	JMPR OPTION	1857
1601716-202	C	1601716-202	C	0601629-002	A	0601629-002	A	6	—	JMPR REWORK	1857
1601716-202	B	1601716-202	B	0601629-002	A	0601629-002	A	6	—	BOM UPDATE	1765
1601716-201	CX	1601716-201	CX	0601629-001	AX	0601629-001	A	6	—	PROM UPDATE	1763
1601716-201	BX	1601716-201	CX	0601629-001	AX	0601629-001	A	6	—	FROM UPDATE	1584
1601716-101	CX	1601716-101	BX	0601629-001	AX	0601629-001	A	6	—	FROM UPDATE	1584
[illegible]	AX	[illegible]	AX	0601629-001	AX	0601629-001	A	6	—	1564	10-14-87
[illegible]	BX	[illegible]	AX	0601629-001	AX	0601629-001	A	6	—	1553	9-23-87
[illegible]	A	[illegible]	AX	0601629-001	AX	0601629-001	A	6	—	1517	8-17-87
[illegible]	AX	[illegible]	AX	0601629-001	AX	0601629-001	A	6	—	PROTOTYPE	—

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

FORM 105-1-78

NEXT ASSY

USED ON CH. II/SIERRA

DR BY	L RIVERA	6-87
CHK BY		

APPROVED BY

CONFIGURATION LIST PCBA:

DIFE CHANGE

SIZE	DWG NO.	REV
A	1601716	AK

SCALE NONE SHEET 1 OF X2

REMARKS:

ECO 2440
SHT 5 OF 9

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

ADD

PCB ASSY & PARTS LIST	REV	SCHEMATIC	REV	P.C.B. FAB. DWG	REV	ARTWORK	REV	NO. LYR	NO. SHT	REMARKS	ECO/DATE
1601716 [illegible]	B	1601716 [illegible]	B	06 [illegible]	A	06 [illegible]	A	6		PC CHG	2440
1601716-501	B	1601716 [illegible]	B	0601629 001	AX	0601629 001	A	6	—	[illegible]	2440
1601716-502	A	1601716-502	A	0601629-002	A	0601629-002	A	6	—	REL SCH.	2452
1601716-501	A	1601716-502	A	0601629-001	AX	0601629-001	A	6	—	REL SCH.	2452
1601716-502	A	1601716-		0601629-002	A	0601629-002	A	6	—	PROM C116.	2259
1601716-501	A	1601716-		0601629-001	AX	0601629-001	A	6	—	PROM C116.	2259

NOTES: UNLESS OTHERWISE SPECIFIED.

1 — FABRICATE P.C. BOARD PER AMPERIF SPECIFICATION 1200001

2 — THIS DOCUMENT DEFINES THE LATEST ACCEPTABLE DOCUMENTATION LEVEL REQUIRED FOR PROCUREMENT OF PRINTED CIRCUIT BOARD ASSEMBLY. ANY DISCREPANCY OR DEVIATION SHOULD BE BROUGHT TO AMPERIF CORP. ATTENTION BEFORE FABRICATING THE CIRCUIT BOARD.

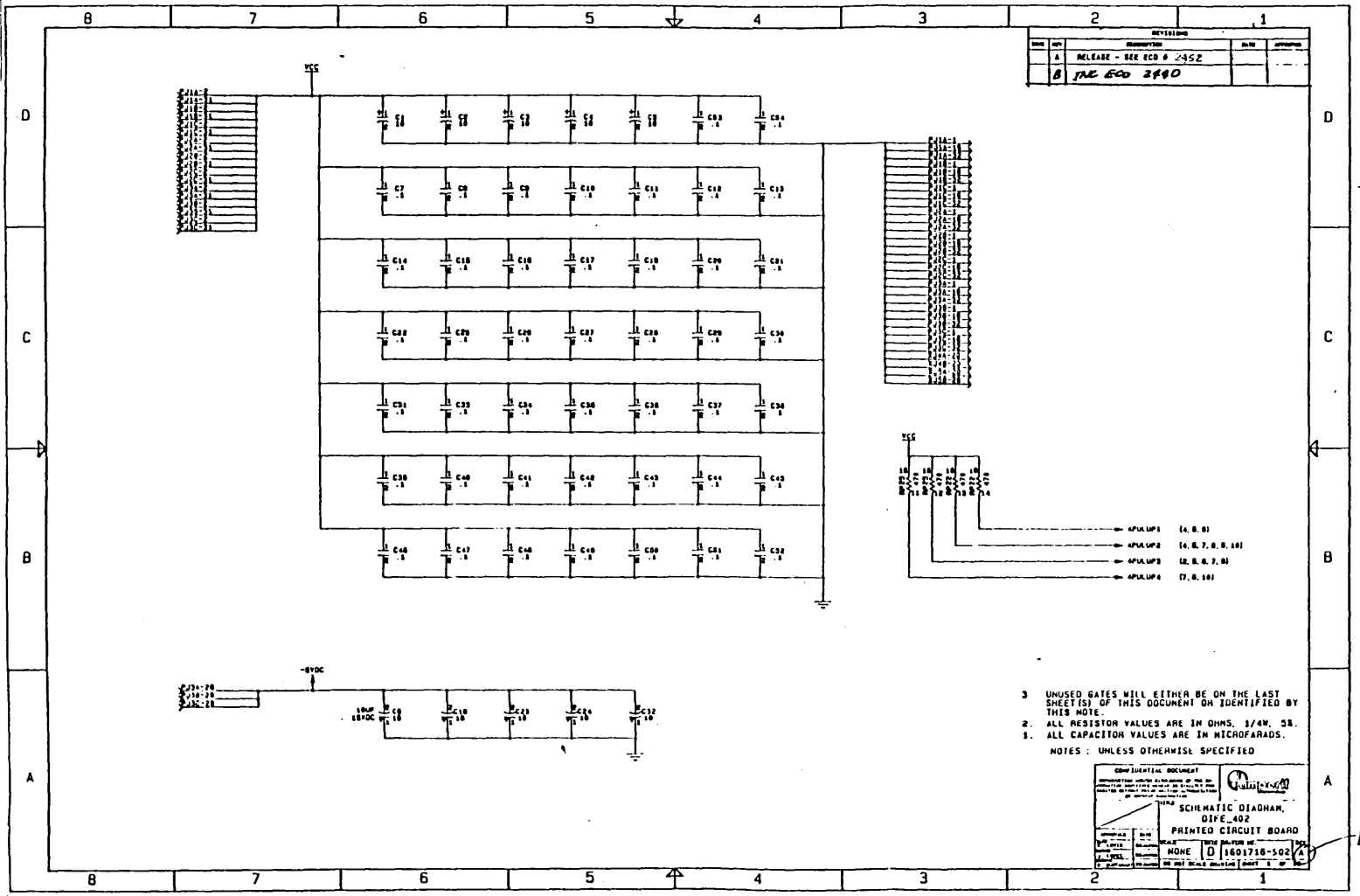
FORM 105-1-78

NEXT ASSY		
USED ON		
DR BY	L. RIVERA	1/3/89
CHK BY		
APPROVED BY		

CONFIGURATION LIST PCBA!

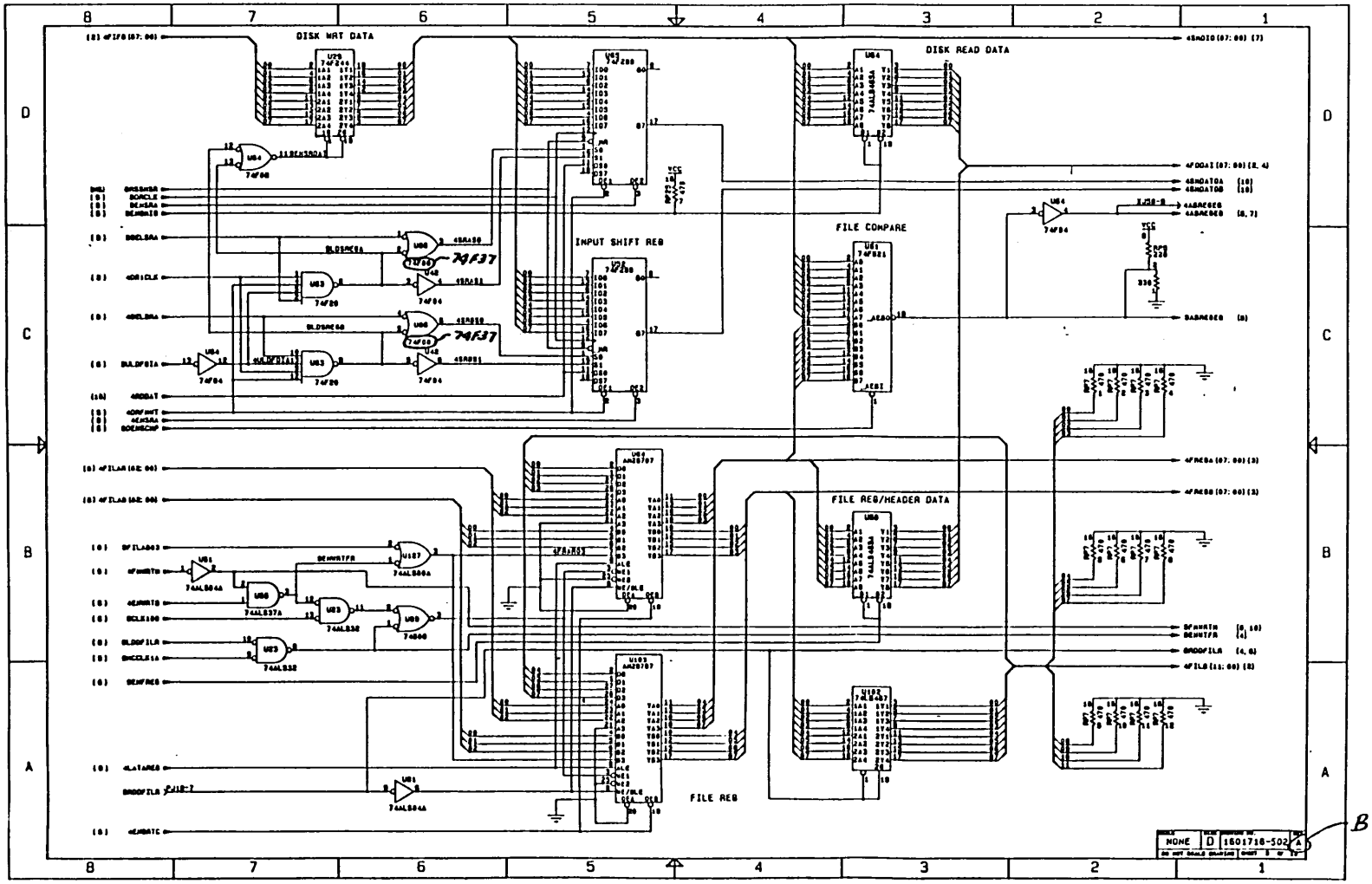
DIFE ADD

SIZE		DWG NO.	REV
A		1601716	F
SCALE NONO		SHEET 2 OF 2	


REVISIONS
A RELEASE - SEE ECO # 2452
B PER ECO 2440
VCC
-8VDC
4PULLUP1 (4, 8, 9)
4PULLUP2 (4, 8, 7, 8, 8, 10)
4PULLUP3 (2, 8, 6, 7, 8)
4PULLUP4 (7, 8, 10)
3 UNUSED GATES WILL EITHER BE ON THE LAST SHEET(S) OF THIS DOCUMENT OR IDENTIFIED BY THIS NOTE.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
1. ALL CAPACITOR VALUES ARE IN MICROFARADS.
NOTES : UNLESS OTHERWISE SPECIFIED
CONFIDENTIAL DOCUMENT
SCHEMATIC DIAGRAM,
DIFE_402
PRINTED CIRCUIT BOARD
NONE
D
1601716-502
A
B

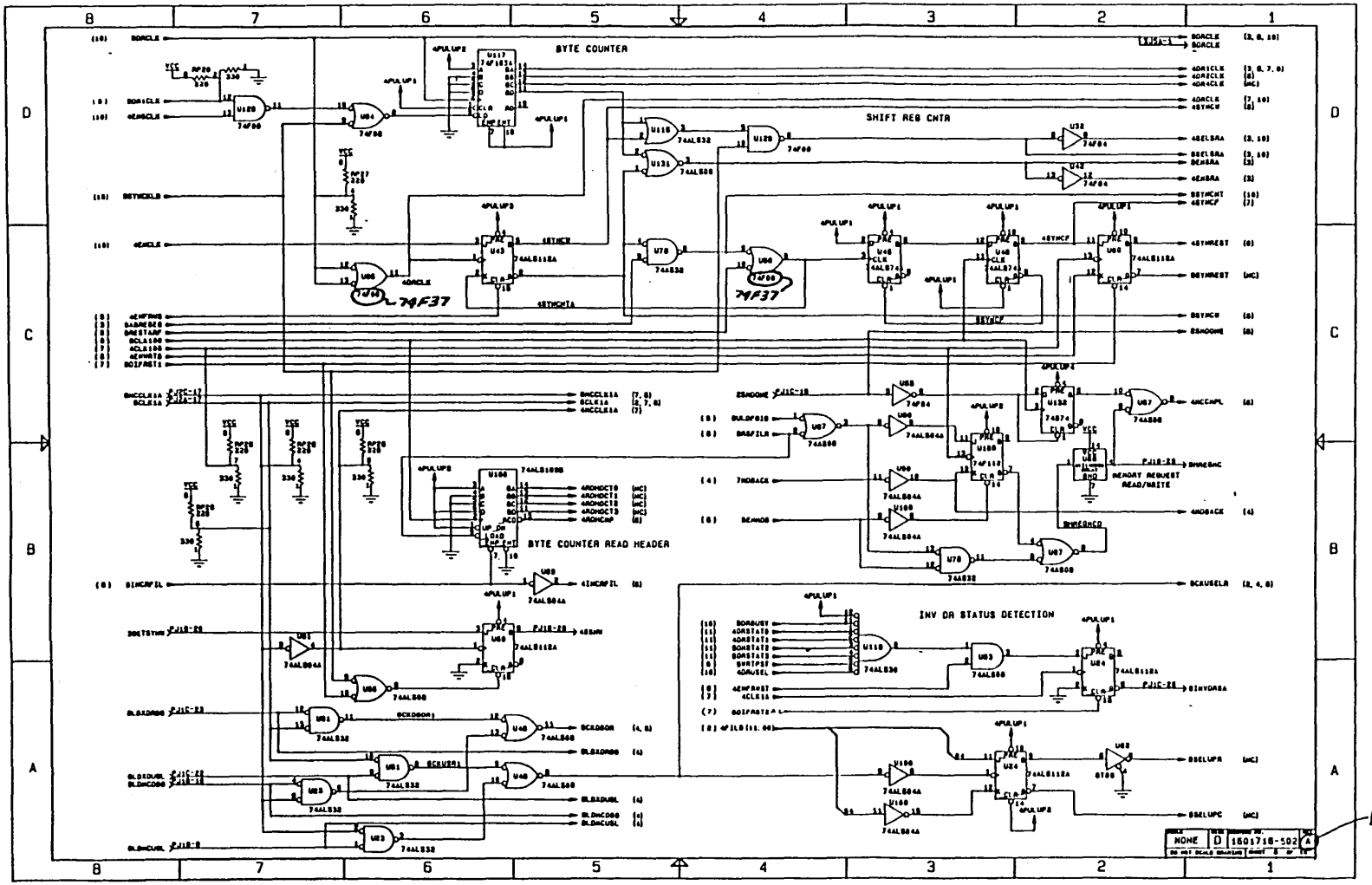
1601716-502 1/12

ECO 2440
SHT 6 OF 9



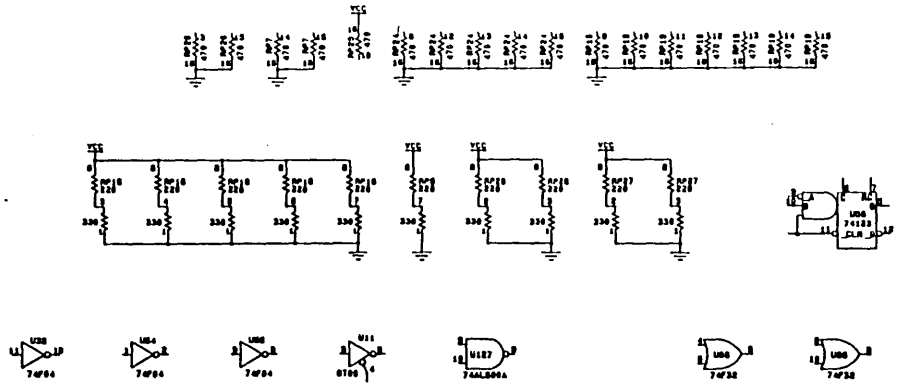
1801718-502 3/12

ECO 2440
SHT 7 OF 9



1601716-502 9/12

ECO 2440
SHT 8 OF 9



DELETE

DEVICE VOLTAGE TABLE					
DEV TYPE	GND	VCC	+12V	-12V	COMPONENT LOCATION
74LS32	8	16			U28
74F00	7	14			U29, U128
74S08	7	14			U99
74S51	7	14			U21
74S74	7	14			U70, U132
74S86	7	14			U30
74S112	8	16			U126
74S133	7	14			U99
74S283	10	20			U17, U29
74S288	7	14			U147, U4, U27, U41, U29
74F299	10	20			U69, U52
74LS259	8	16			U27, U92
74LS298	8	16			U97
74LS367	10	20			U83, U8, U102
74AS888	7	14			U127
74F02	7	14			U19
74AS364	7	14			U98, U99, U83, U100
74F08	7	14			U94, U32, U42, U39
74AS08	7	14			U74, U83, U48, U98, U131
*	*	*			U97
74AS11	7	14			U92
74F20	7	14			U93
74AS30	7	14			U33, U118, U82, U3
74AS32	7	14			U33, U83, U72, U118
74AS37	7	14			U28
74AS74	7	14			U48, U118
74AS112	8	16			U73, U74, U88, U43
*	*	*			U81, U32
74AS138	8	16			U120, U93
74AS193	8	16			U118, U77, U88
74AS193	8	16			U98, U108
MC1458	8	15			U97 *PIN 15 TO -5V
MC10116	8, 16				U45 *PIN 8 TO -5V
MC10116	16	8, 9			U58 *PIN 8 TO -5V
MC10125	16	8			U74 *PIN 8 TO -5V
MC10198	16				U76 *PIN 8 TO -5V
74F37	7	14			U86

ADD

DEVICE VOLTAGE TABLE(CONT'D)					
DEV TYPE	GND	VCC	+12V	-12V	COMPONENT LOCATION
74AS1034	8	16			U88
74AS257	8	16			U13, U18, U19, U28, U40, U104
74AS402	10	20			U112, U83, U39, U84, U18
74F08	7	14			U84
74AS240	10	20			U14
74F321	10	20			U31
74AS299	10	20			U129
74AS374	10	20			U101, U20, U111, U121, U114
*	*	*			U78
74AS378	10	20			U2, U13, U18, U39, U7
*	*	*			U19, U90, U8
74AS620	10	20			U48, U3
74AS870	12	24			U1
74AS899	12	24			U124, U130, U118
AM29707	14	28			U84, U102
AM9321-3	20	40			U74
8T98	7	14			U82, U11
74F112	8	16			U31, U109
74F193	8	16			U117
74F244	10	20			U89
74F74	7	14			U107
74F32	7	14			U98
470 PU	N/A	16			RP22, RP23
470 PDN	10	N/A			RP7, RP24, RP28
820/330 TE	1	8			RP1, RP2, RP3, RP4, RP5
*	*	*			RP8, RP15, RP20, RP21
7406	7	14			RP27, RP28
8T97/81A	10	24			U78
74LS2	10	20			U122, U73
56 Ohm SIP	8				U39, U49, U103, U123
22 Ohm SIP	8				RP9, RP11
1000hm SIP					RP10
1800hm SIP					RP12, RP16
4700hm SIP	1				RP14, RP17
2000hm SIP					RP13, RP18 *PIN 1 TO -5V
4700hm SIP					RP19

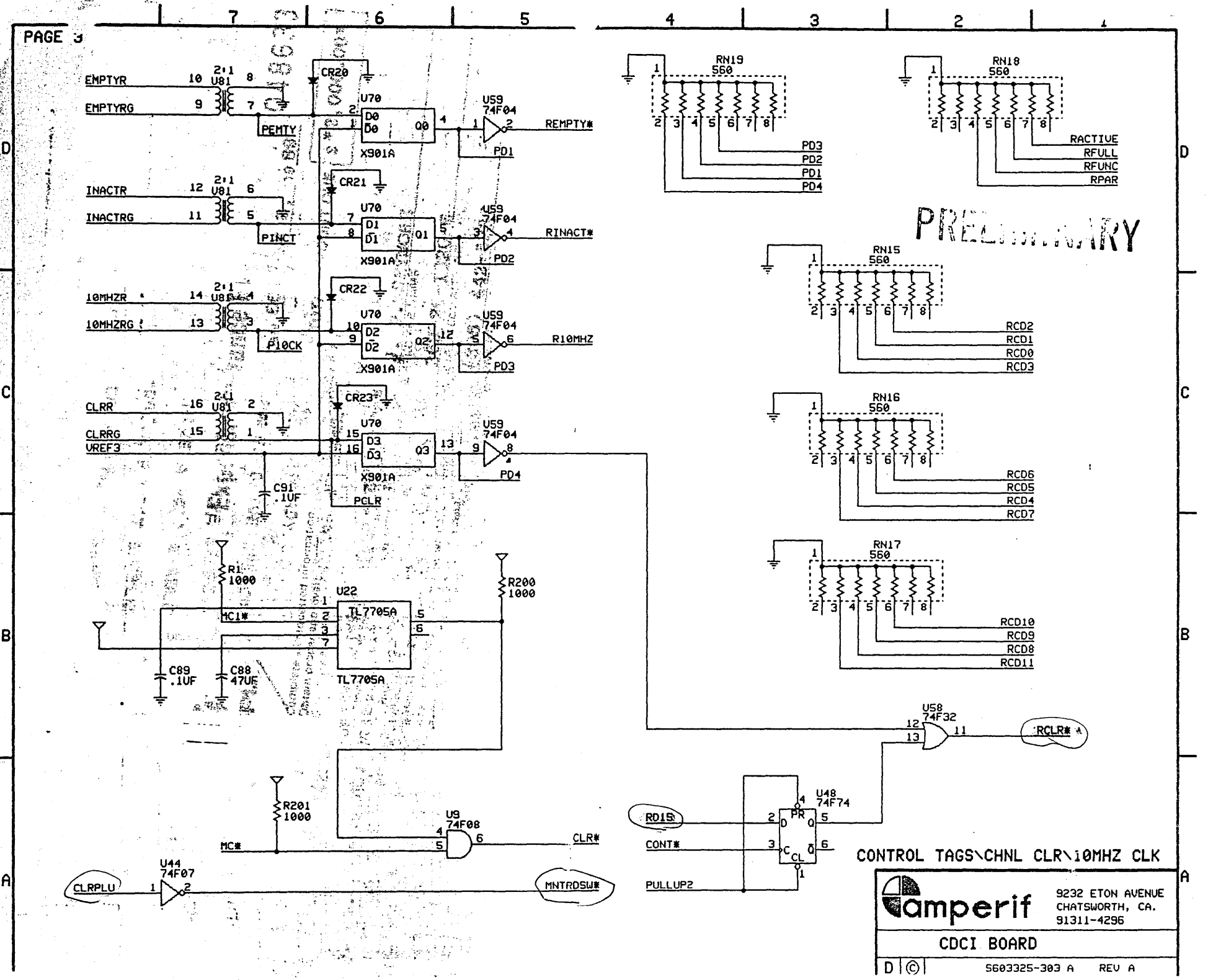
DEVICE VOLTAGE TABLE					
DEV TYPE	GND	VCC	+12V	-12V	COMPONENT LOCATION
1884	10	20			U44
8T98	10	20			U108, U104, U129
DELAY 2MB	7	14			U88
74AS08	7	14			U87
56 Ohm PDN	10				RP10

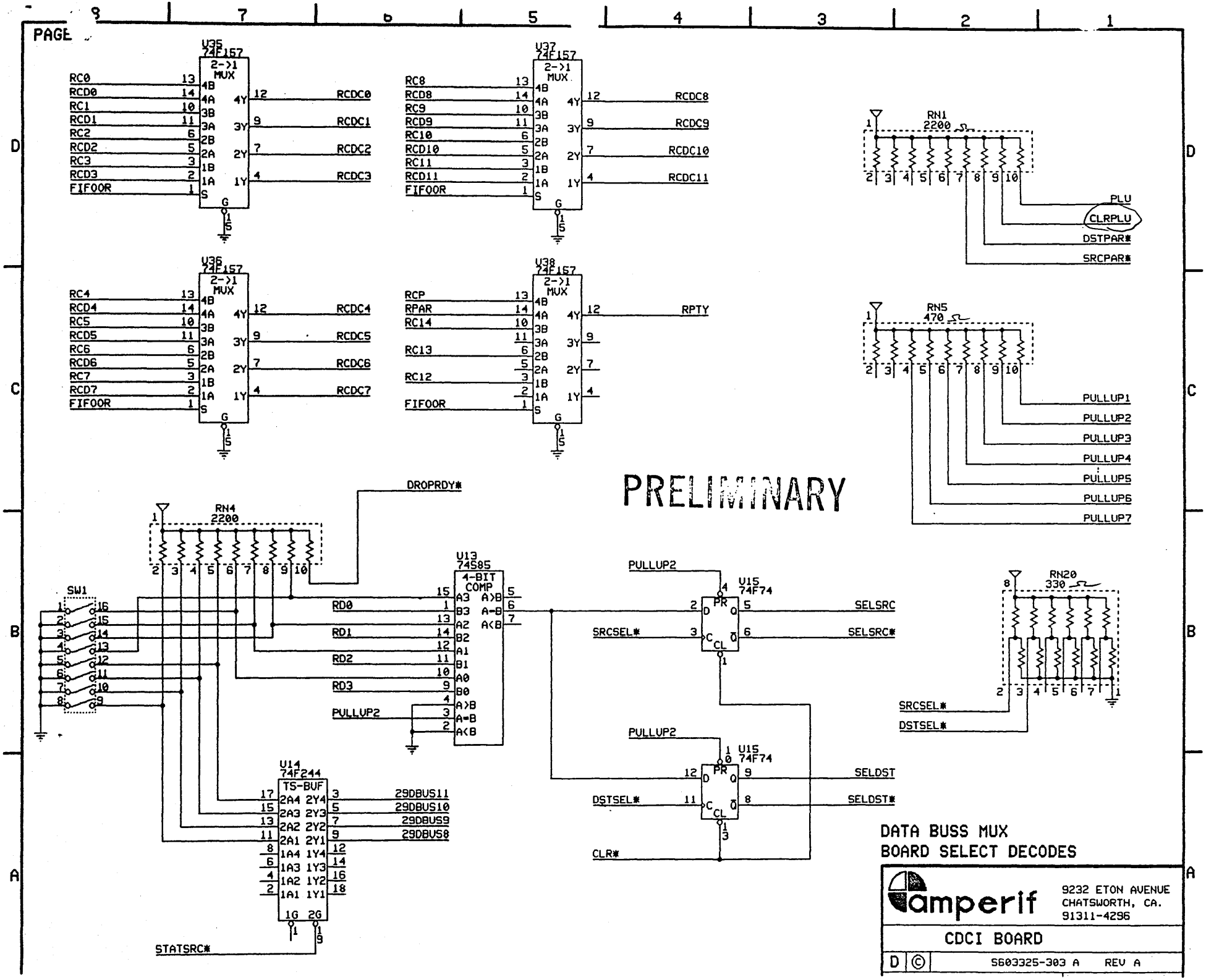
B

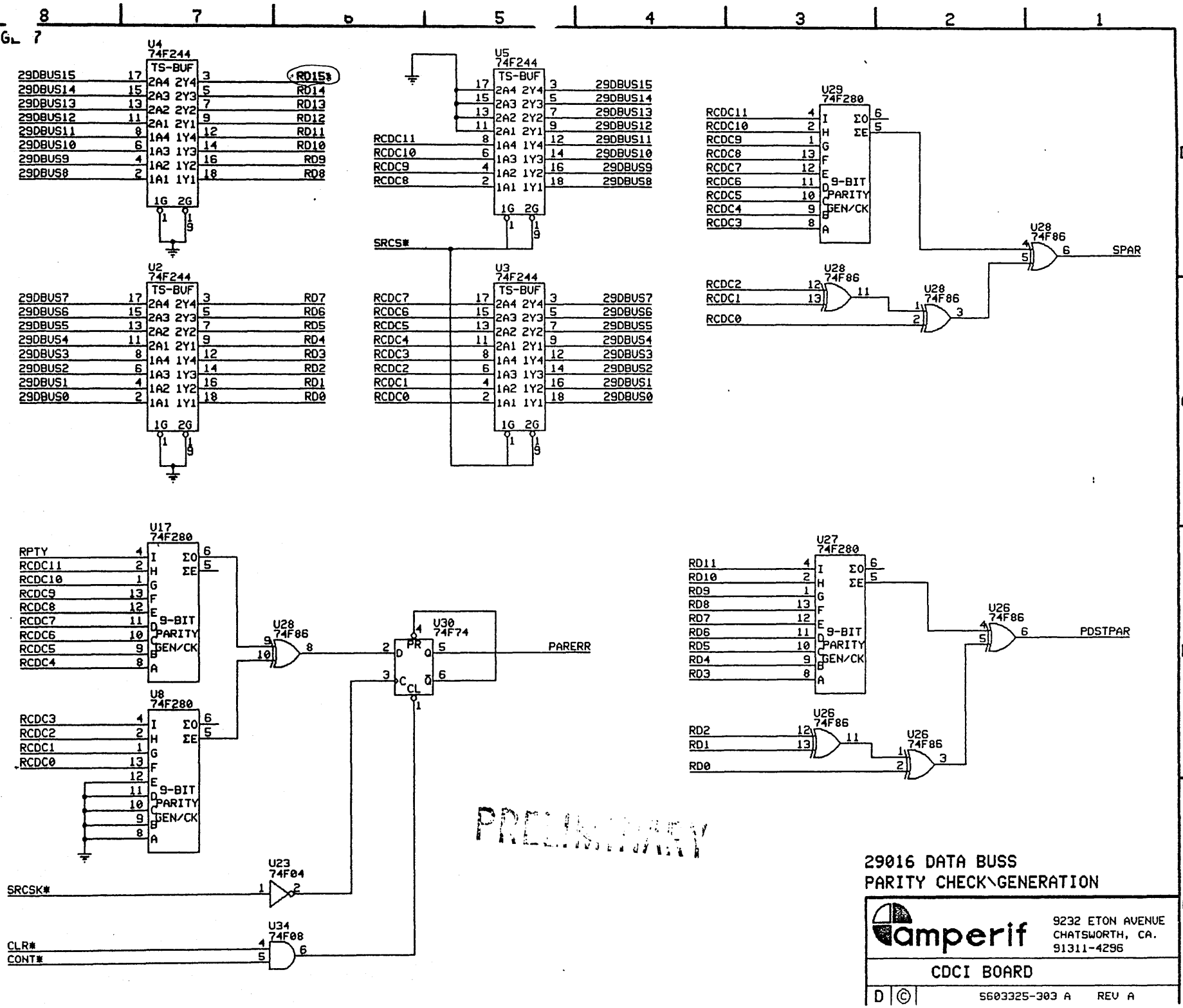
NONE	D	1801718-502	X	

16 OCT 86-SOC 12/12

ECO' 2440
SHT 9 OF 9

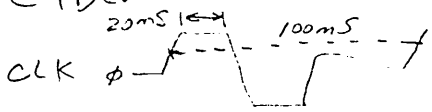

PAGE 3
EMPTYR
EMPTYRG
PEMTY
CR20
U70
X901A
U59
74F04
REMPTY*
PD1
INACTR
INACTRG
PINCT
CR21
RINACT*
PD2
10MHZR
10MHZRG
P10CK
CR22
R10MHZ
PD3
CLRR
CLRRG
VREF3
CR23
PD4
C91
.1UF
PCLR
R1
1000
HC1*
U22
TL7705A
R200
C89
.1UF
C88
47UF
R201
MC*
U9
74F08
CLR*
CLRPLU
U44
74F07
MNTRDSW*
RN19
560
PD3
PD2
PD1
PD4
RN18
RACTIVE
RFULL
RFUNC
RPAR
PRELIMINARY
RN15
RCD2
RCD1
RCD0
RCD3
RN16
RCD6
RCD5
RCD4
RCD7
RN17
RCD10
RCD9
RCD8
RCD11
U58
74F32
RCLR*
RD15
CONT*
PULLUP2
U48
74F74
CONTROL TAGS\CHNL CLR\10MHZ CLK
amperif
9232 ETON AVENUE
CHATSWORTH, CA.
91311-4296
CDCI BOARD
D
S603325-303 A
REV A


PAGE
U35 74F157 2->1 MUX
RC0 RCD0 RC1 RCD1 RC2 RCD2 RC3 RCD3 FIFOOR
RCDC0 RCDC1 RCDC2 RCDC3
U37 74F157 2->1 MUX
RC8 RCD8 RC9 RCD9 RC10 RCD10 RC11 RCD11 FIFOOR
RCDC8 RCDC9 RCDC10 RCDC11
U36 74F157 2->1 MUX
RC4 RCD4 RC5 RCD5 RC6 RCD6 RC7 RCD7 FIFOOR
RCDC4 RCDC5 RCDC6 RCDC7
U38 74F157 2->1 MUX
RCP RPAR RC14 RC13 RC12 FIFOOR
RPTY
RN1 2200
PLU CLRPLU DSTPAR* SRCPAR*
RN5 470
PULLUP1 PULLUP2 PULLUP3 PULLUP4 PULLUP5 PULLUP6 PULLUP7
PRELIMINARY
DROPRDY*
RN4 2200
SW1
U13 74S85 4-BIT COMP
RD0 RD1 RD2 RD3 PULLUP2
U15 74F74
SRCSEL* SELSRC SELSRC*
RN20 330
SRCSEL* DSTSEL*
U15 74F74
DSTSEL* SELDST SELDST*
CLR*
U14 74F244 TS-BUF
29DBUS11 29DBUS10 29DBUS9 29DBUS8
STATSRC*
DATA BUSS MUX
BOARD SELECT DECODES
amperif
9232 ETON AVENUE
CHATSWORTH, CA.
91311-4296
CDCI BOARD
S603325-303 A REV A


PAGE 7
U4 74F244 TS-BUF
29DBUS15 29DBUS14 29DBUS13 29DBUS12 29DBUS11 29DBUS10 29DBUS9 29DBUS8
RD15 RD14 RD13 RD12 RD11 RD10 RD9 RD8
U5 74F244 TS-BUF
RCDC11 RCDC10 RCDC9 RCDC8
29DBUS15 29DBUS14 29DBUS13 29DBUS12 29DBUS11 29DBUS10 29DBUS9 29DBUS8
SRCS*
U2 74F244 TS-BUF
29DBUS7 29DBUS6 29DBUS5 29DBUS4 29DBUS3 29DBUS2 29DBUS1 29DBUS0
RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0
U3 74F244 TS-BUF
RCDC7 RCDC6 RCDC5 RCDC4 RCDC3 RCDC2 RCDC1 RCDC0
29DBUS7 29DBUS6 29DBUS5 29DBUS4 29DBUS3 29DBUS2 29DBUS1 29DBUS0
U29 74F280 9-BIT PARITY GEN/CK
RCDC11 RCDC10 RCDC9 RCDC8 RCDC7 RCDC6 RCDC5 RCDC4 RCDC3
U28 74F86
RCDC2 RCDC1 RCDC0
SPAR
U17 74F280 9-BIT PARITY GEN/CK
RPTY RCDC11 RCDC10 RCDC9 RCDC8 RCDC7 RCDC6 RCDC5 RCDC4
U28 74F86
U8 74F280 9-BIT PARITY GEN/CK
RCDC3 RCDC2 RCDC1 RCDC0
U30 74F74 PR CL
PARERR
U23 74F04
SRCSK*
U34 74F08
CLR*
CONT*
U27 74F280 9-BIT PARITY GEN/CK
RD11 RD10 RD9 RD8 RD7 RD6 RD5 RD4 RD3
U26 74F86
RD2 RD1 RD0
PDSTPAR
PRELIMINARY
29016 DATA BUSS
PARITY CHECK\GENERATION
amperif
9232 ETON AVENUE
CHATSWORTH, CA.
91311-4296
CDCI BOARD
D
5603325-303 A
REV A

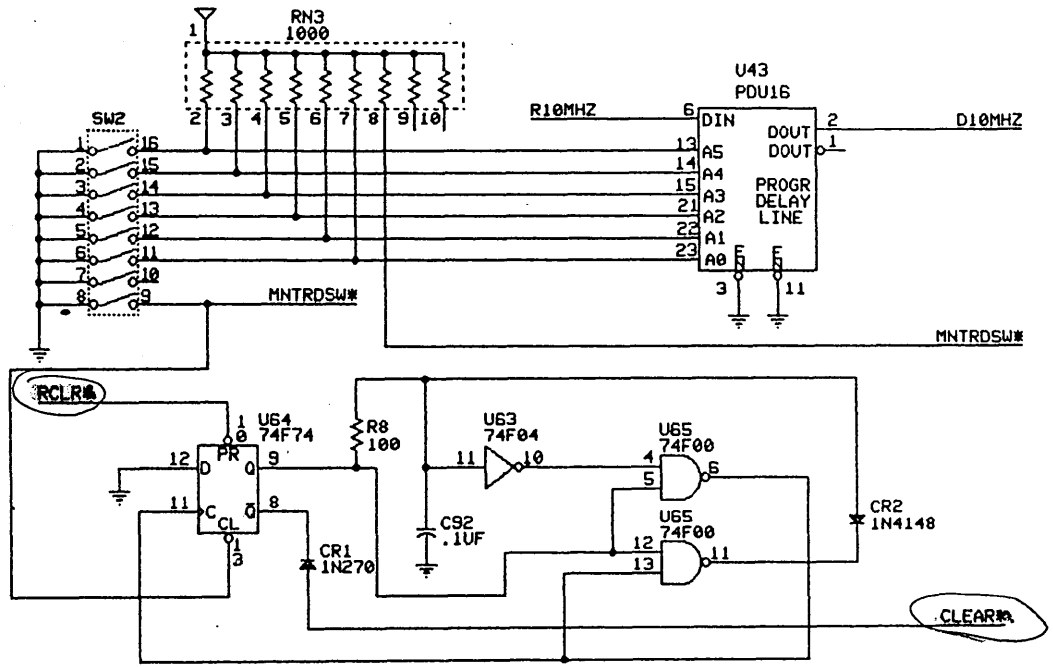
PAGE 10

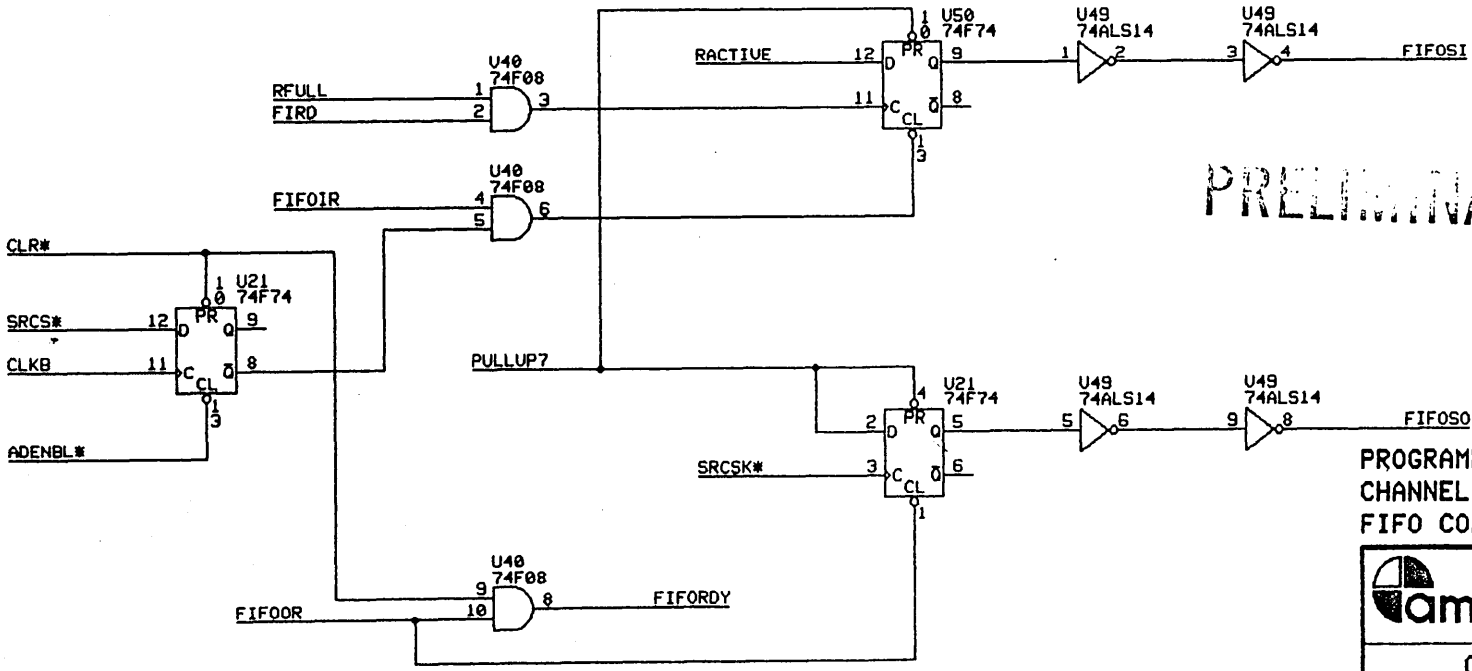
CYBER 830 ch'in



FULL

SW2-4 = OFF





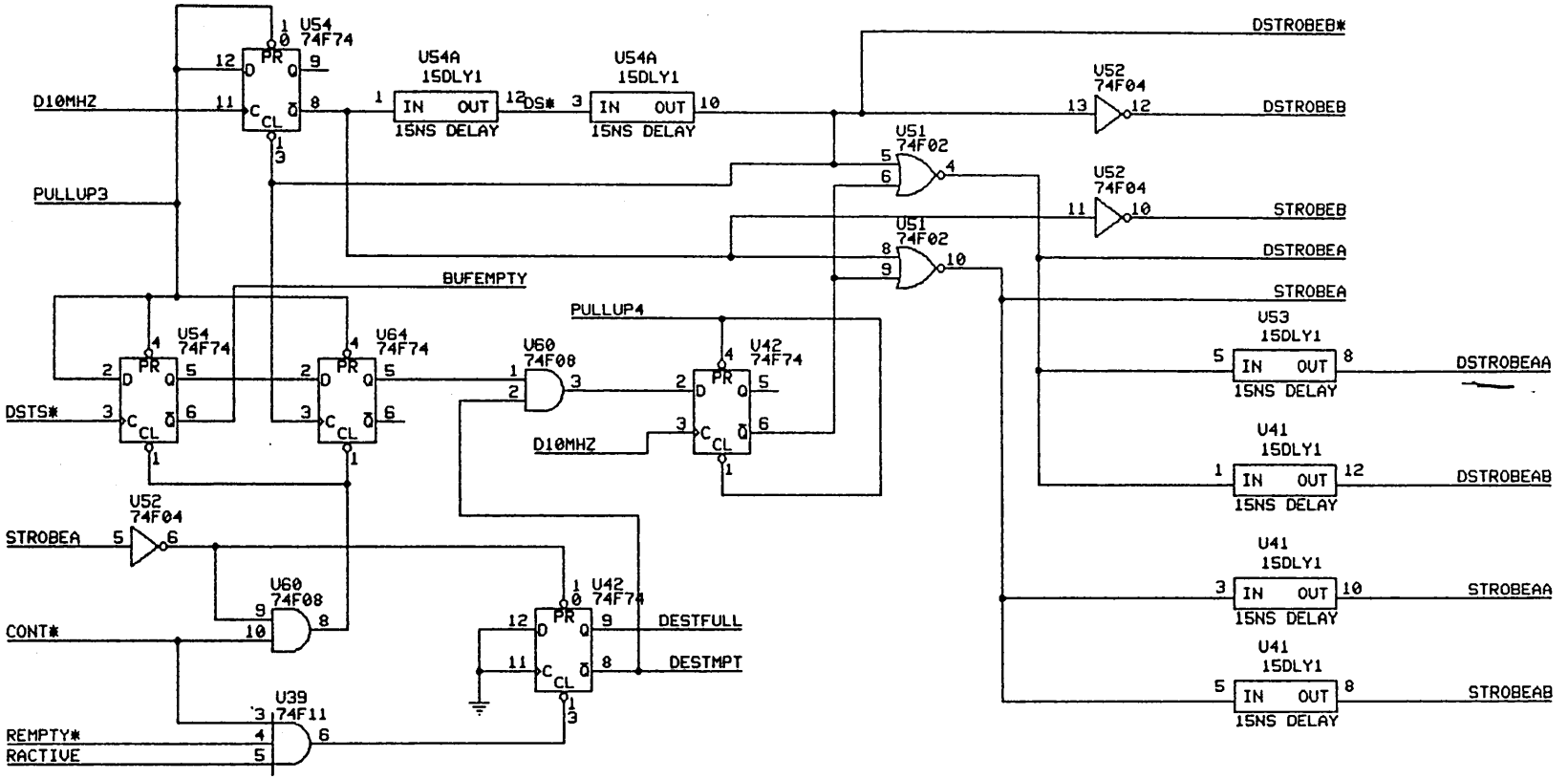
PRELIMINARY

PROGRAMMABLE 10MHZ DELAY LOGIC
CHANNEL CLEAR
FIFO CONTROL

amperif
9232 ETON AVENUE
CHATSWORTH, CA.
91311-4296

CDCI BOARD

PAGE 11



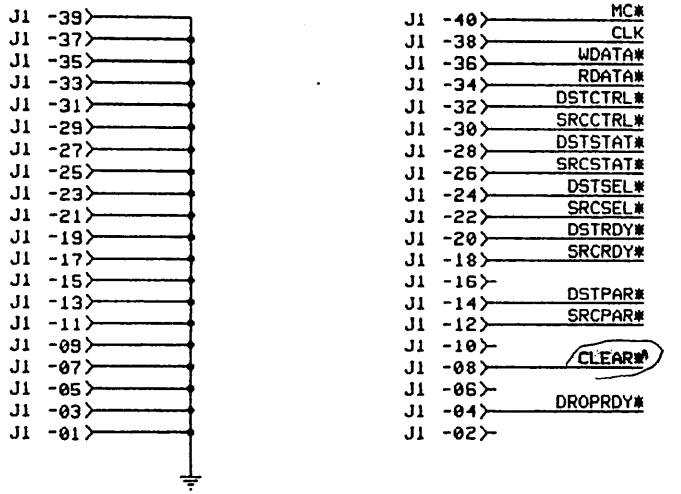
DATA TAG CLOCK GENERATION

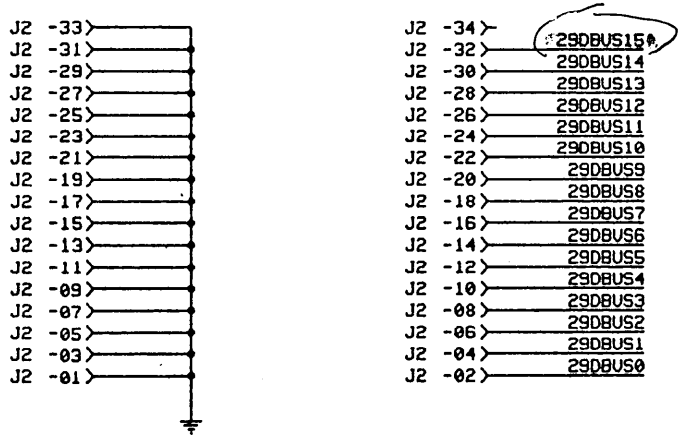
amperif
9232 ETON AVENUE
CHATSWORTH, CA.
91311-4296

CDCI BOARD

D | 0 | 5603325-303 A | REV A

PAGE





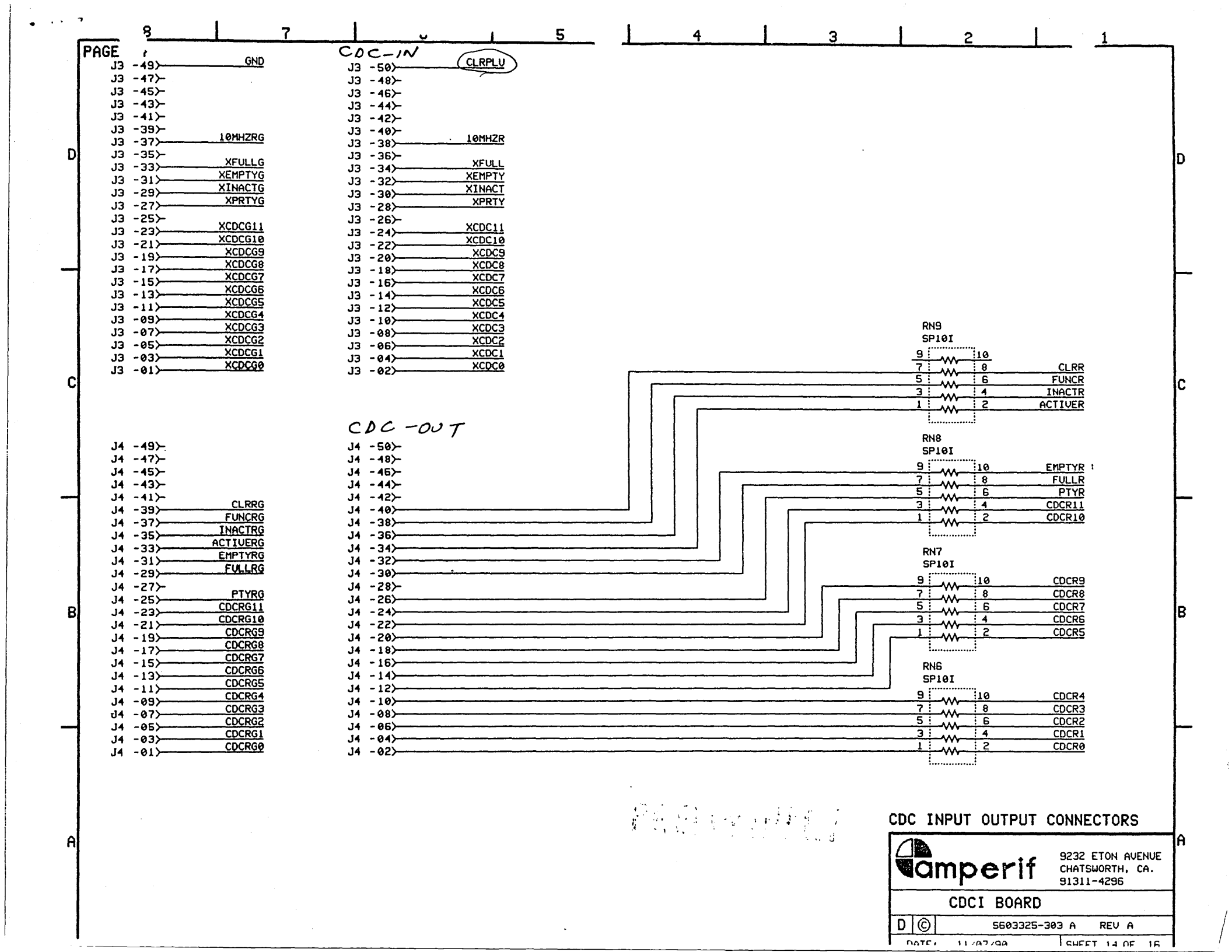
PRELIMINARY

J1,J2 CONN \ CAP LAYOUT

amperif
9232 ETON AVENUE
CHATSWORTH, CA.
91311-4296

CDCI BOARD

D | © | 5603325-303 A REV A

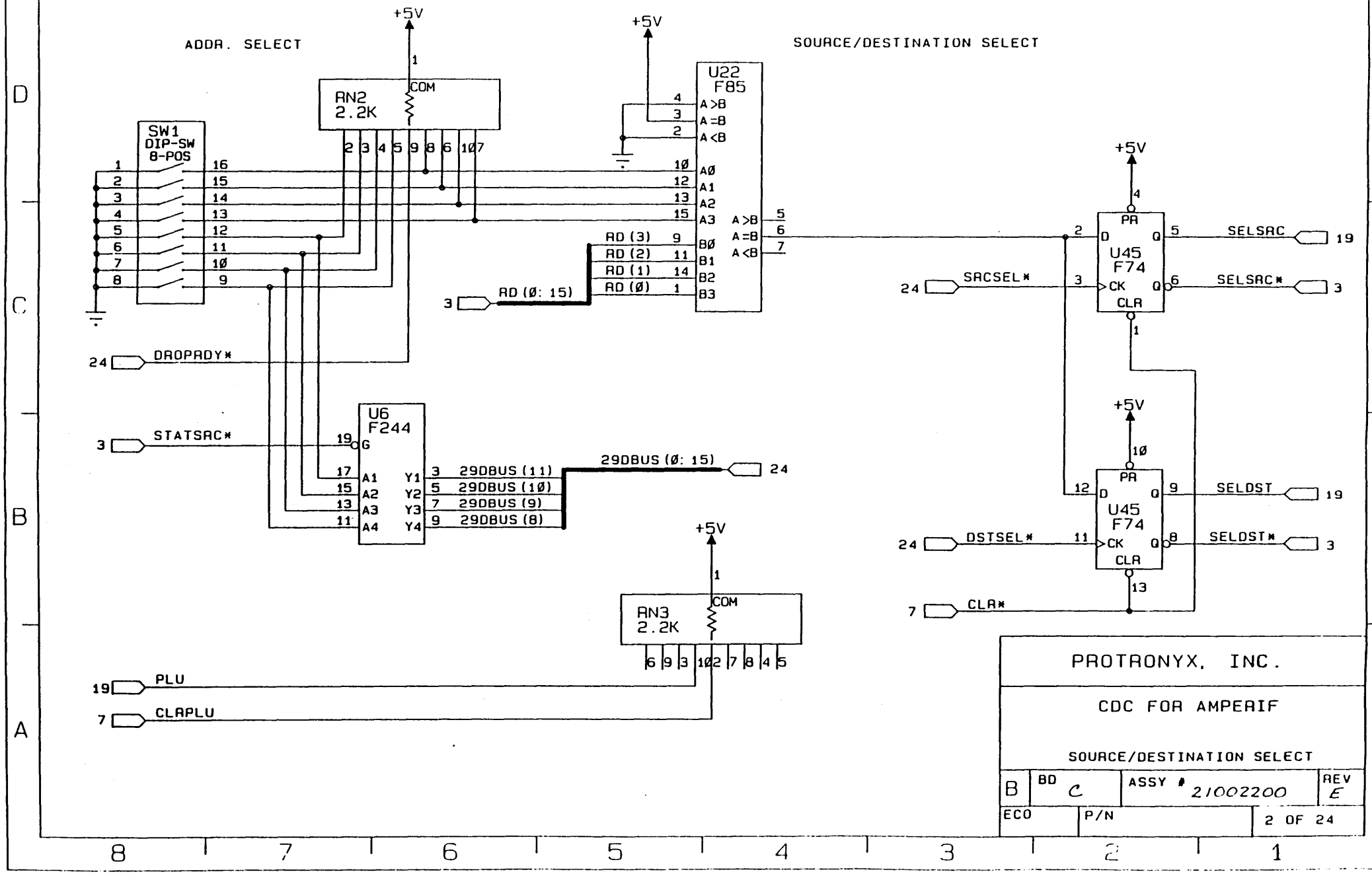

PAGE
CDC-IN
J3 -49) GND
J3 -47)
J3 -45)
J3 -43)
J3 -41)
J3 -39)
J3 -37) 10MHZRG
J3 -35)
J3 -33) XFULLG
J3 -31) XEMPTYG
J3 -29) XINACTG
J3 -27) XPRTYG
J3 -25)
J3 -23) XCDCG11
J3 -21) XCDCG10
J3 -19) XCDCG9
J3 -17) XCDCG8
J3 -15) XCDCG7
J3 -13) XCDCG6
J3 -11) XCDCG5
J3 -09) XCDCG4
J3 -07) XCDCG3
J3 -05) XCDCG2
J3 -03) XCDCG1
J3 -01) XCDCG0
J3 -50) CLRPLU
J3 -48)
J3 -46)
J3 -44)
J3 -42)
J3 -40)
J3 -38) 10MHZR
J3 -36)
J3 -34) XFULL
J3 -32) XEMPTY
J3 -30) XINACT
J3 -28) XPRTY
J3 -26)
J3 -24) XCDC11
J3 -22) XCDC10
J3 -20) XCDC9
J3 -18) XCDC8
J3 -16) XCDC7
J3 -14) XCDC6
J3 -12) XCDC5
J3 -10) XCDC4
J3 -08) XCDC3
J3 -06) XCDC2
J3 -04) XCDC1
J3 -02) XCDC0
CDC-OUT
J4 -49)
J4 -47)
J4 -45)
J4 -43)
J4 -41)
J4 -39) CLRRG
J4 -37) FUNCRG
J4 -35) INACTRG
J4 -33) ACTIVERG
J4 -31) EMPTYRG
J4 -29) FULLRG
J4 -27)
J4 -25) PTYRG
J4 -23) CDCRG11
J4 -21) CDCRG10
J4 -19) CDCRG9
J4 -17) CDCRG8
J4 -15) CDCRG7
J4 -13) CDCRG6
J4 -11) CDCRG5
J4 -09) CDCRG4
J4 -07) CDCRG3
J4 -05) CDCRG2
J4 -03) CDCRG1
J4 -01) CDCRG0
J4 -50)
J4 -48)
J4 -46)
J4 -44)
J4 -42)
J4 -40)
J4 -38)
J4 -36)
J4 -34)
J4 -32)
J4 -30)
J4 -28)
J4 -26)
J4 -24)
J4 -22)
J4 -20)
J4 -18)
J4 -16)
J4 -14)
J4 -12)
J4 -10)
J4 -08)
J4 -06)
J4 -04)
J4 -02)
RN9
SP10I
9 10
7 8 CLRR
5 6 FUNCR
3 4 INACTR
1 2 ACTIVER
RN8
SP10I
9 10 EMPTYR
7 8 FULLR
5 6 PTYR
3 4 CDCR11
1 2 CDCR10
RN7
SP10I
9 10 CDCR9
7 8 CDCR8
5 6 CDCR7
3 4 CDCR6
1 2 CDCR5
RN6
SP10I
9 10 CDCR4
7 8 CDCR3
5 6 CDCR2
3 4 CDCR1
1 2 CDCR0
CDC INPUT OUTPUT CONNECTORS
amperif
9232 ETON AVENUE
CHATSWORTH, CA.
91311-4296
CDCI BOARD
D ©
5603325-303 A REV A
DATE: 11/07/90
SHEET 14 OF 16

COMPLETED APRIL 24, 1986

Initial Release of Rev. C Bd. - ECO# 131

PROTRONYX, INC.			
CDC FOR AMPERIF			
REVISION HISTORY			
B	BD C	ASSY # 21002200	REV E
ECO	P/N		1 OF 24

ECO 2568
SH 15



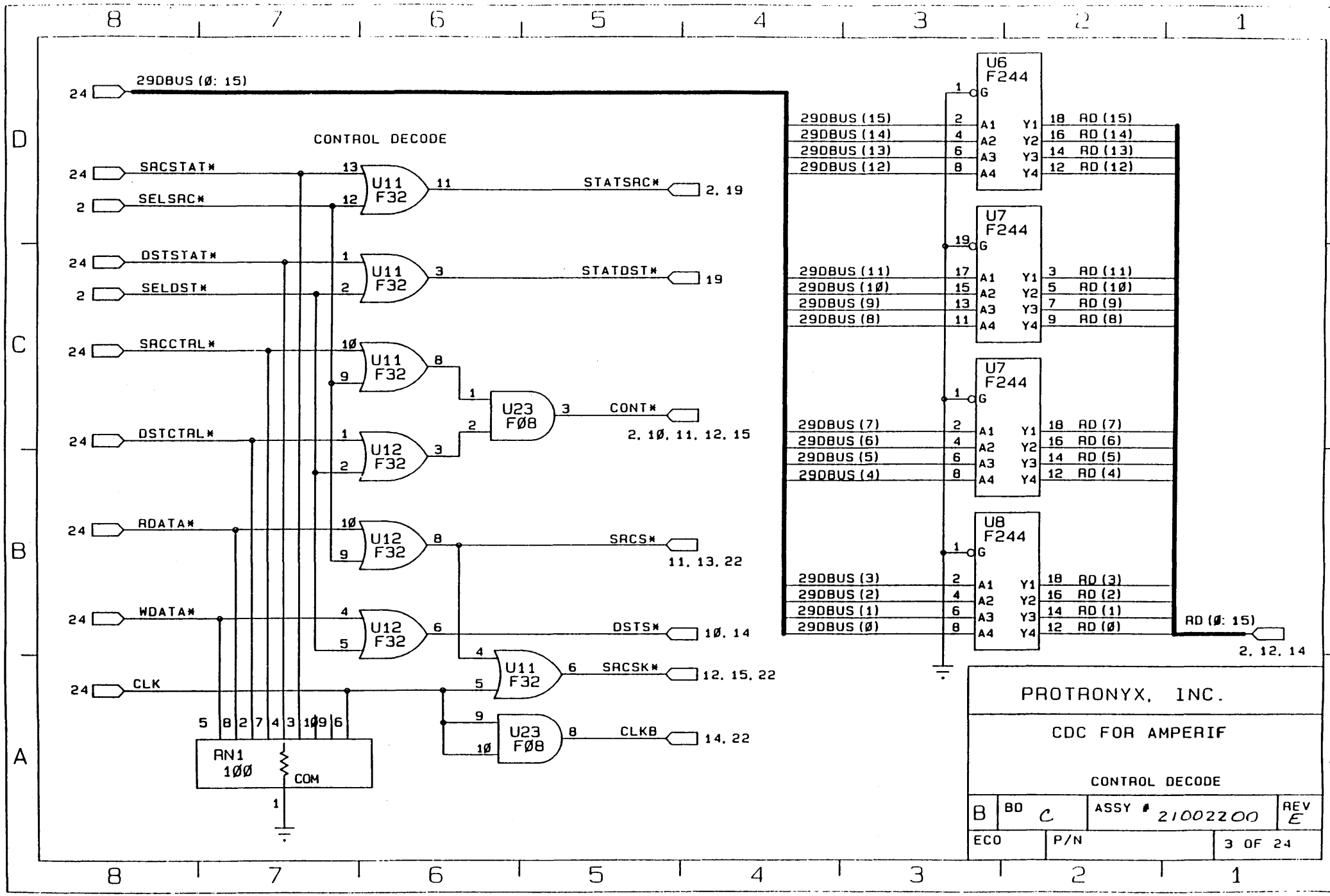
PROTRONYX, INC.

CDC FOR AMPERIF

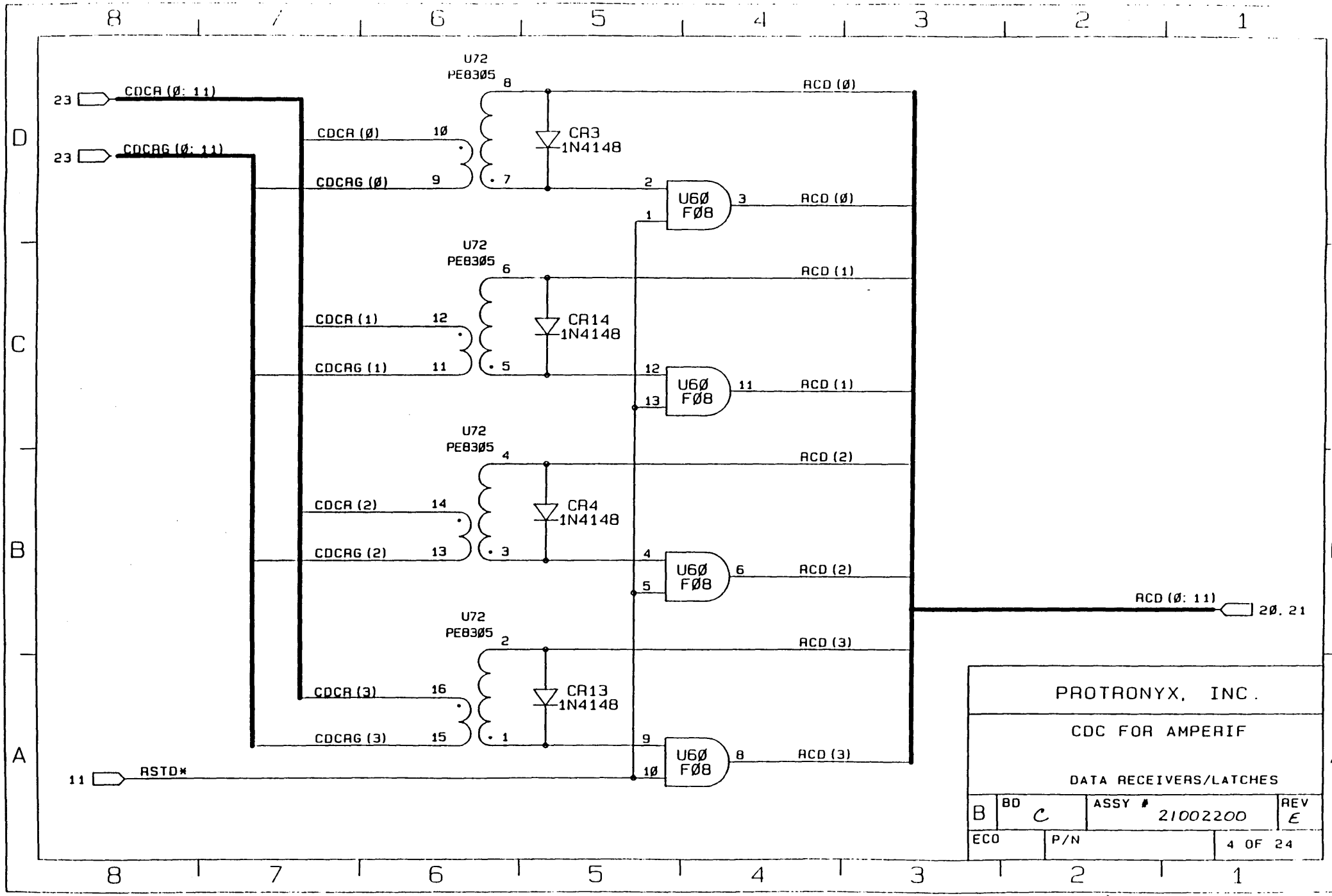
SOURCE/DESTINATION SELECT

B	BD C	ASSY # 21002200	REV E
ECO	P/N		2 OF 24

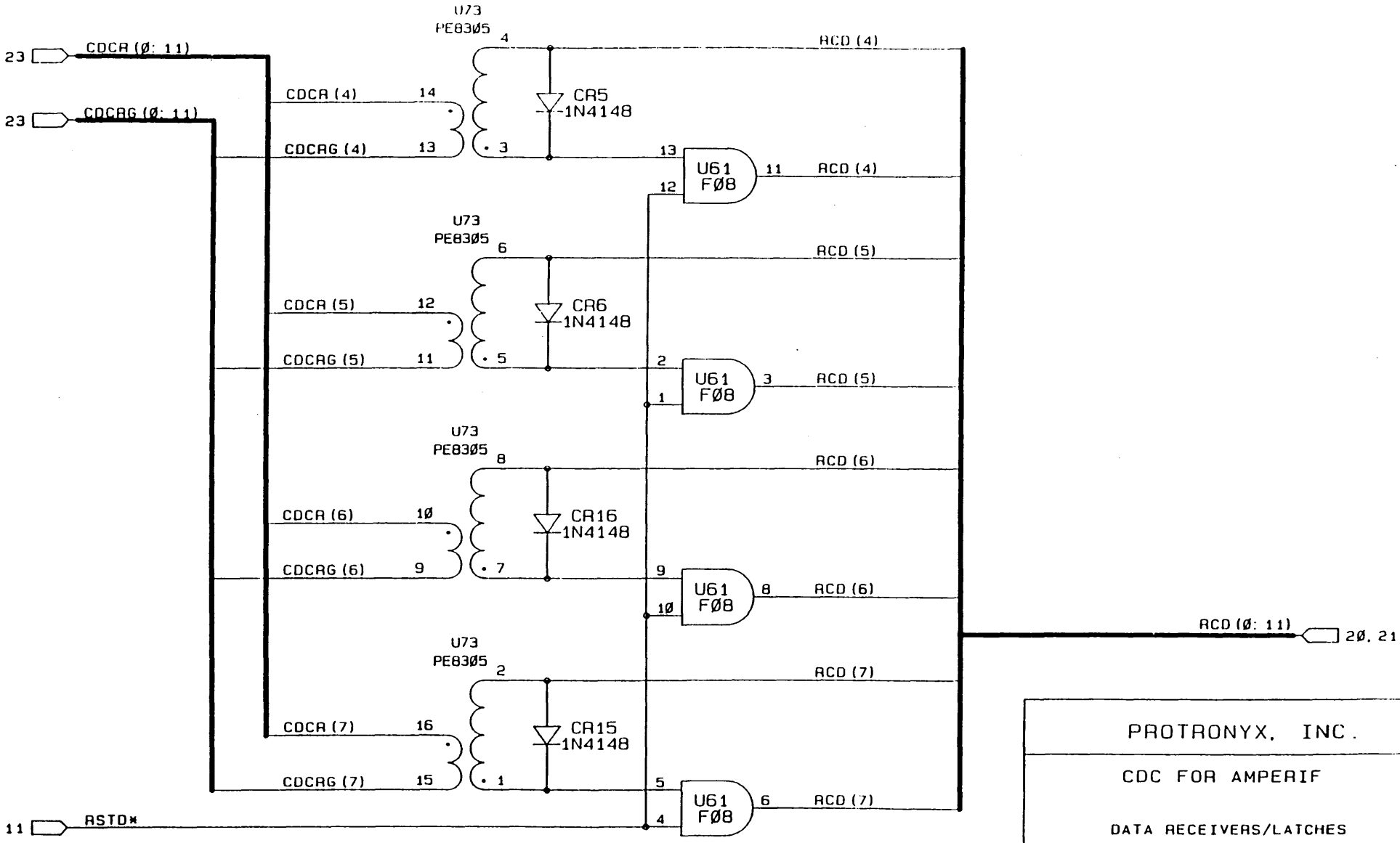
ECO 2588
SH 76



ECO 2588
SH 77

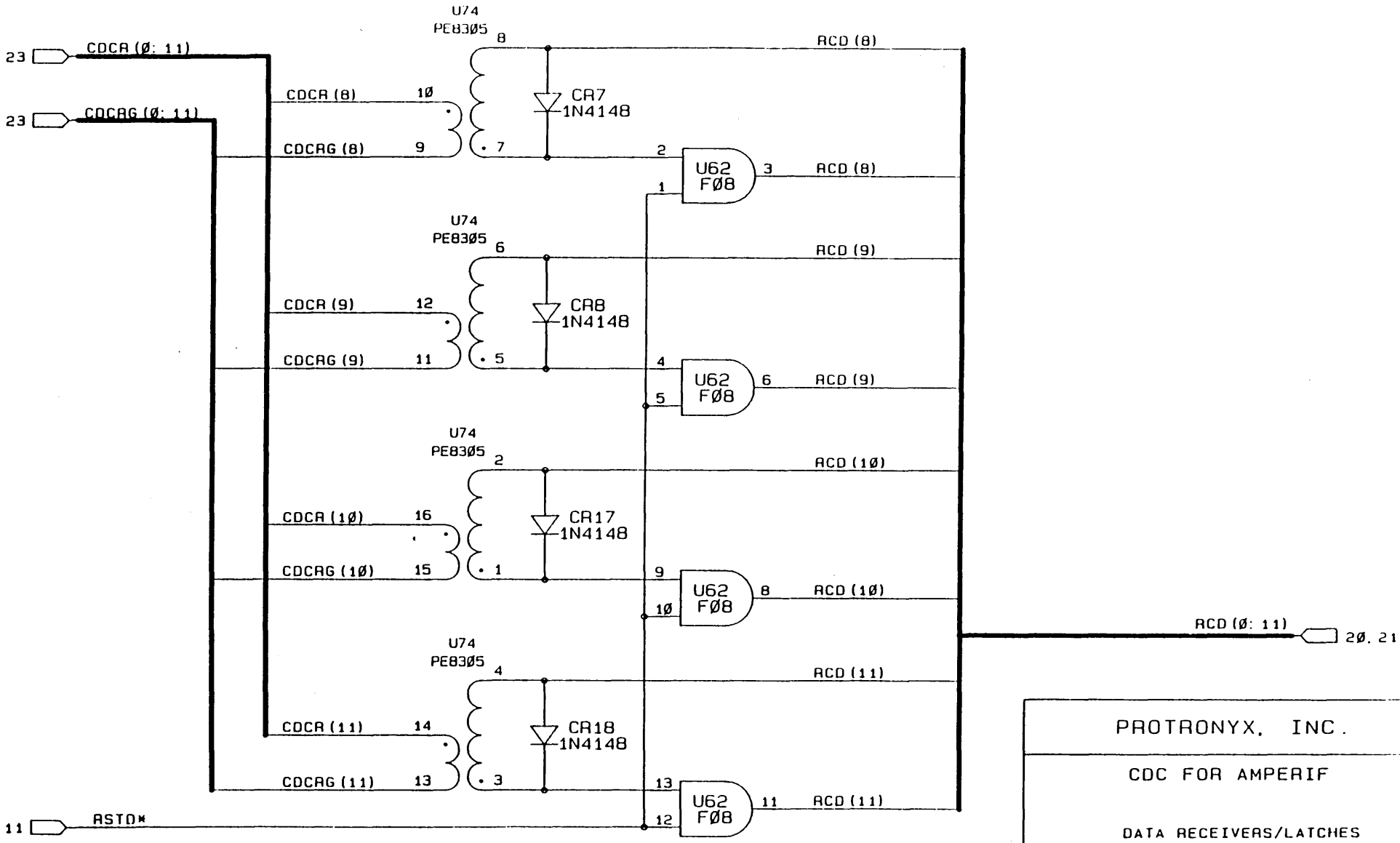


ECO 2586
SH 78



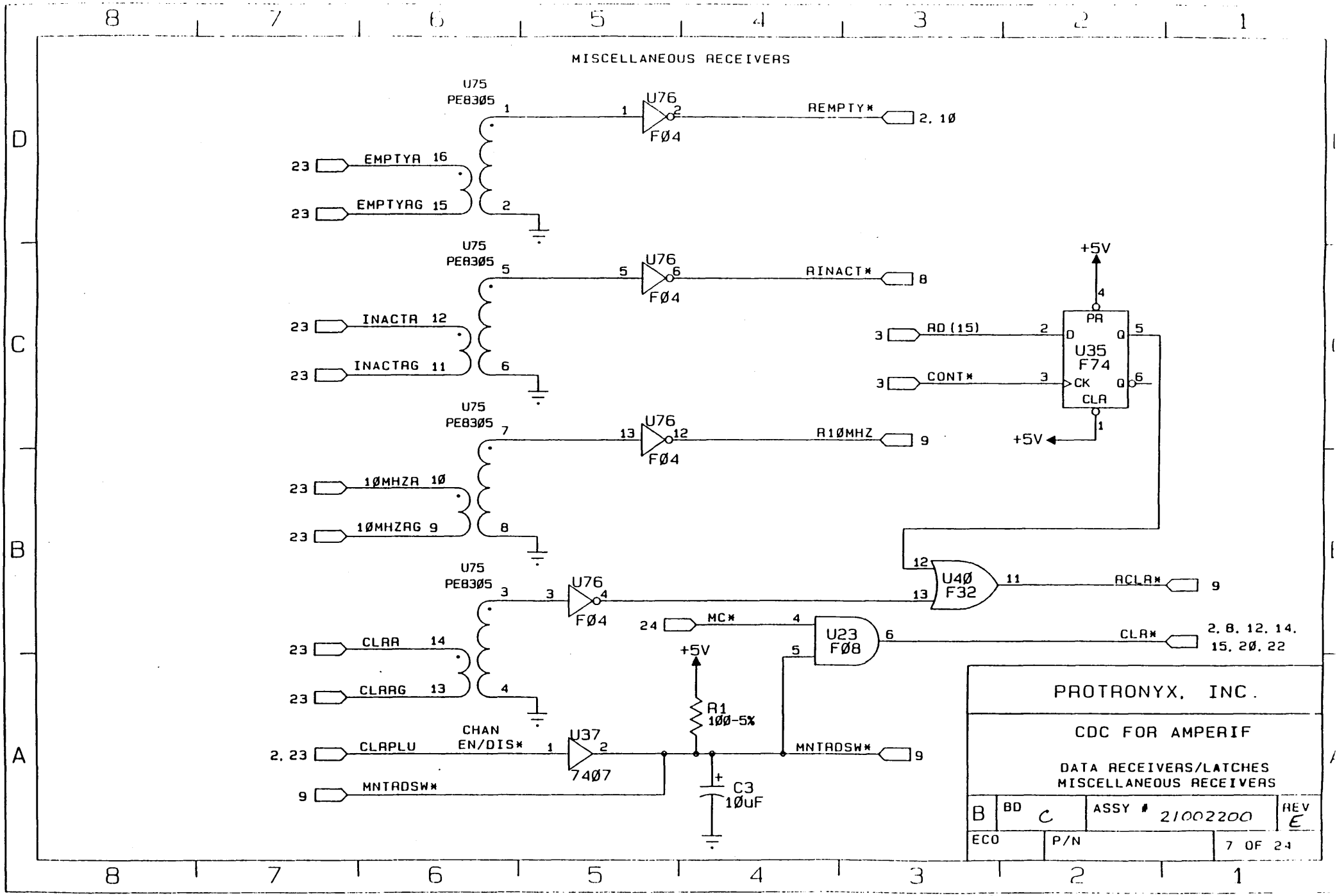
PROTRONYX, INC.			
CDC FOR AMPERIF			
DATA RECEIVERS/LATCHES			
B	BD C	ASSY # 21002200	REV E
ECO	P/N	5 OF 24	

ECO 2556
SH 79

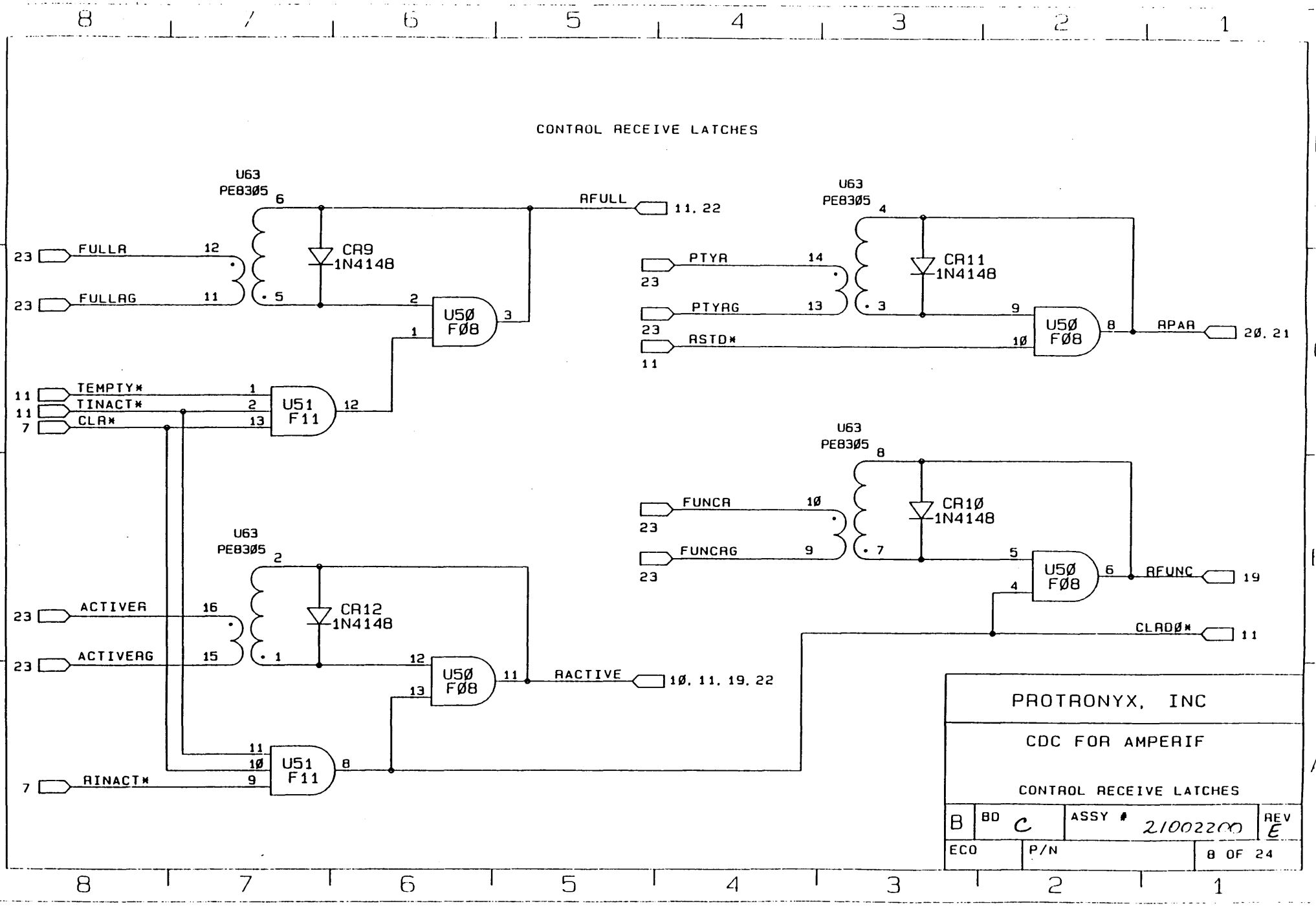


PROTRONYX, INC.			
CDC FOR AMPERIF			
DATA RECEIVERS/LATCHES			
B	BD C	ASSY # 21002200	REV E
ECO	P/N	6 OF 24	

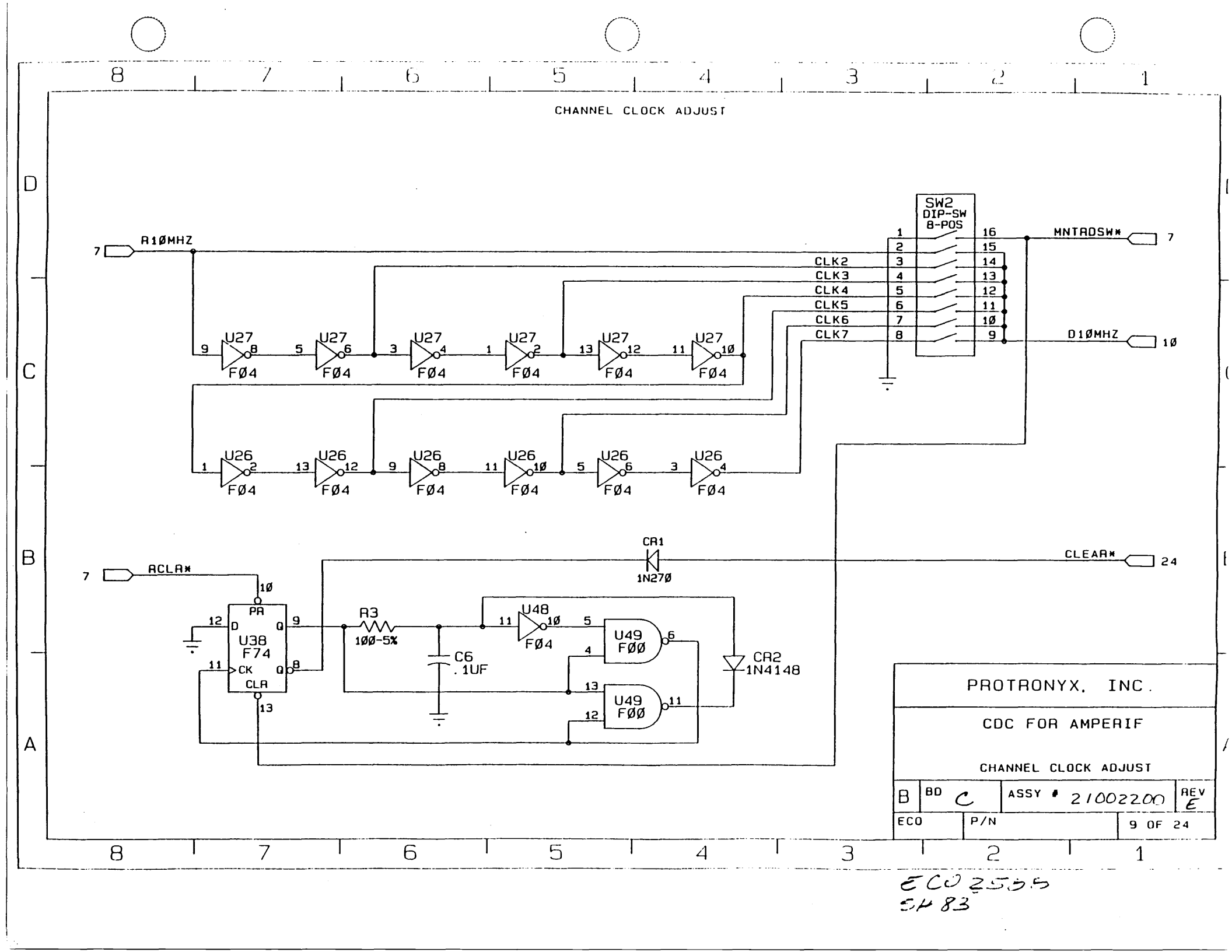
EC1-2515
SH 3?


MISCELLANEOUS RECEIVERS
U75
PE8305
U76
FØ4
REMPTY*
2, 1Ø
EMPTYA
EMPTYAG
RINACT*
8
INACTA
INACTAG
RD(15)
CONT*
U35
F74
PR
CLR
+5V
R1ØMHZ
9
1ØMHZA
1ØMHZAG
U4Ø
F32
RCLR*
MC*
U23
FØ8
CLR*
2, 8, 12, 14, 15, 2Ø, 22
CLRA
CLRAG
R1
1ØØ-5%
CHAN
EN/DIS*
U37
7407
CLAPLU
MNTRDSW*
C3
1ØuF
PROTRONYX, INC.
CDC FOR AMPERIF
DATA RECEIVERS/LATCHES
MISCELLANEOUS RECEIVERS
B
BD C
ASSY # 21002200
REV E
ECO
P/N
7 OF 24

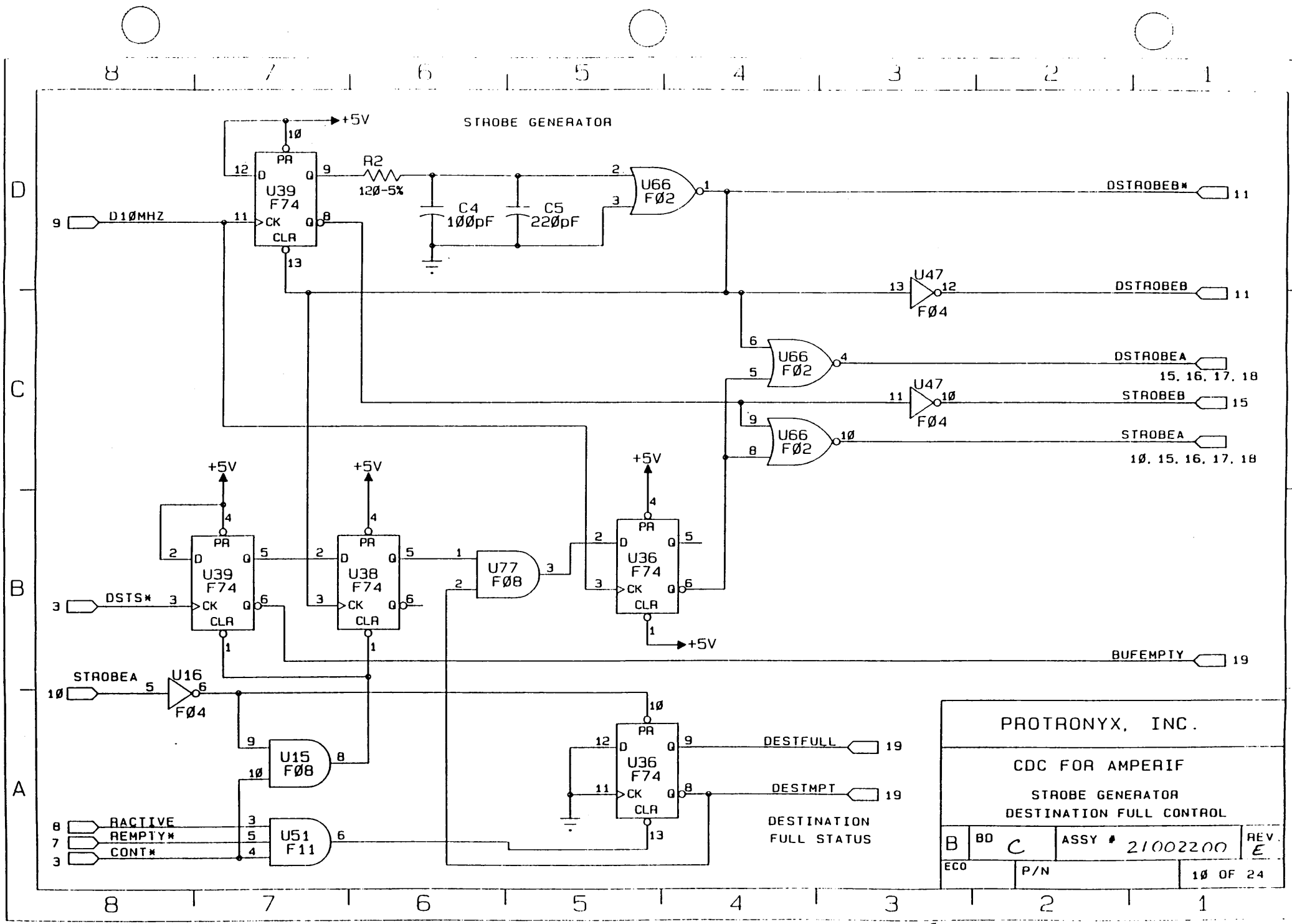
50255
SH 81



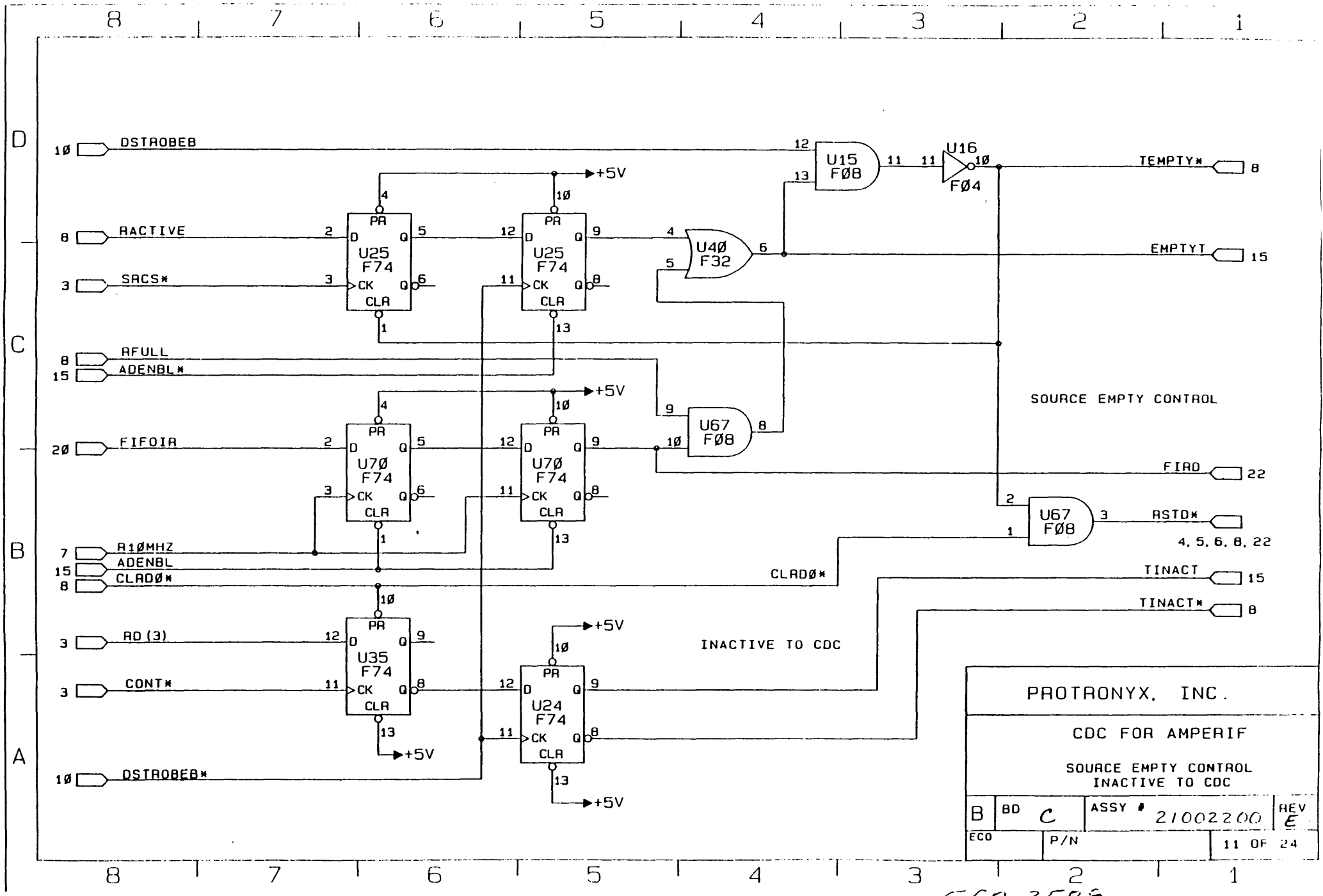
E 002540
SH 82



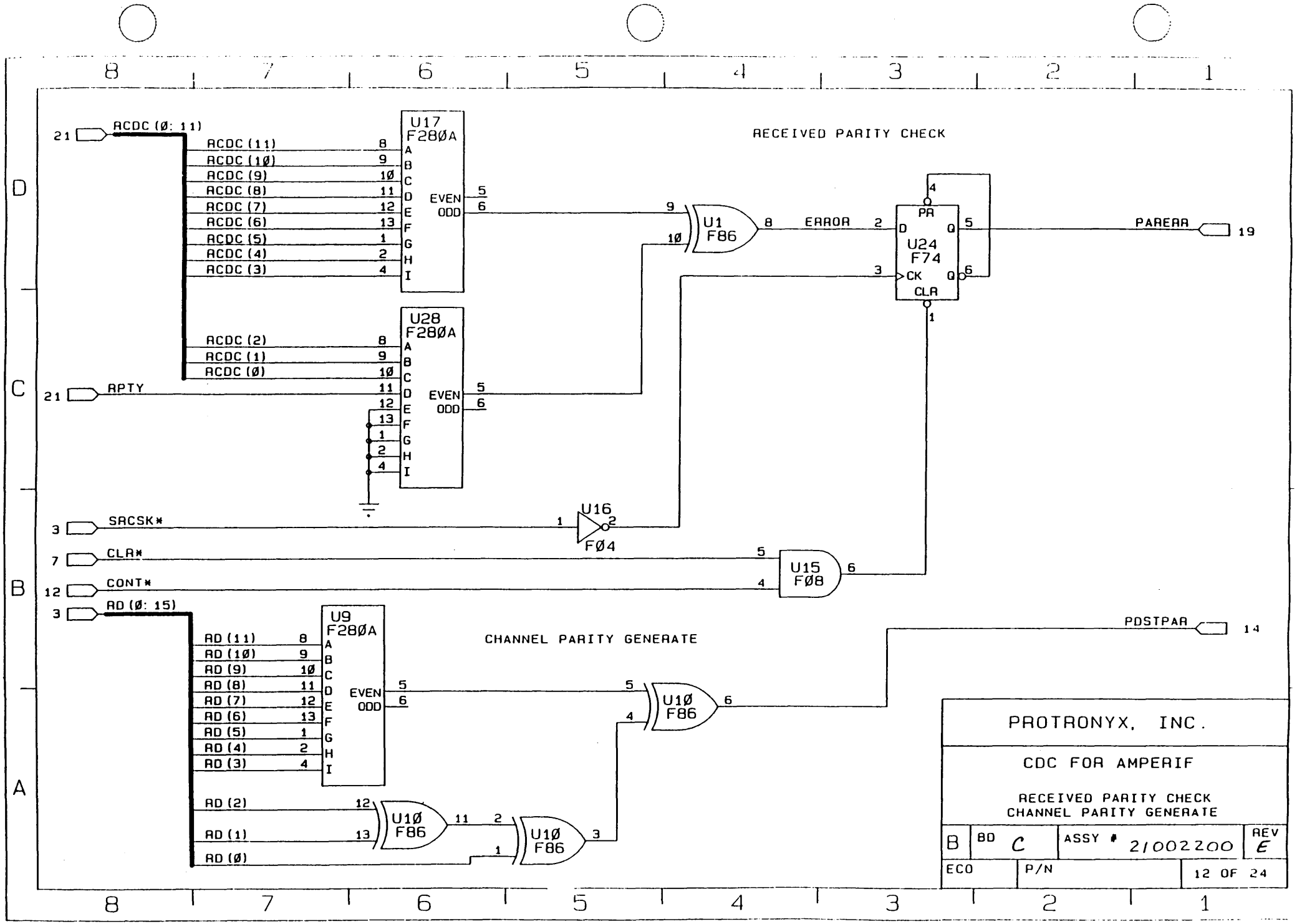
ECO 2555
SH 83



ECO 2582,
SH 84

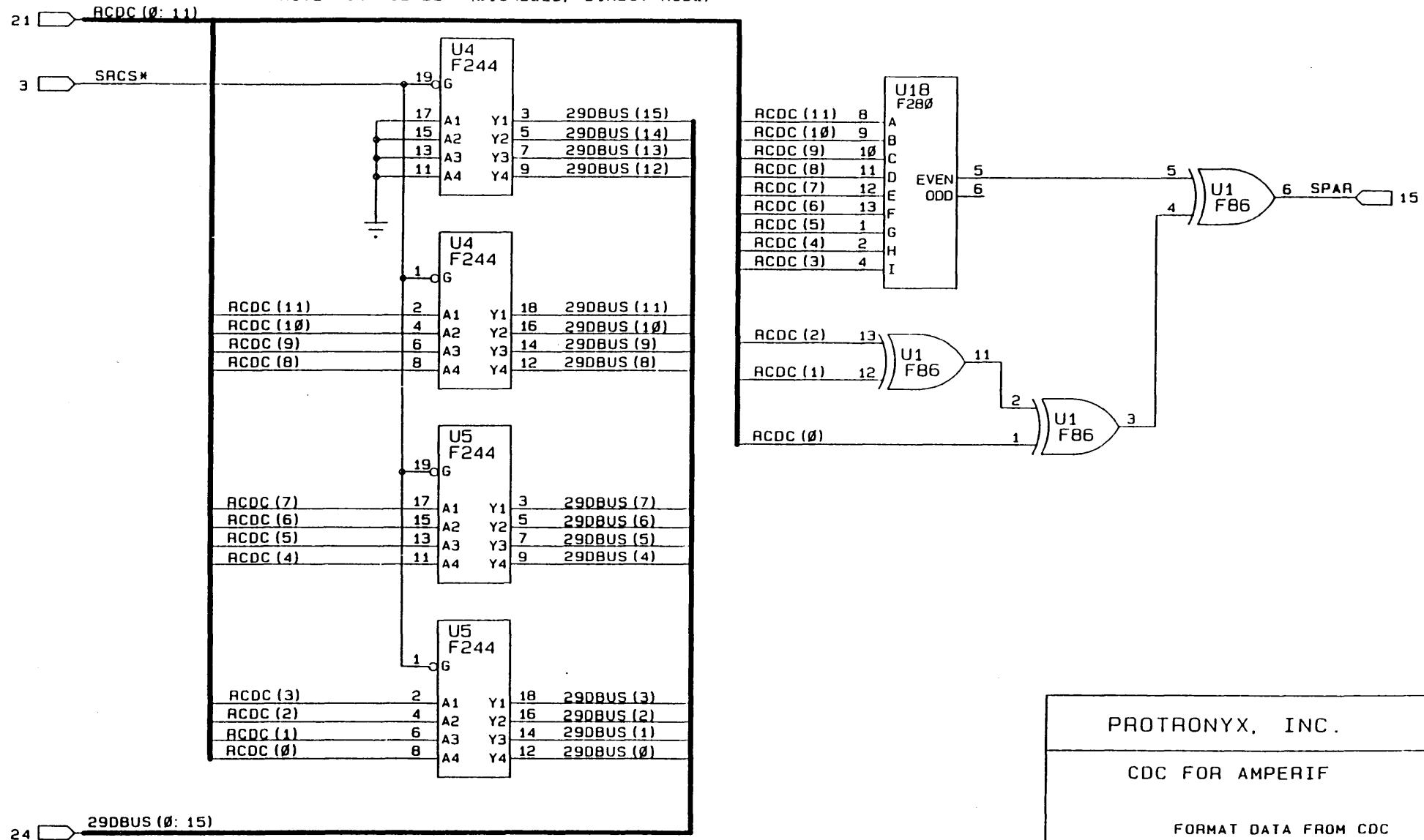


ECO 2585
SH 35


RECEIVED PARITY CHECK
ACDC (Ø: 11)
21
ACDC (11)
ACDC (1Ø)
ACDC (9)
ACDC (8)
ACDC (7)
ACDC (6)
ACDC (5)
ACDC (4)
ACDC (3)
U17
F28ØA
EVEN
ODD
ACDC (2)
ACDC (1)
ACDC (Ø)
U28
F28ØA
APTY
U1
F86
ERROR
U24
F74
PR
CK
CLR
PAREAR
19
SACSK*
U16
FØ4
CLR*
CONT*
U15
FØ8
AD (Ø: 15)
CHANNEL PARITY GENERATE
U9
F28ØA
AD (11)
AD (1Ø)
AD (9)
AD (8)
AD (7)
AD (6)
AD (5)
AD (4)
AD (3)
AD (2)
AD (1)
AD (Ø)
U1Ø
F86
PDSTPAR
14
PROTRONYX, INC.
CDC FOR AMPERIF
RECEIVED PARITY CHECK
CHANNEL PARITY GENERATE
B
BD C
ASSY # 21002200
REV E
ECO
P/N
12 OF 24

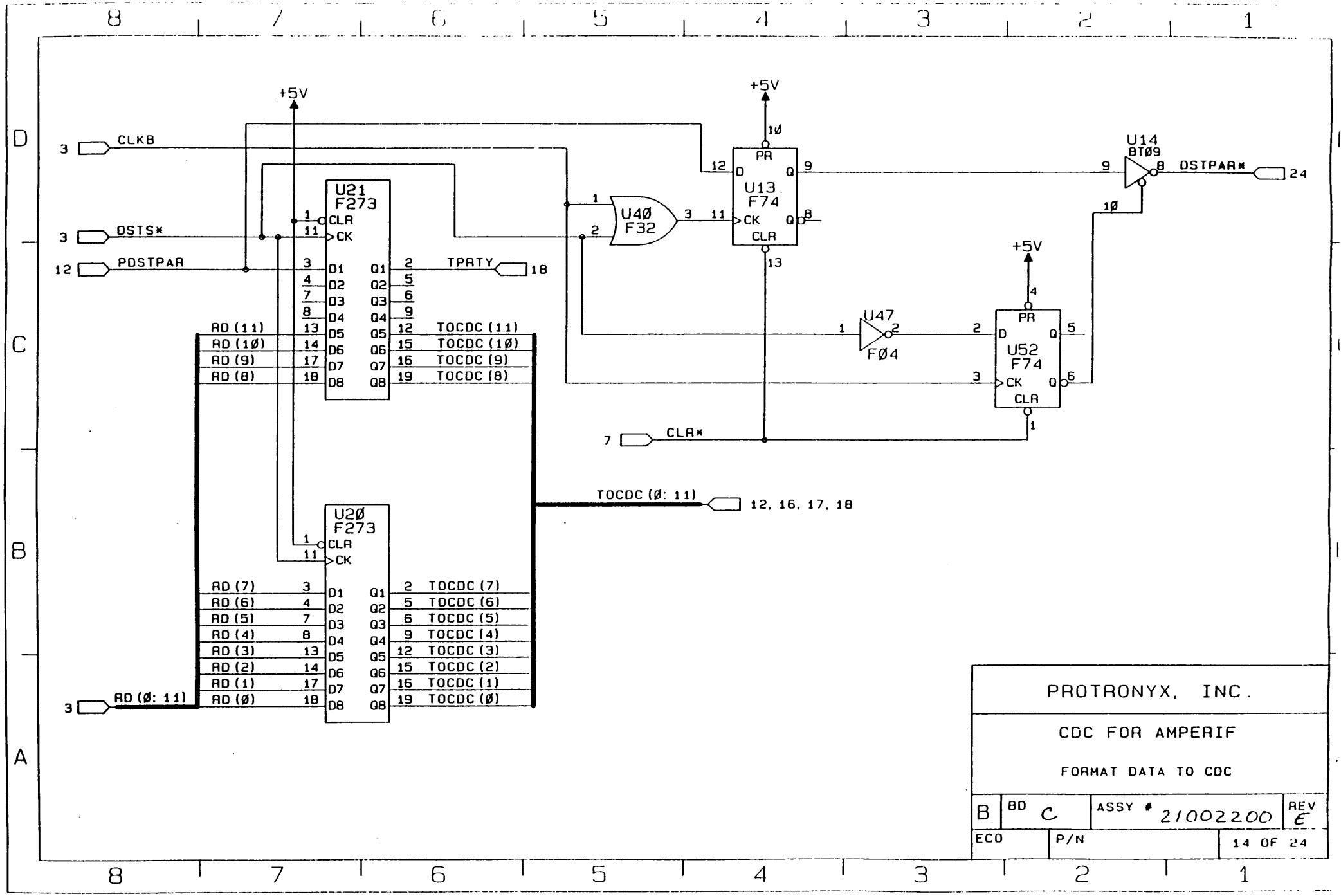
ECO 2555
5/86

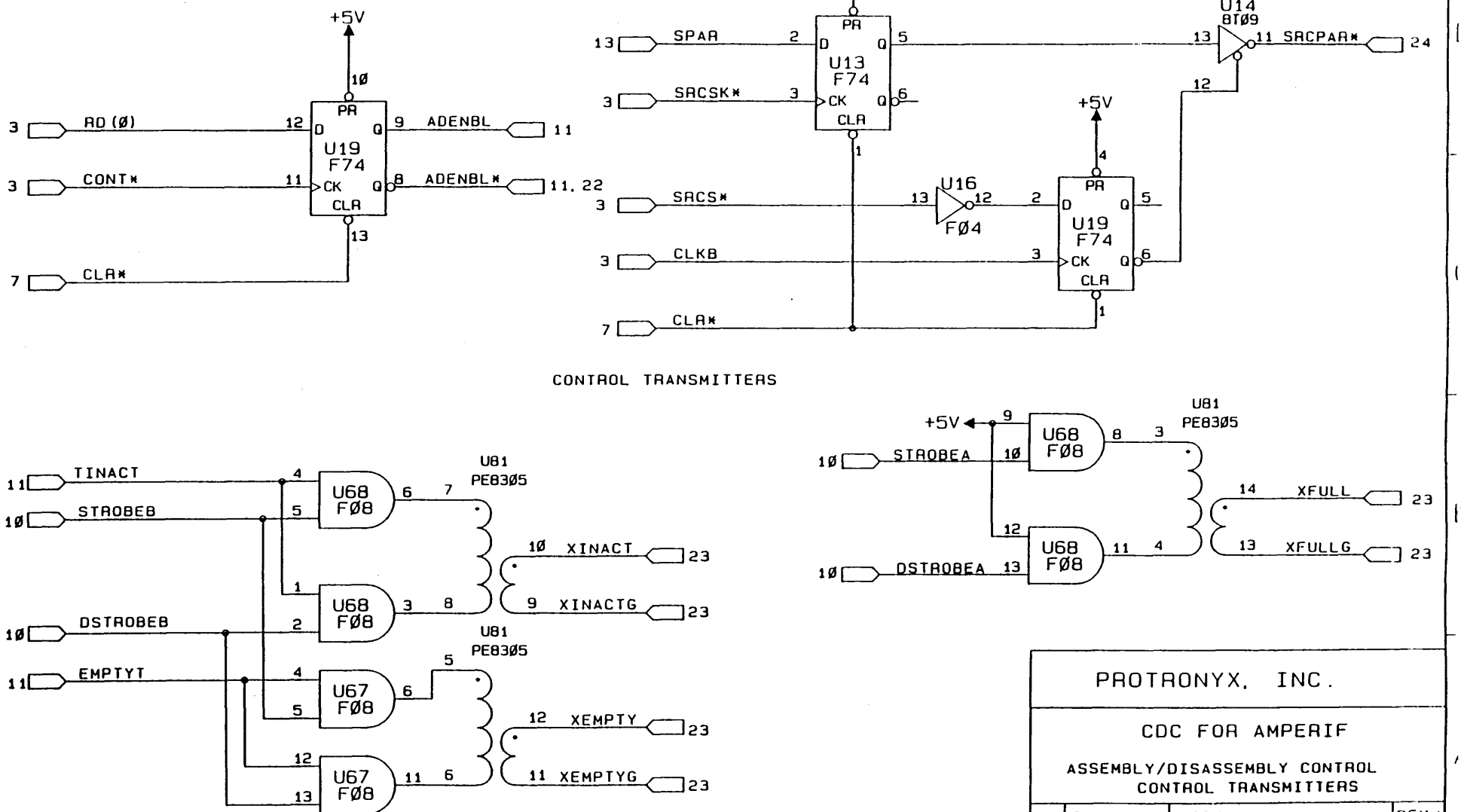
WRITE DISASSEMBLY (DISABLED, DIRECT MODE)



PROTRONYX, INC.			
CDC FOR AMPERIF			
FORMAT DATA FROM CDC			
B	BD C	ASSY # 21002200	REV E
ECO	P/N		13 OF 24

ECO 2545
CH 87


+5V
CLKB
DSTS*
PDSTPAR
U21
F273
CLR
CK
D1
D2
D3
D4
D5
D6
D7
D8
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
TPRTY
AD (11)
AD (10)
AD (9)
AD (8)
TOCDC (11)
TOCDC (10)
TOCDC (9)
TOCDC (8)
U20
F273
AD (7)
AD (6)
AD (5)
AD (4)
AD (3)
AD (2)
AD (1)
AD (0)
AD (0: 11)
TOCDC (7)
TOCDC (6)
TOCDC (5)
TOCDC (4)
TOCDC (3)
TOCDC (2)
TOCDC (1)
TOCDC (0)
TOCDC (0: 11)
12, 16, 17, 18
U40
F32
U13
F74
PR
CK
CLR
U47
F04
U52
F74
U14
8T09
DSTPAR*
CLR*
PROTRONYX, INC.
CDC FOR AMPERIF
FORMAT DATA TO CDC
B
BD C
ASSY # 21002200
REV E
ECO
P/N
14 OF 24



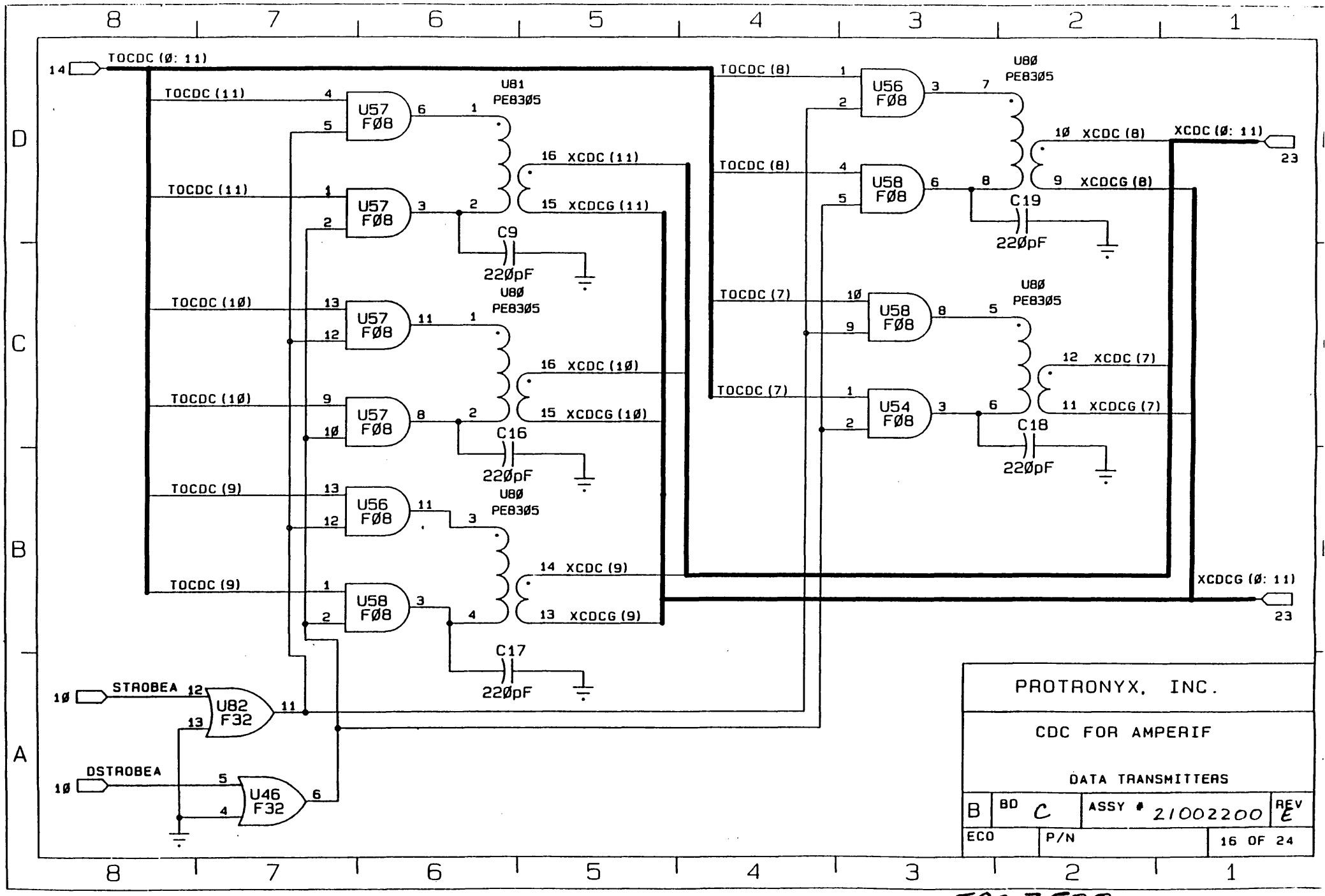
PROTRONYX, INC.

CDC FOR AMPERIF

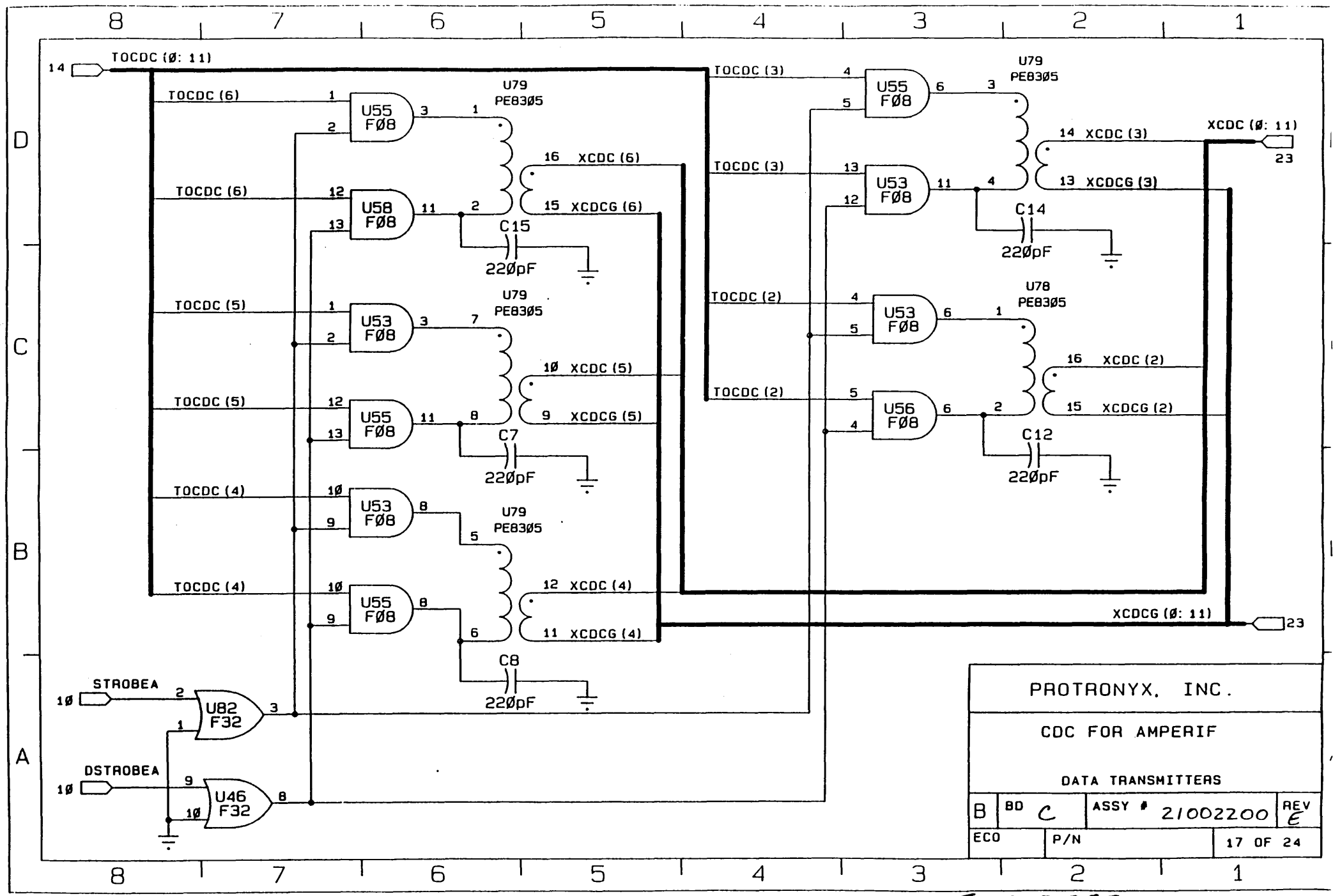
ASSEMBLY/DISASSEMBLY CONTROL
CONTROL TRANSMITTERS

B	BD	ASSY # 21002200	REV E
ECO 129	P/N		15 OF 24

ECO 2585
SH 89



ECO 2588
SH 90



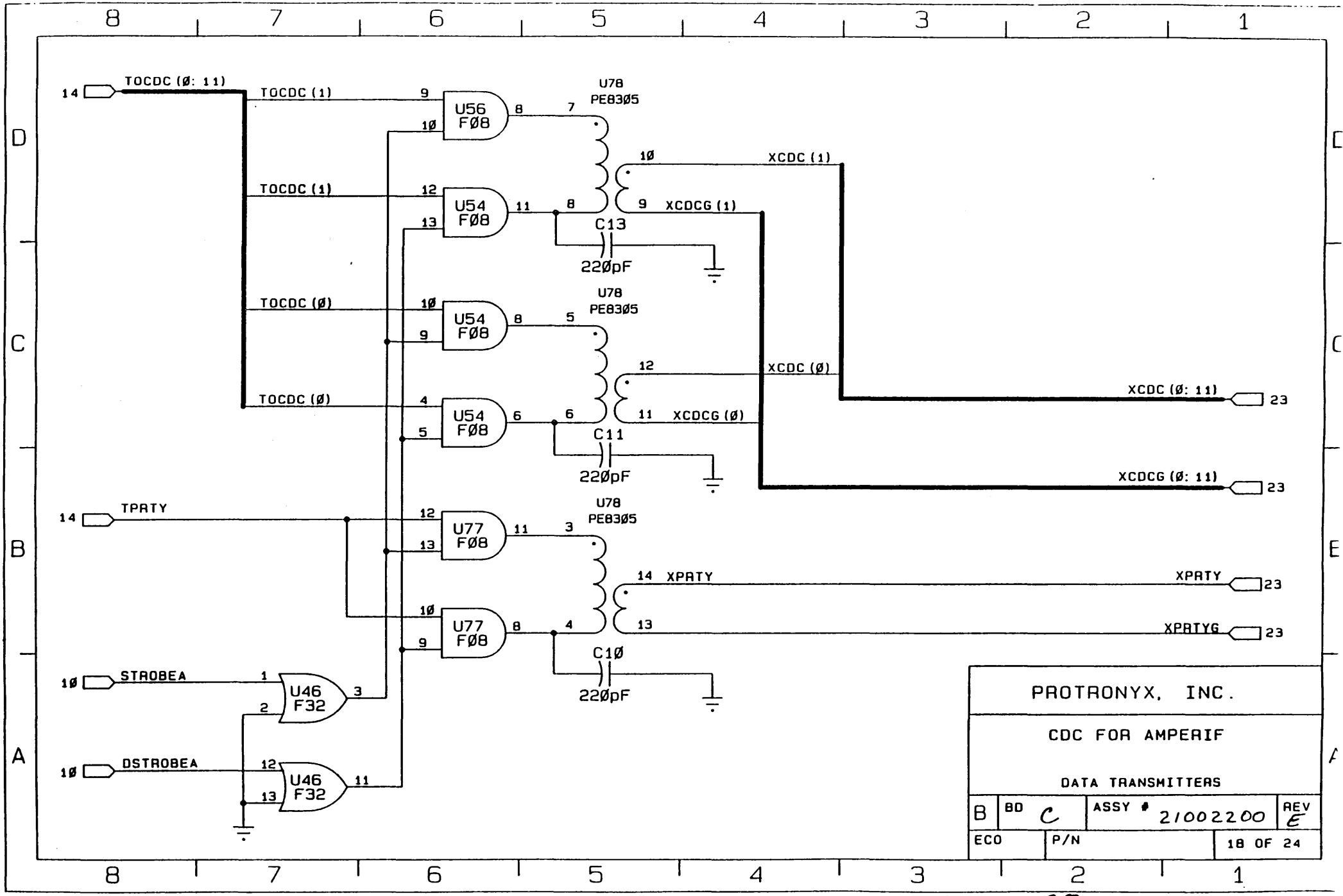
PROTRONYX, INC.

CDC FOR AMPERIF

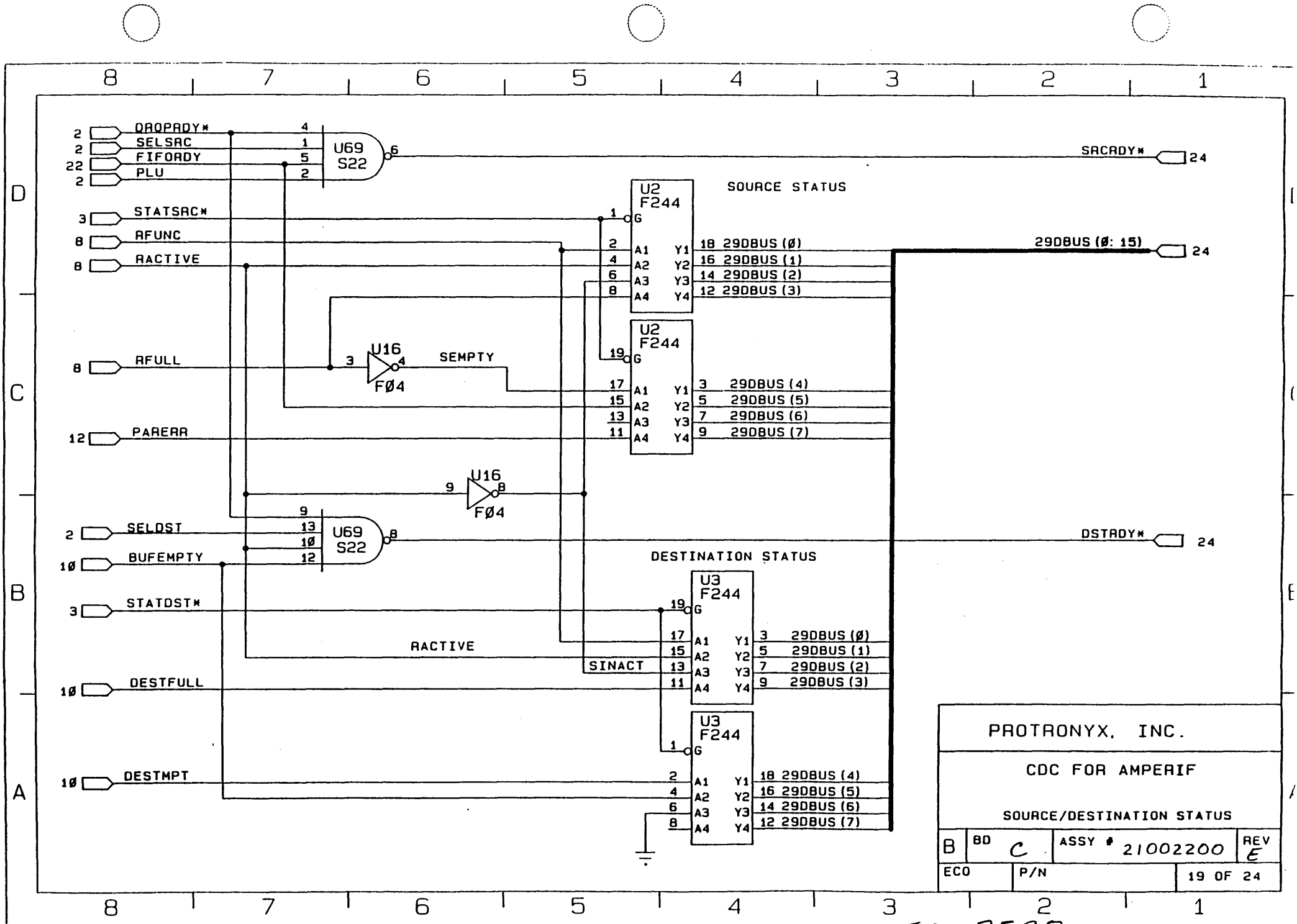
DATA TRANSMITTERS

B	BD C	ASSY # 21002200	REV E
ECO	P/N		17 OF 24

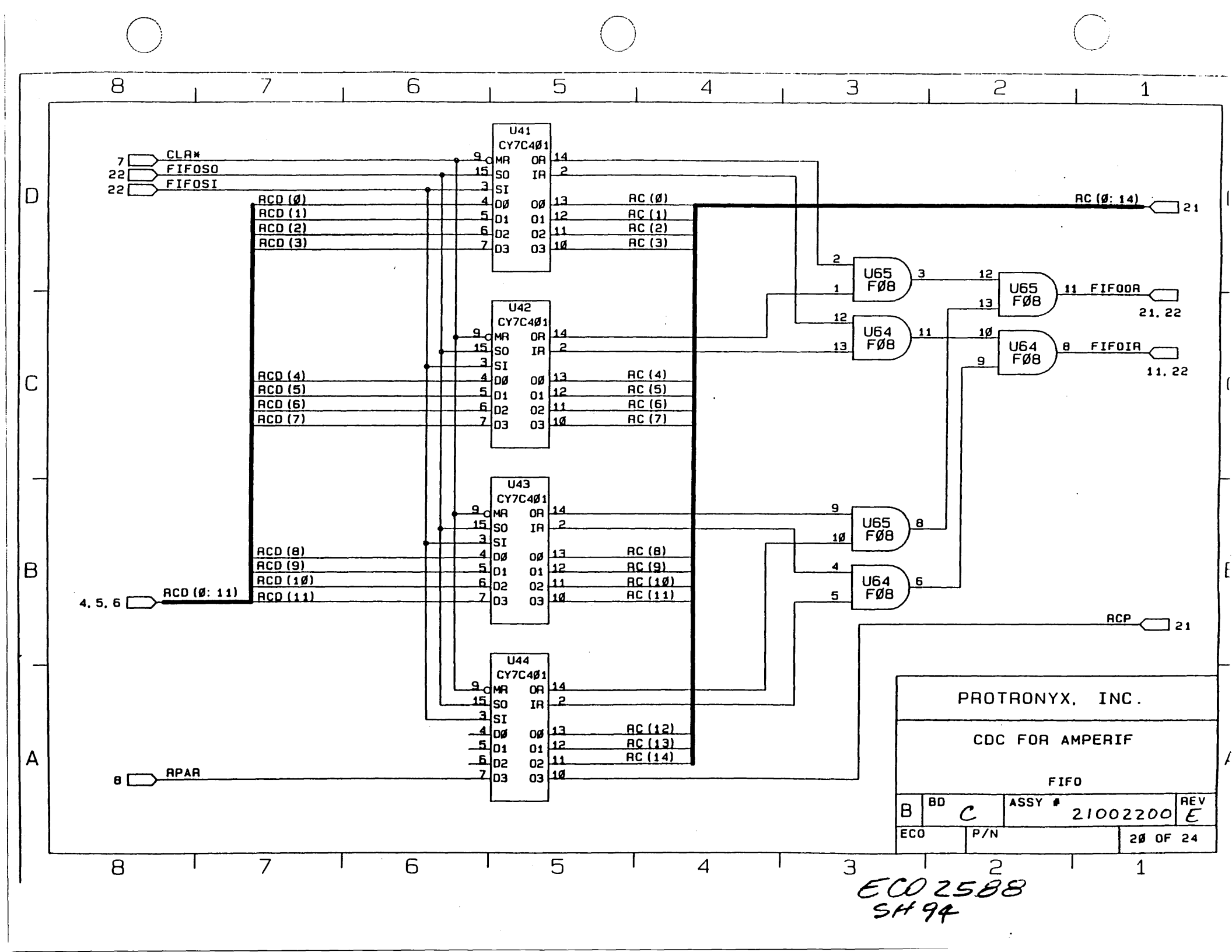
ECO 2588
SH 91

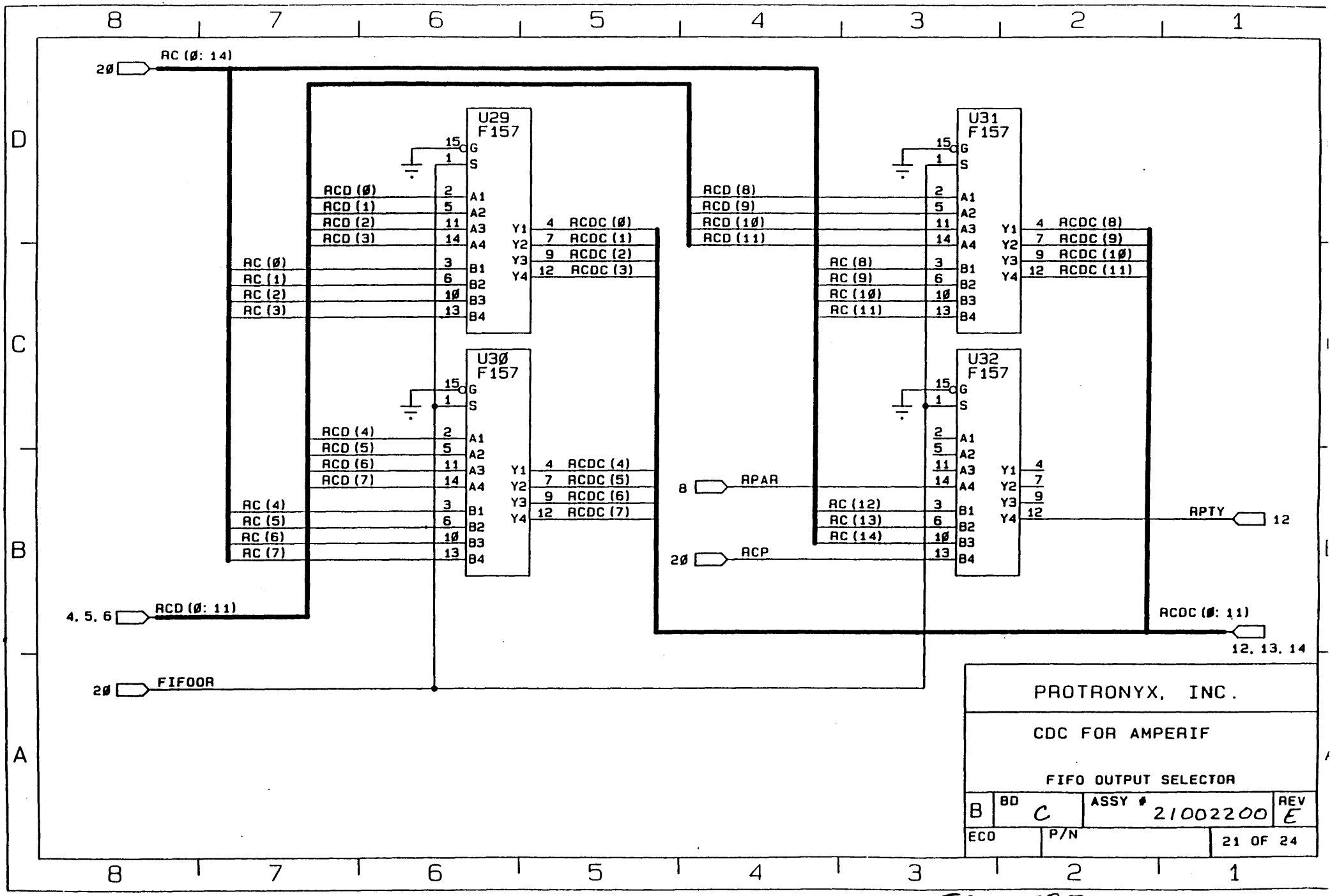


ECO 2588
SH 92



ECO 2588
SH 93


U41
CY7C401
U42
CY7C401
U43
CY7C401
U44
CY7C401
MR
SO
SI
D0
D1
D2
D3
OR
IR
O0
O1
O2
O3
CLR*
FIFOSO
FIFOSI
RCD (0)
RCD (1)
RCD (2)
RCD (3)
RCD (4)
RCD (5)
RCD (6)
RCD (7)
RCD (8)
RCD (9)
RCD (10)
RCD (11)
RCD (0: 11)
APAR
RC (0)
RC (1)
RC (2)
RC (3)
RC (4)
RC (5)
RC (6)
RC (7)
RC (8)
RC (9)
RC (10)
RC (11)
RC (12)
RC (13)
RC (14)
RC (0: 14)
U65 F08
U64 F08
FIFOOR
FIFOIR
21, 22
11, 22
RCP
PROTRONYX, INC.
CDC FOR AMPERIF
FIFO
B
BD C
ASSY # 21002200
REV E
ECO
P/N
20 OF 24
ECO 2588
SH 9R



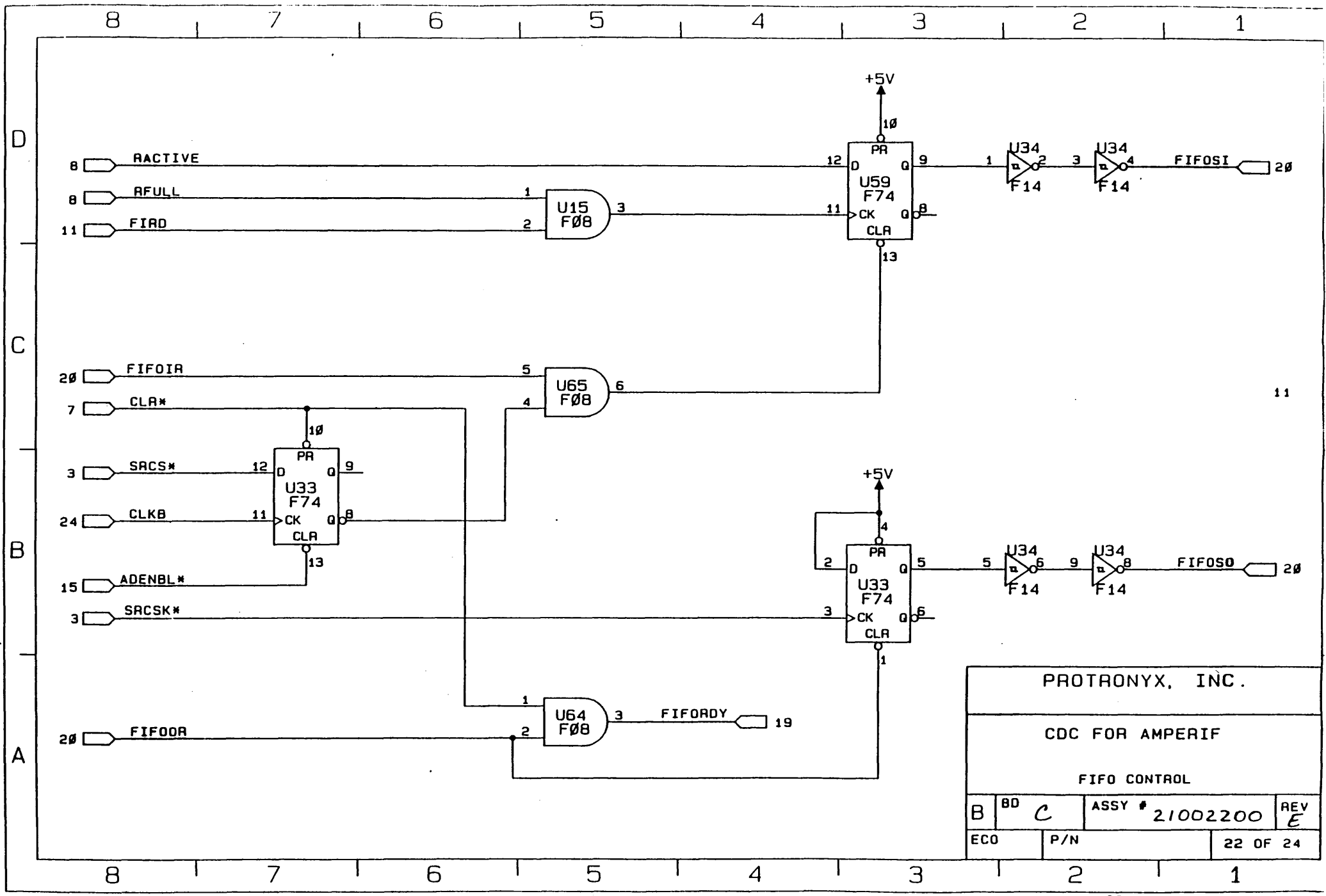
PROTRONYX, INC.

CDC FOR AMPERIF

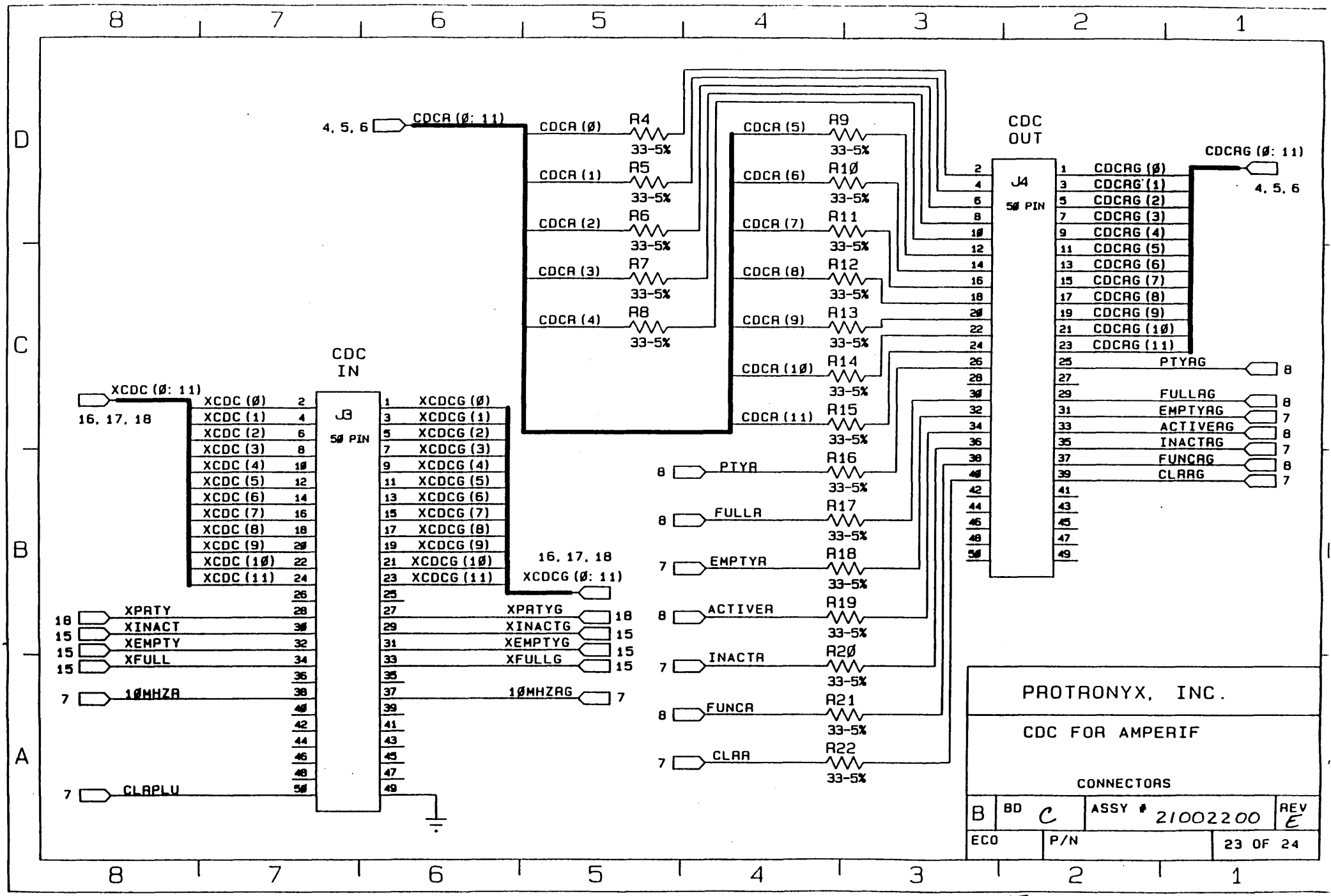
FIFO OUTPUT SELECTOR

B	BD C	ASSY # 21002200	REV E
ECO	P/N		21 OF 24

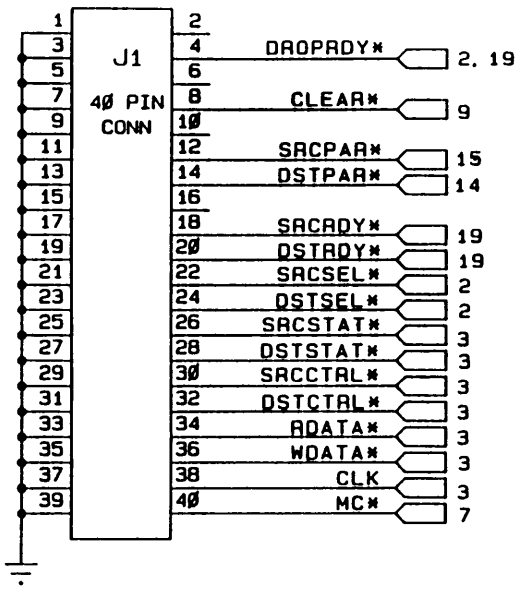
ECO 2588
SH 95

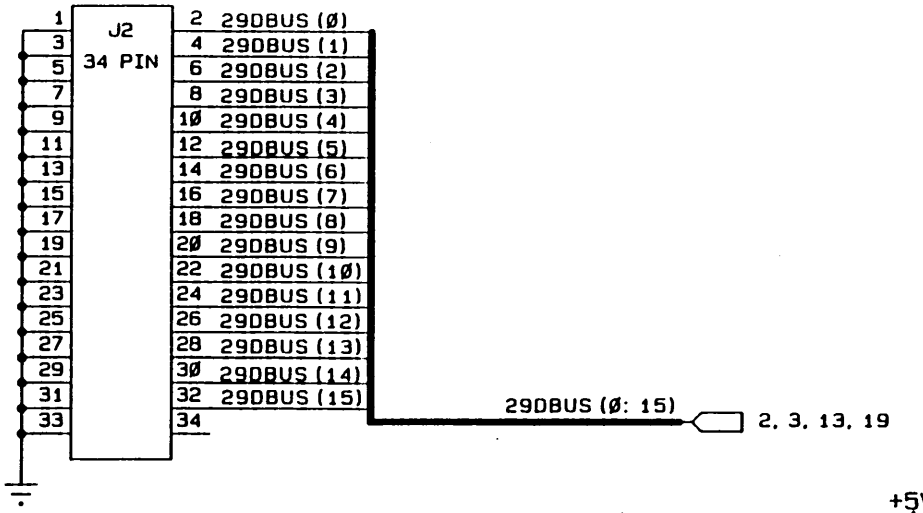


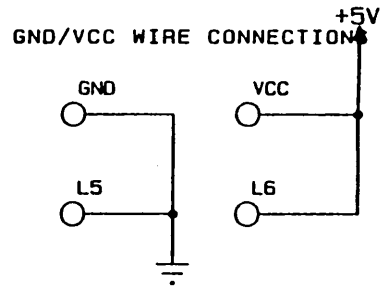
ECO 2588
SH 96

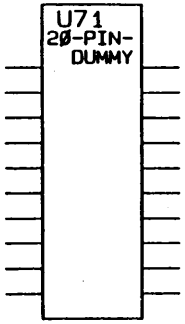


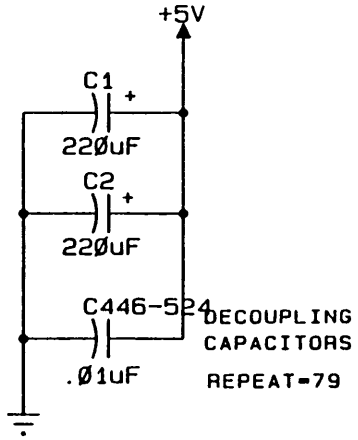
ECO 2588
SH 97











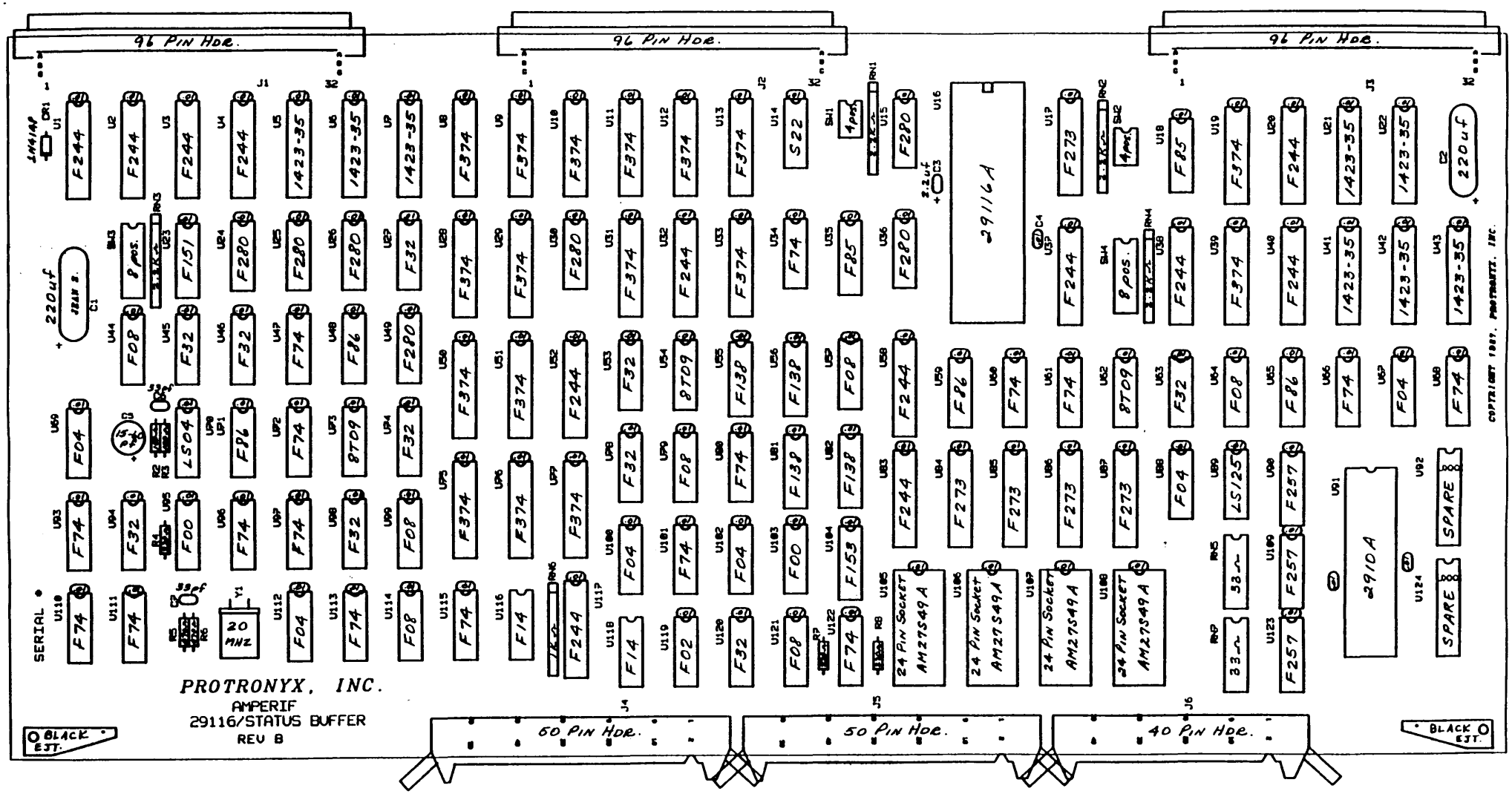
PROTRONYX, INC.			
CDC FOR AMPERIF			
J1, J2 CONNECTORS			
B	BD C	ASSY # 21002200	REV E
ECO	P/N		24 OF 24

ECO-2588
SH 98

ECO 2588
SH 34

REWORK PER ECO 135

Assembly 21002100
Rev. B (Board) 11/25/87
Rev. ~~B~~ C (Assembly)

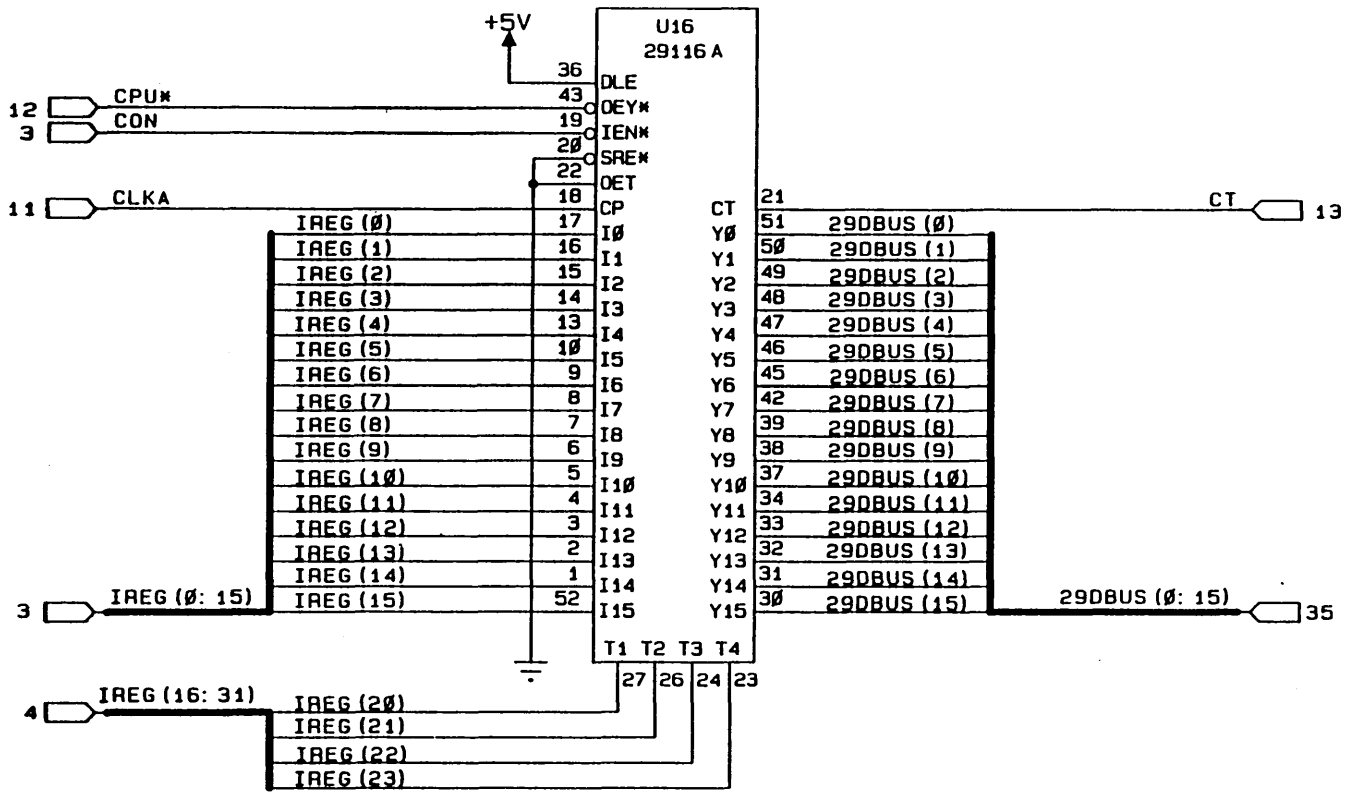


SEE ECO 135

PROTRONYX, INC.			
29116 FOR AMPERIF			
REVISION HISTORY			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		1 OF 35

PROTRONYX, INC.
COPYRIGHT, 1987

ECO 2588
SH 35

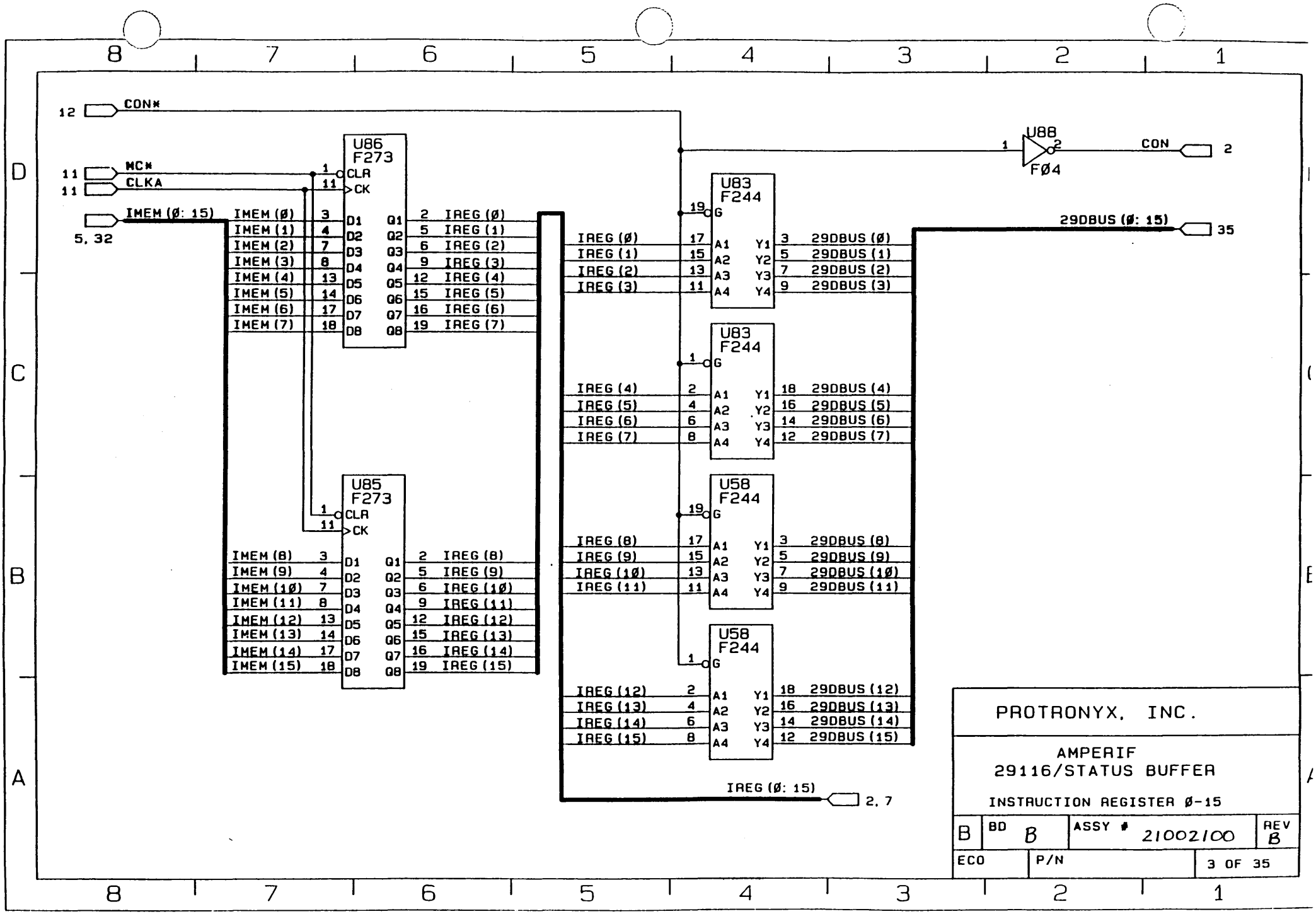


NOTES:

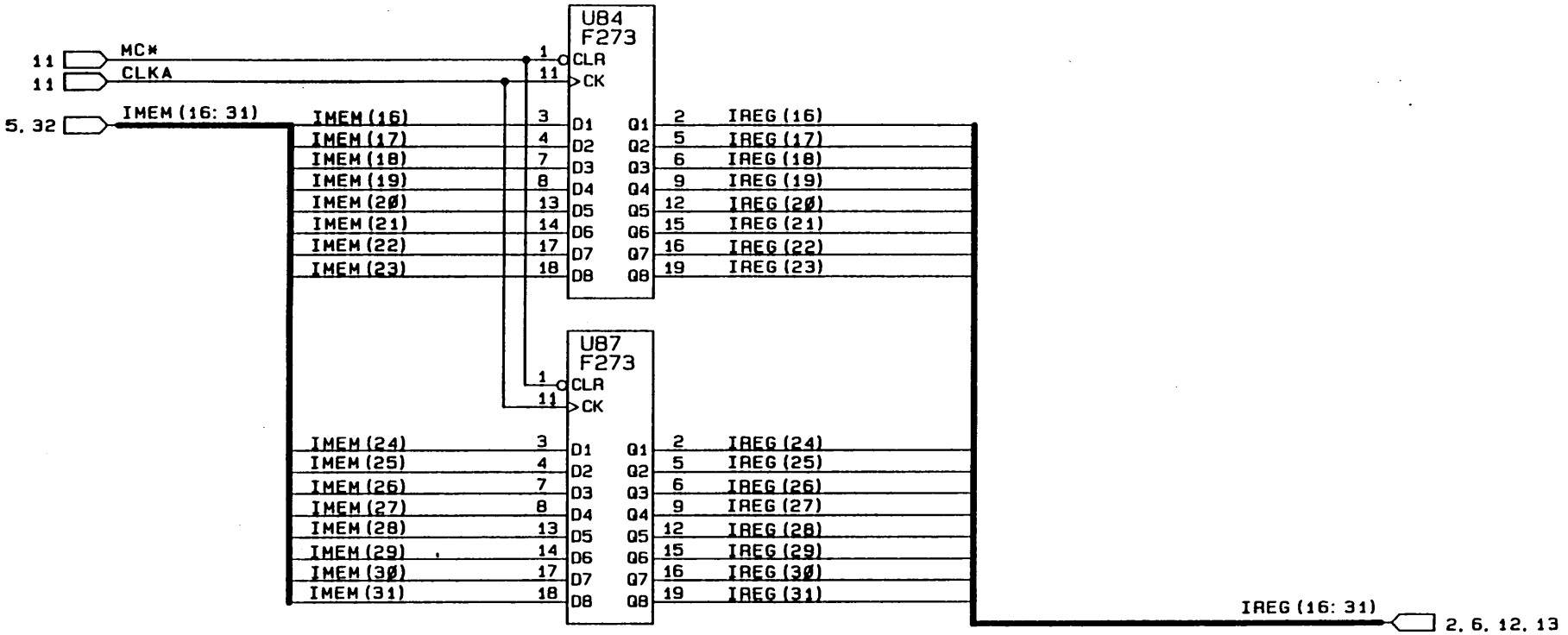
1. C3 AND C4 ARE PLACED BETWEEN VCC AND GND ON U16.
2. U16 - PINS 12, 40, 41 ARE VCC.
3. U16 - PINS 11, 25, 35, 44 ARE GND.

PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER			
HIGH SPEED PROCESSOR			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		2 OF 35

ECO 2588
SH 36

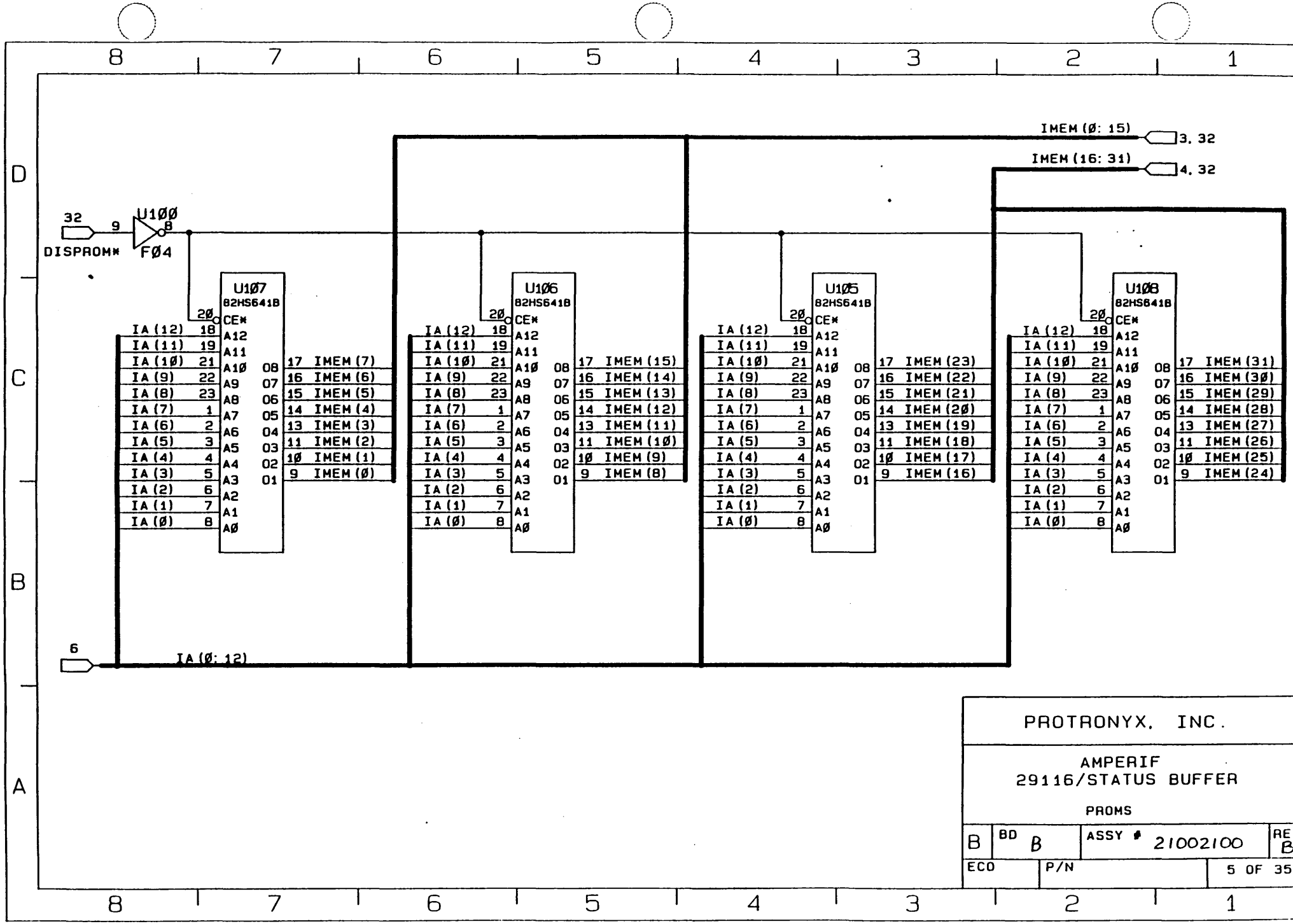

12 CON*
11 MC*
11 CLKA
IMEM (Ø: 15)
5, 32
U86 F273
U85 F273
CLR
CK
IMEM (Ø) IMEM (1) IMEM (2) IMEM (3) IMEM (4) IMEM (5) IMEM (6) IMEM (7)
IREG (Ø) IREG (1) IREG (2) IREG (3) IREG (4) IREG (5) IREG (6) IREG (7)
IMEM (8) IMEM (9) IMEM (1Ø) IMEM (11) IMEM (12) IMEM (13) IMEM (14) IMEM (15)
IREG (8) IREG (9) IREG (1Ø) IREG (11) IREG (12) IREG (13) IREG (14) IREG (15)
U88 FØ4
CON 2
U83 F244
U58 F244
G
A1 A2 A3 A4
Y1 Y2 Y3 Y4
29DBUS (Ø: 15) 35
29DBUS (Ø) 29DBUS (1) 29DBUS (2) 29DBUS (3) 29DBUS (4) 29DBUS (5) 29DBUS (6) 29DBUS (7) 29DBUS (8) 29DBUS (9) 29DBUS (1Ø) 29DBUS (11) 29DBUS (12) 29DBUS (13) 29DBUS (14) 29DBUS (15)
IREG (Ø: 15) 2, 7
PROTRONYX, INC.
AMPERIF
29116/STATUS BUFFER
INSTRUCTION REGISTER Ø-15
B BD B ASSY # 21002100 REV B
ECO P/N 3 OF 35

ECO 2588
SH 37


U84
F273
U87
F273
11 MC*
11 CLKA
5, 32 IMEM (16: 31)
1 CLR
11 CK
IMEM (16) 3 D1 Q1 2 IREG (16)
IMEM (17) 4 D2 Q2 5 IREG (17)
IMEM (18) 7 D3 Q3 6 IREG (18)
IMEM (19) 8 D4 Q4 9 IREG (19)
IMEM (20) 13 D5 Q5 12 IREG (20)
IMEM (21) 14 D6 Q6 15 IREG (21)
IMEM (22) 17 D7 Q7 16 IREG (22)
IMEM (23) 18 D8 Q8 19 IREG (23)
IMEM (24) 3 D1 Q1 2 IREG (24)
IMEM (25) 4 D2 Q2 5 IREG (25)
IMEM (26) 7 D3 Q3 6 IREG (26)
IMEM (27) 8 D4 Q4 9 IREG (27)
IMEM (28) 13 D5 Q5 12 IREG (28)
IMEM (29) 14 D6 Q6 15 IREG (29)
IMEM (30) 17 D7 Q7 16 IREG (30)
IMEM (31) 18 D8 Q8 19 IREG (31)
IREG (16: 31) 2, 6, 12, 13

PROTRONYX INC.			
AMPERIF 29116/STATUS BUFFER			
INSTRUCTION REGISTER 16 - 31			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		4 OF 35

ECO 2588
SH 38



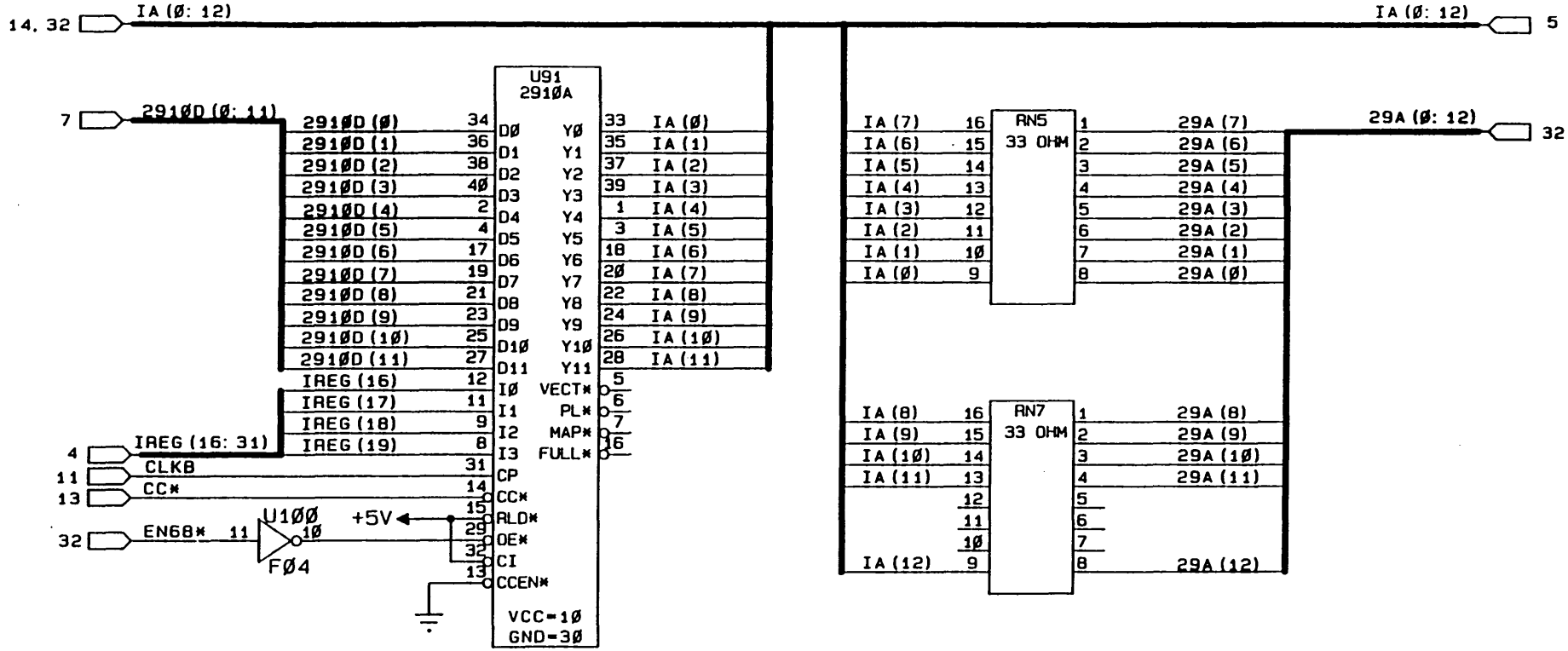
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

PROMS

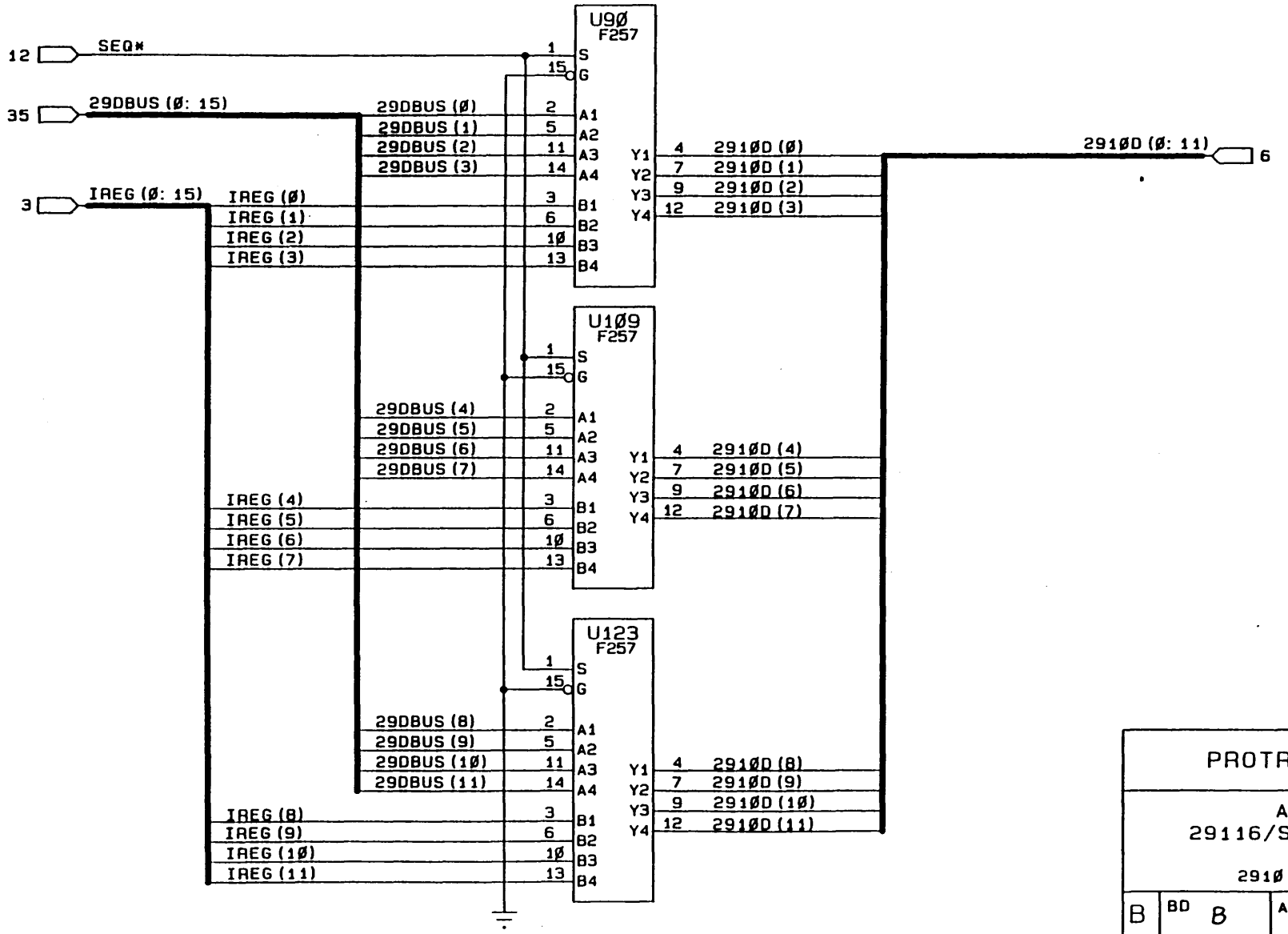
B	BD B	ASSY # 21002100	REV B
ECO	P/N		5 OF 35

ECO 2588
SH 39



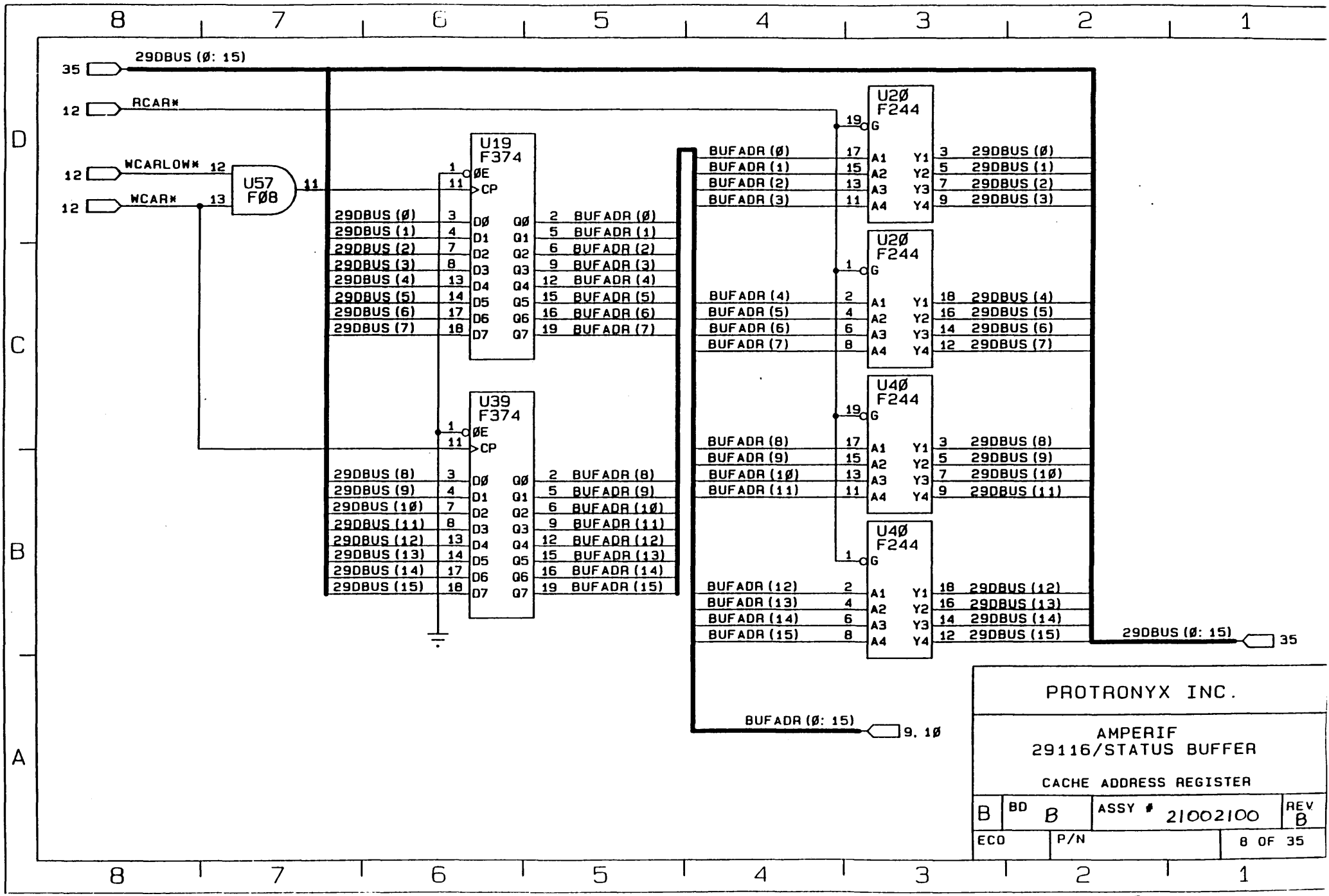
PROTRONYX INC.			
AMPERIF 29116/STATUS BUFFER PROGRAM SEQUENCER			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		6 OF 35

ECO 2588
SH 40



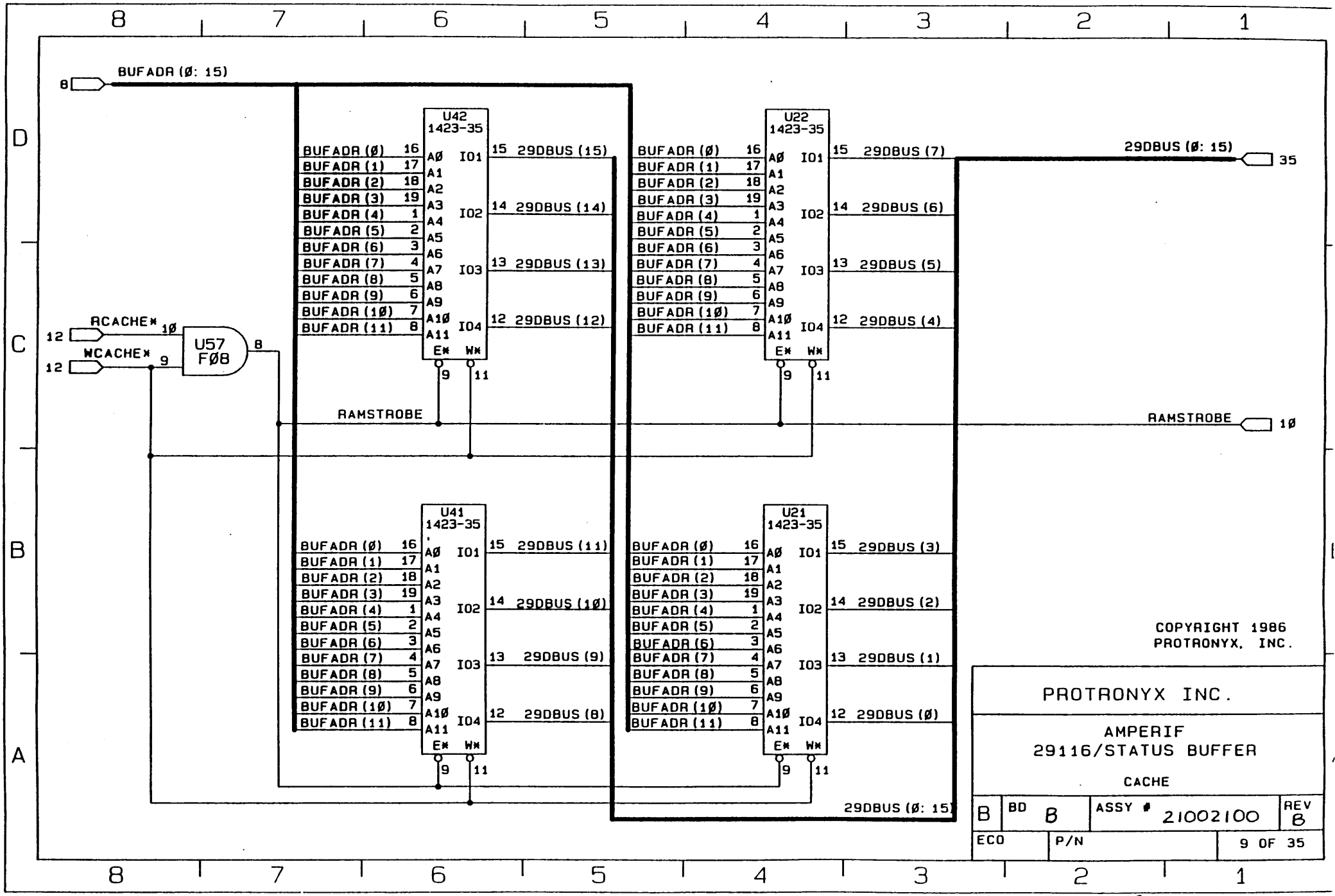
PROTRONYX INC.			
AMPERIF 29116/STATUS BUFFER 2910 ADDRESS MUX			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		7 OF 35

ECO 2588
SH 41



PROTRONYX INC.			
AMPERIF 29116/STATUS BUFFER			
CACHE ADDRESS REGISTER			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		8 OF 35

ECO 2588
SH 42



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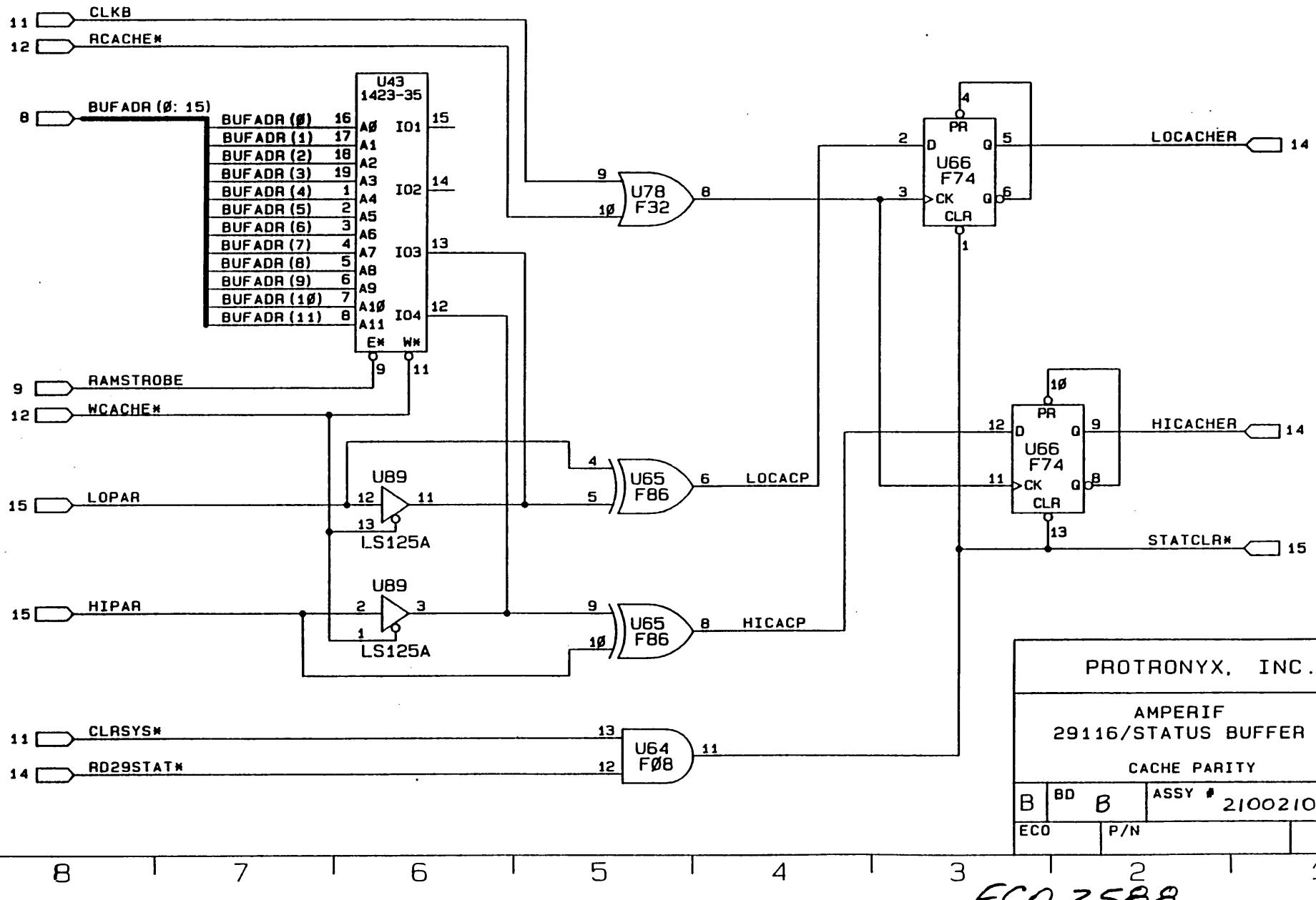
PROTRONYX INC.

AMPERIF
29116/STATUS BUFFER

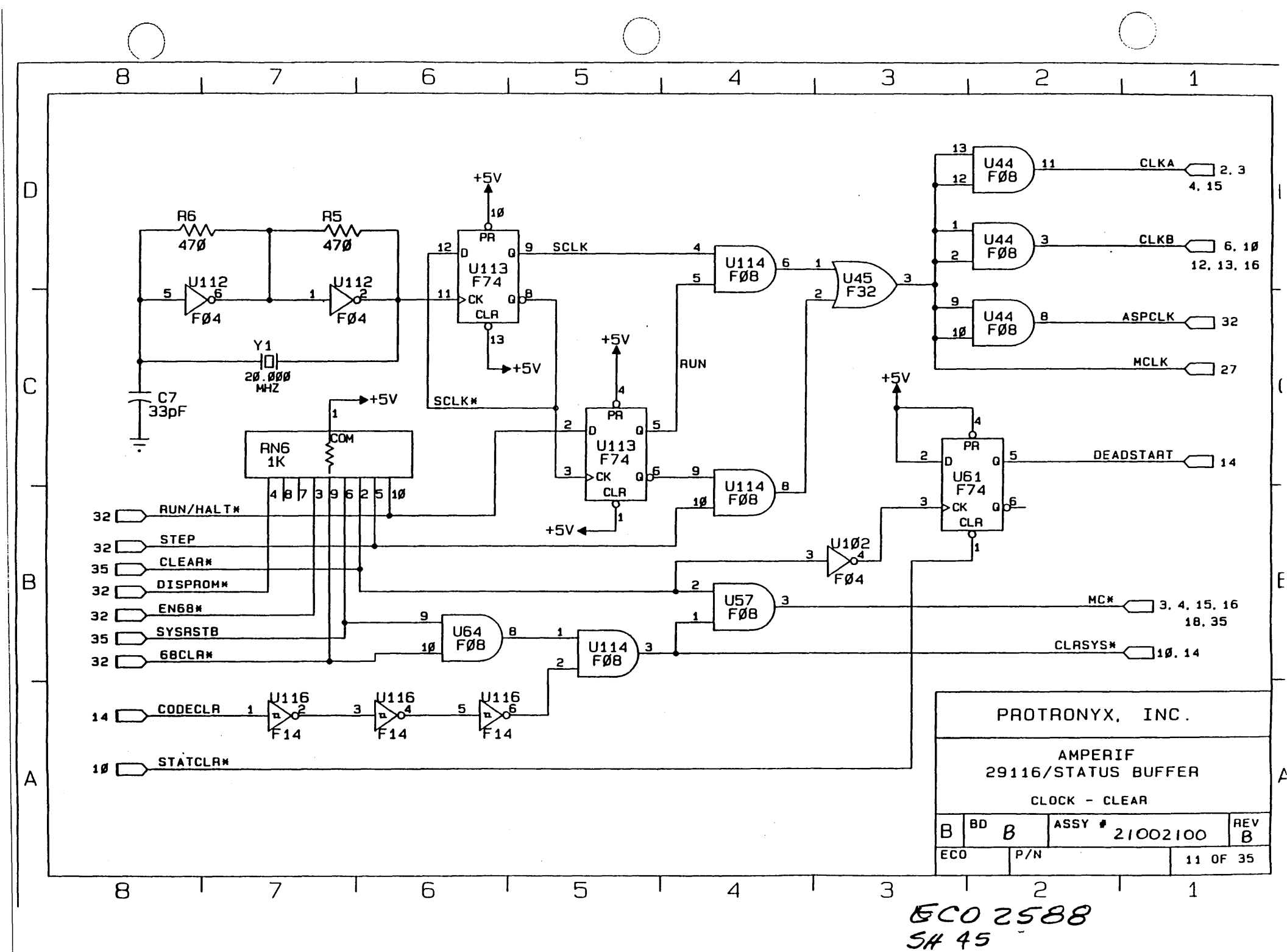
CACHE

B	BD B	ASSY # 21002100	REV B
ECO	P/N		9 OF 35

ECO 2588
SH 43



ECO 2588
SH 44



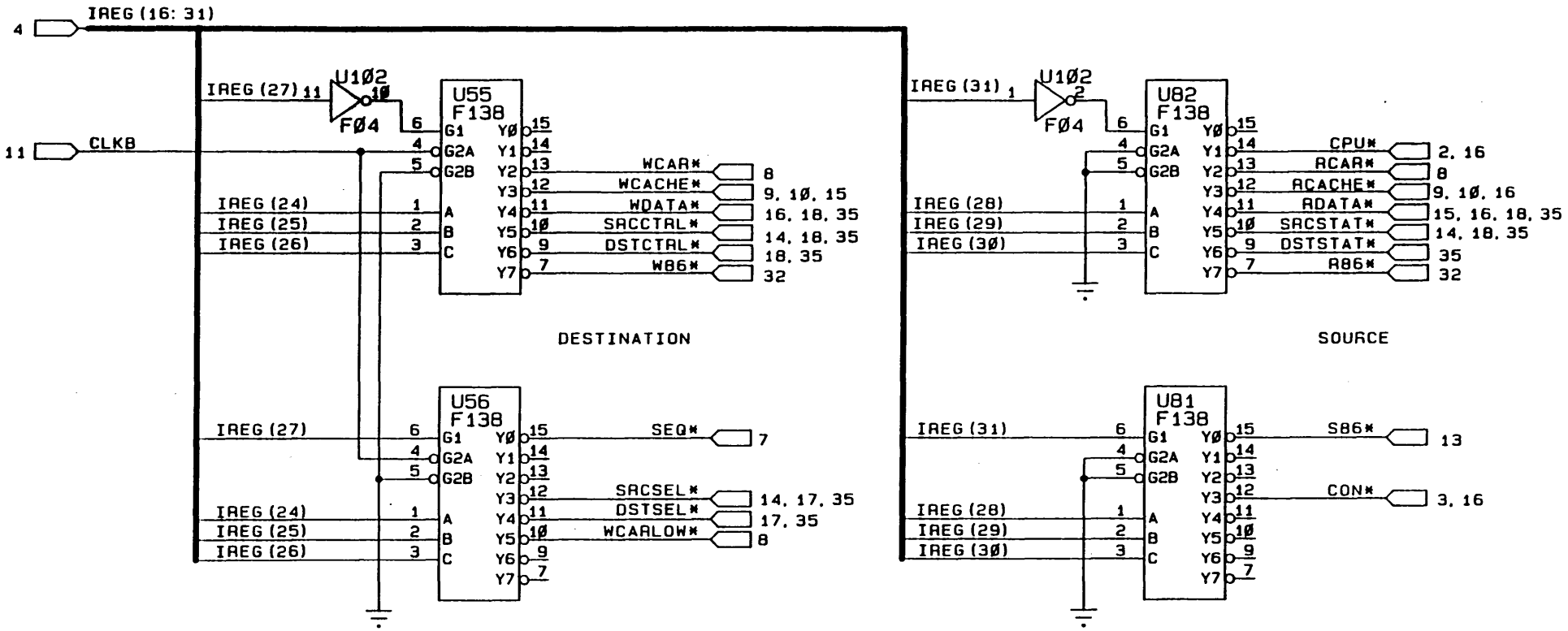
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

CLOCK - CLEAR

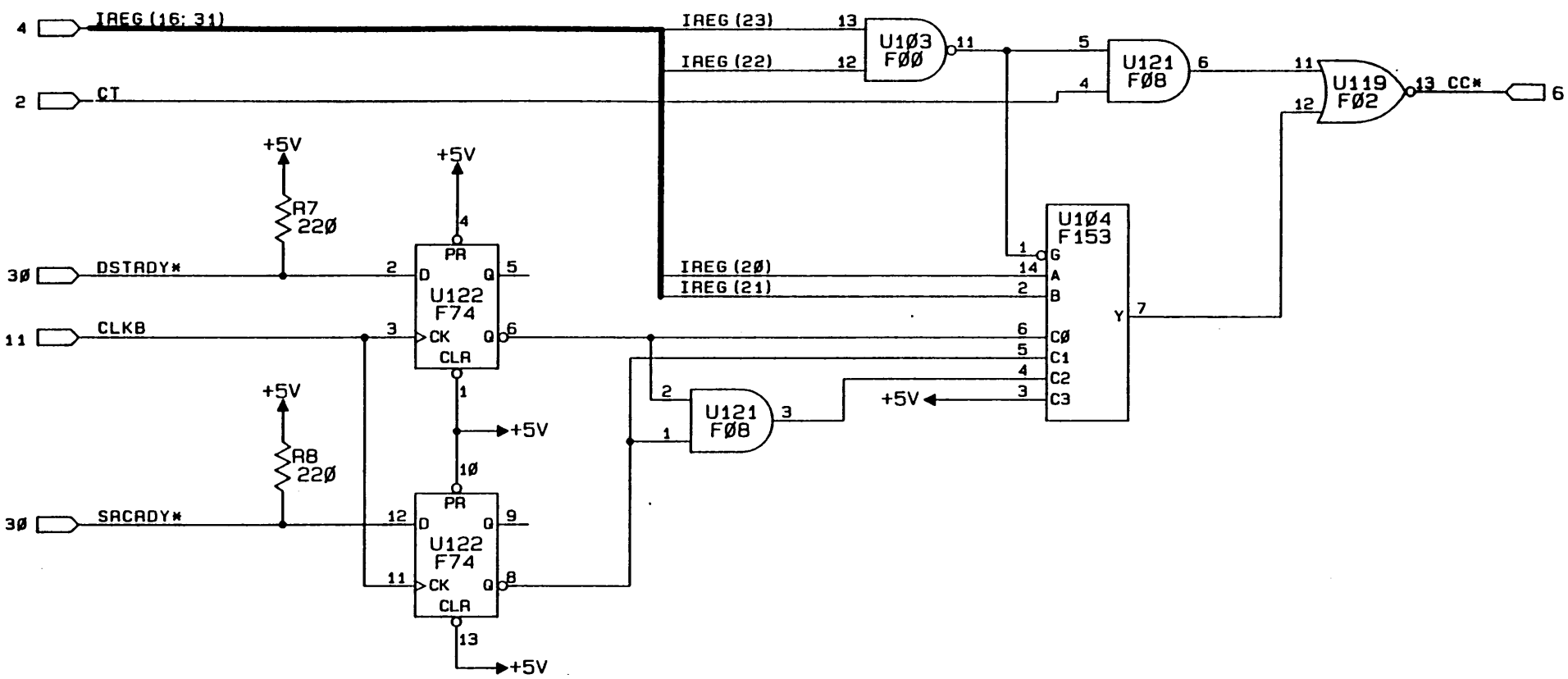
B	BD B	ASSY # 21002100	REV B
ECO	P/N		11 OF 35

ECO 2588
SH 45



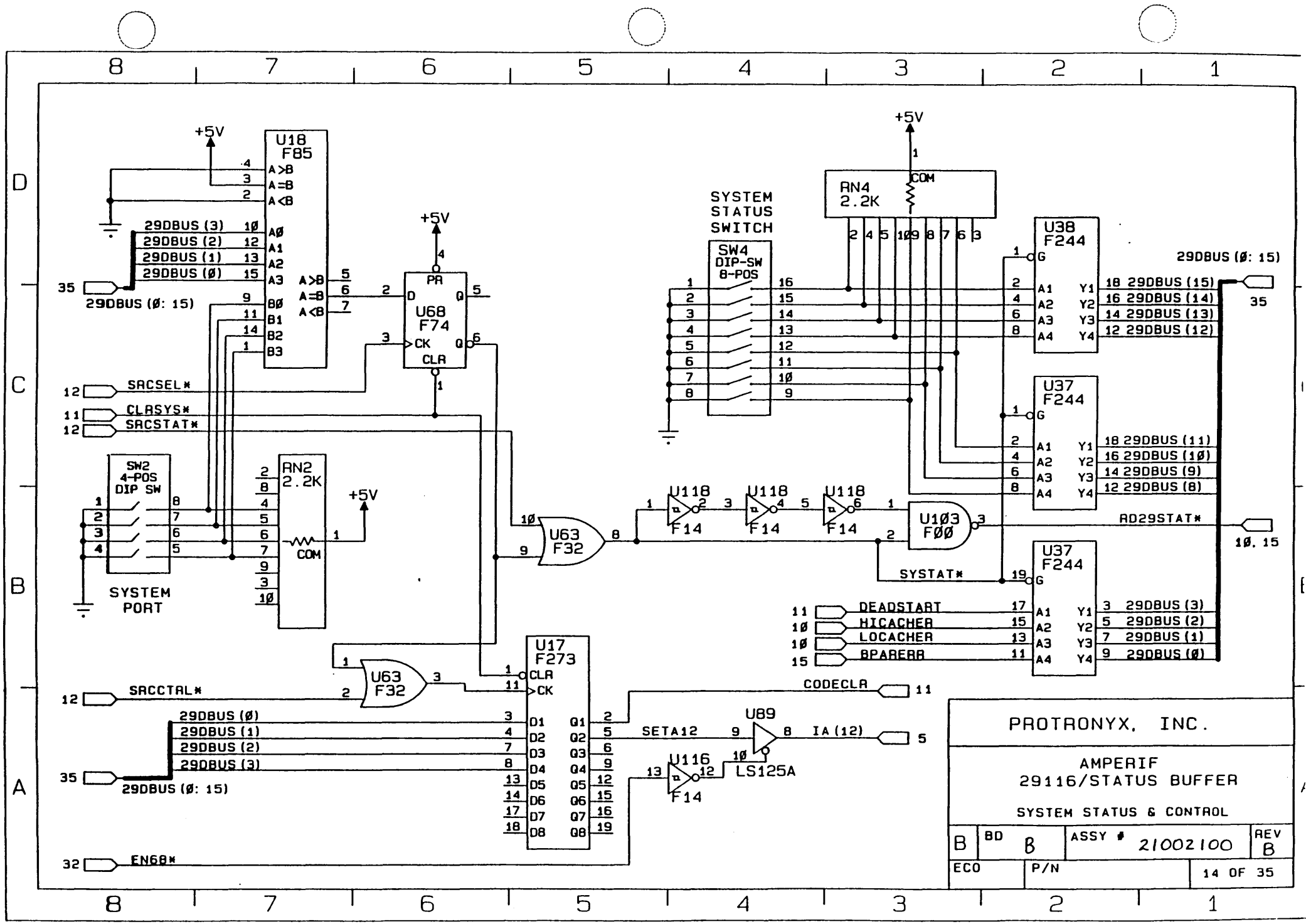
PROTRONYX INC.			
AMPERIF 29116/STATUS BUFFER			
BUS SRC/DST DECODER			
B	BD B	ASSY # 21002100	REV B
ECO 127	P/N		12 OF 35

ECO 2588
SH 46

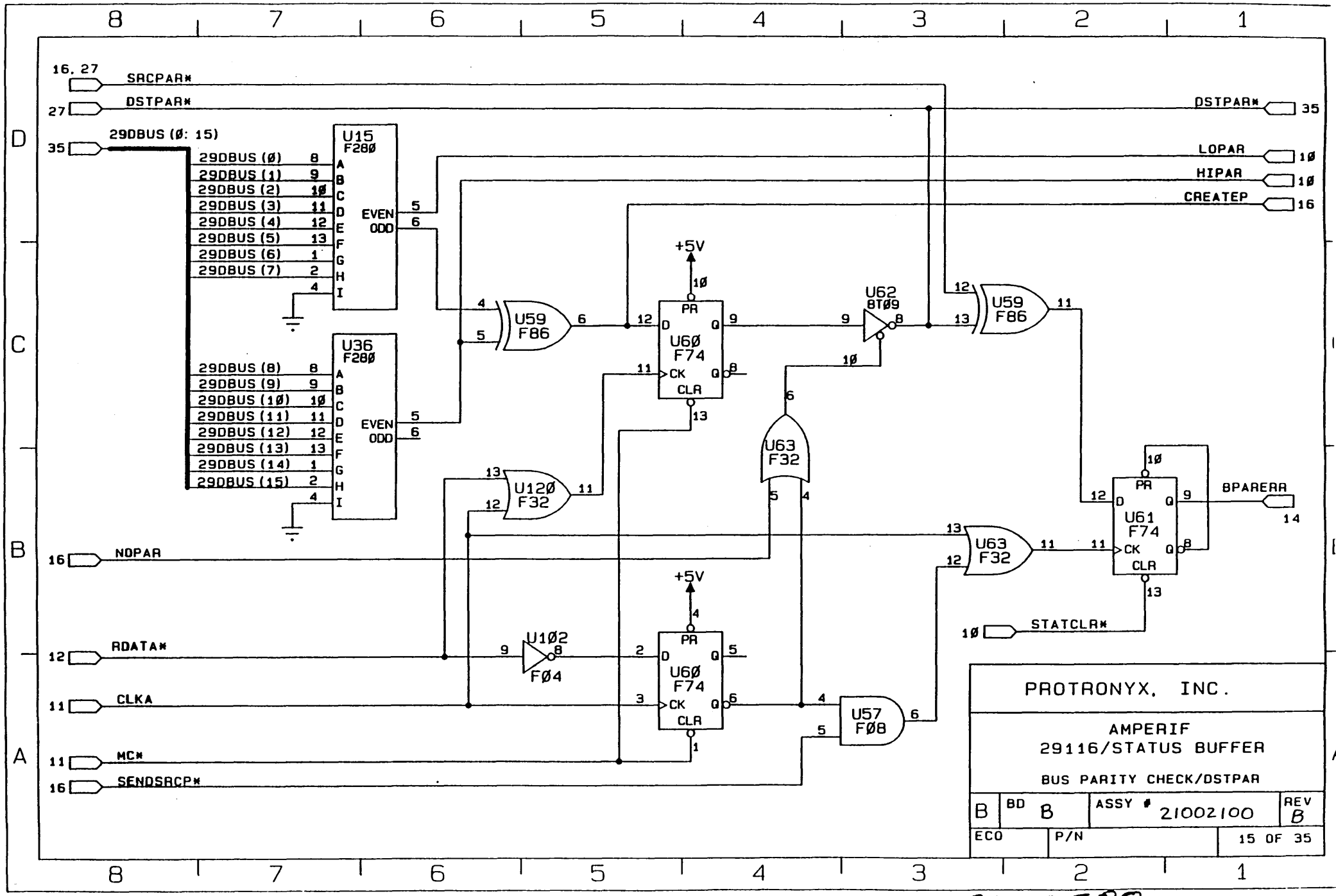


PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER			
CONDITION CODE			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		13 OF 35

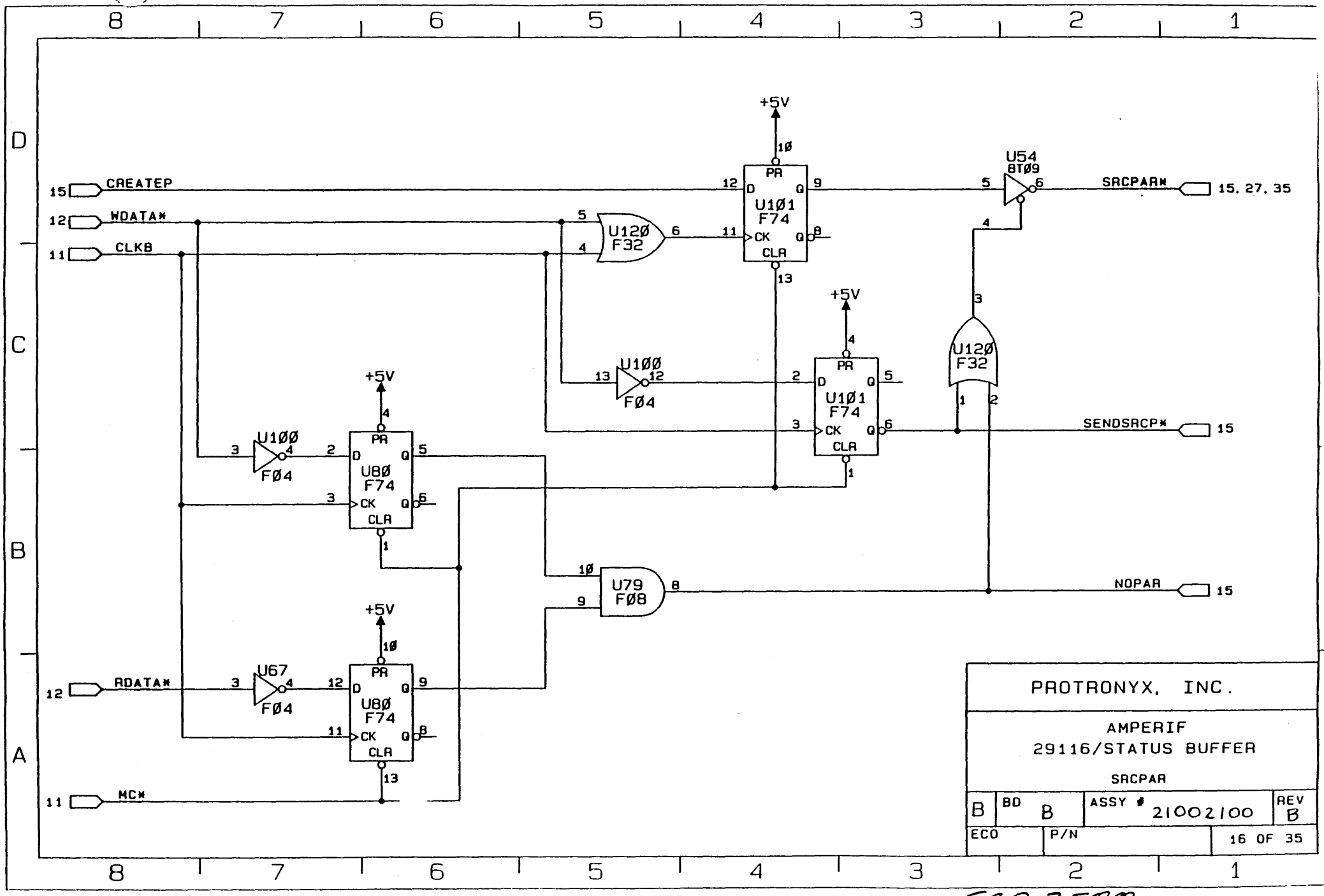
ECO 2588
SH 47



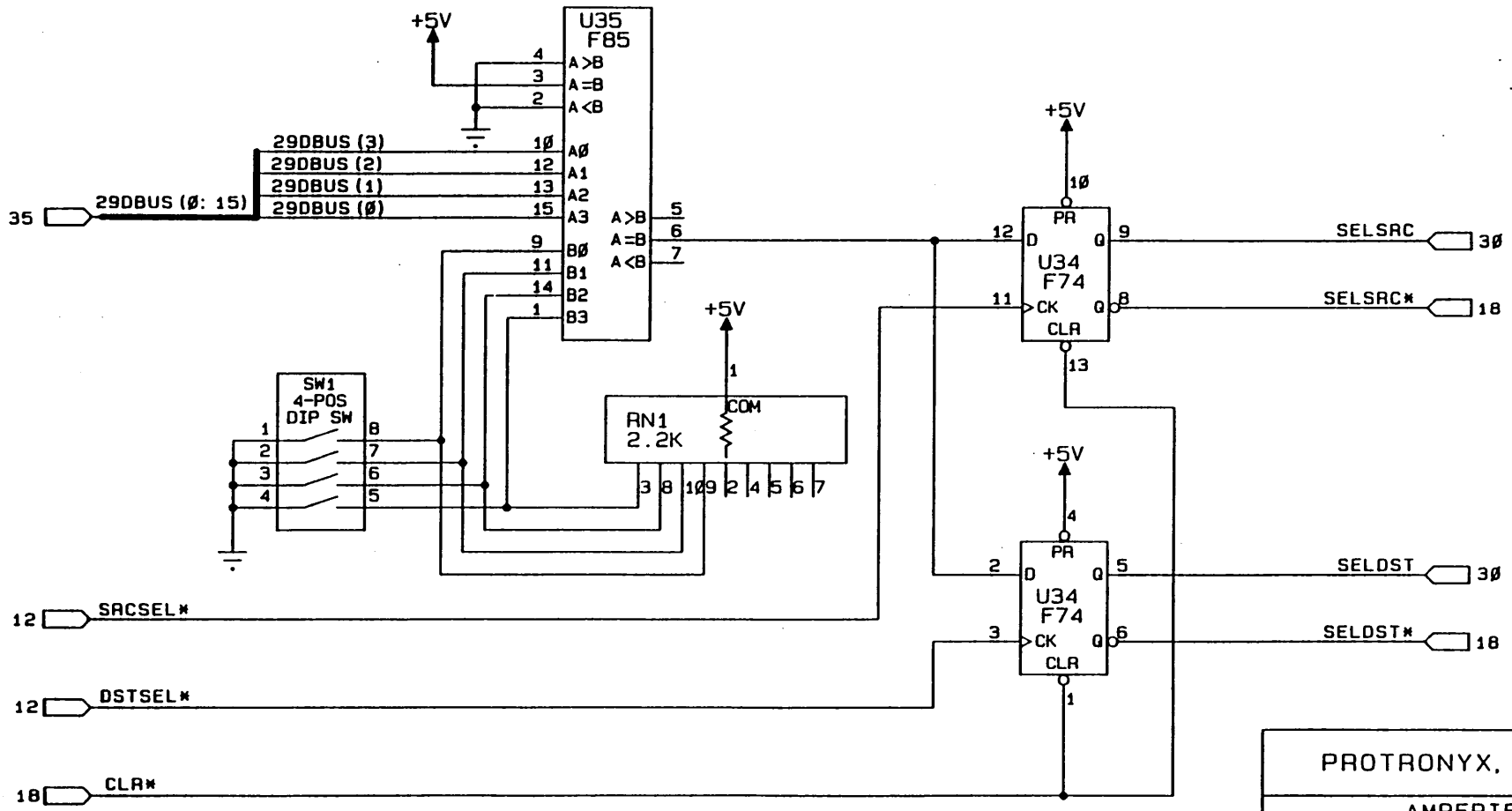
ECO 2588
SH 48



ECO 2588
SH 49



ECO 2588
SH 50



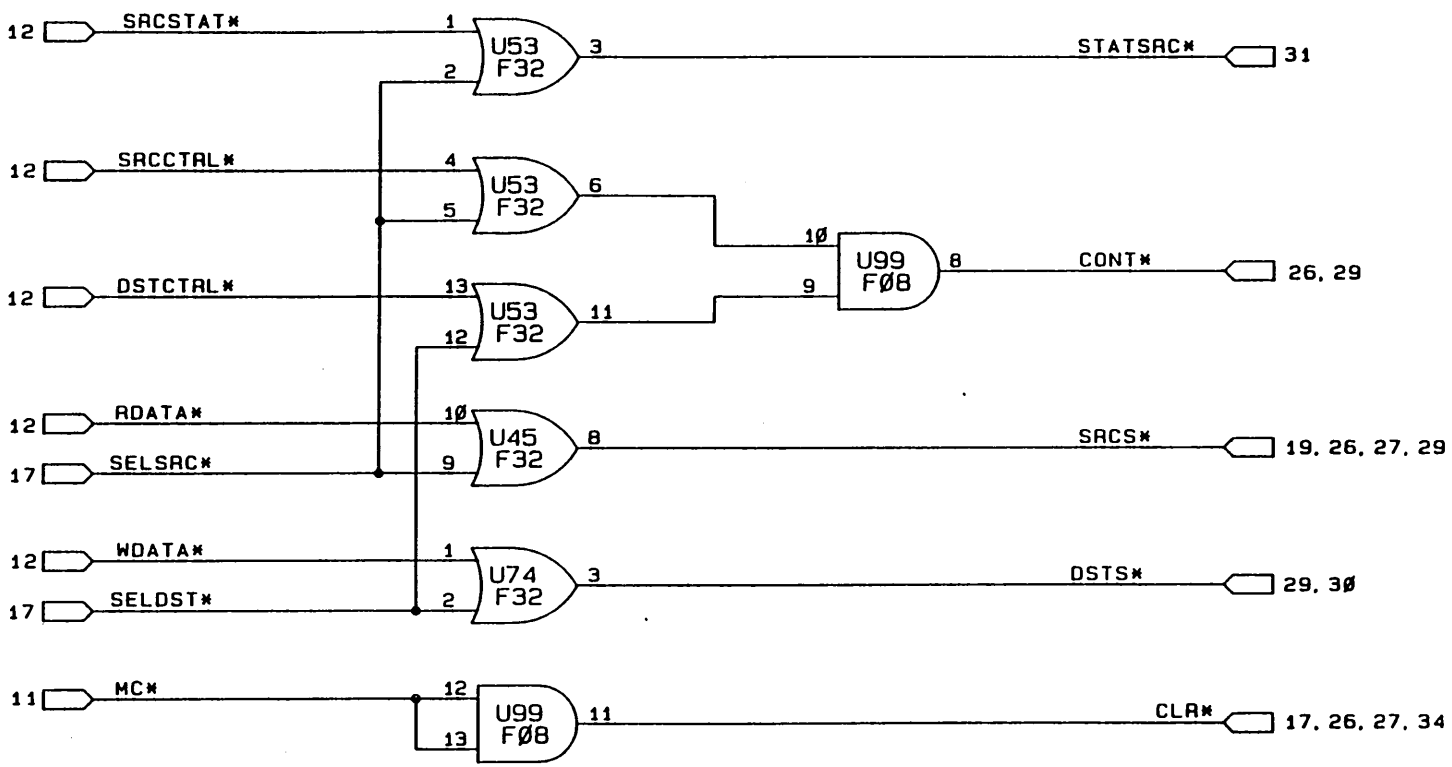
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

STATUS BUFFER
SOURCE/DEST SELECT

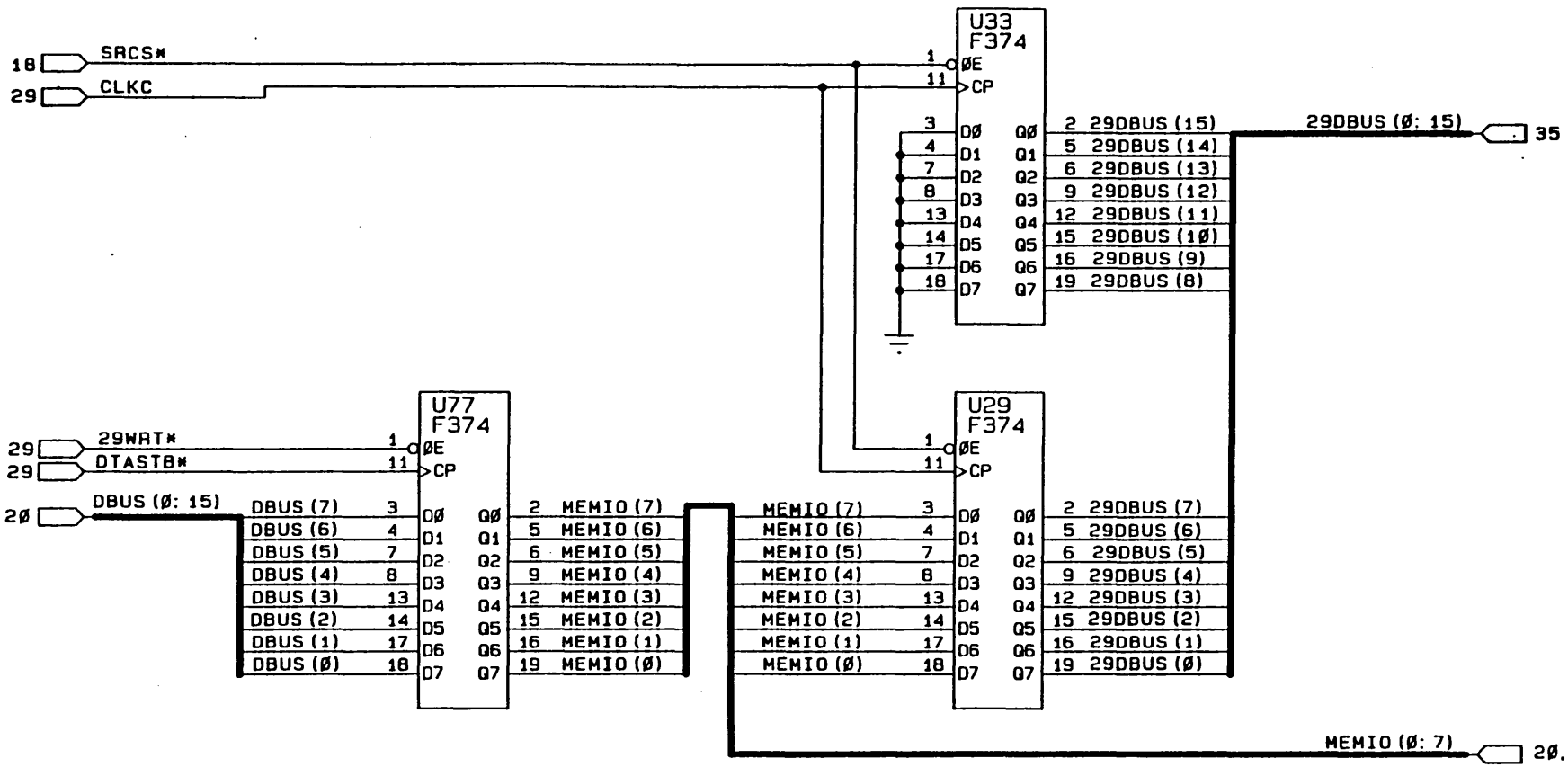
B	BD B	ASSY # 21002100	REV B
ECO	P/N		17 OF 35

ECO 2588
SH 51



PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER STATUS BUFFER CONTROL DECODE			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		18 OF 35

ECO 2588
SH 52



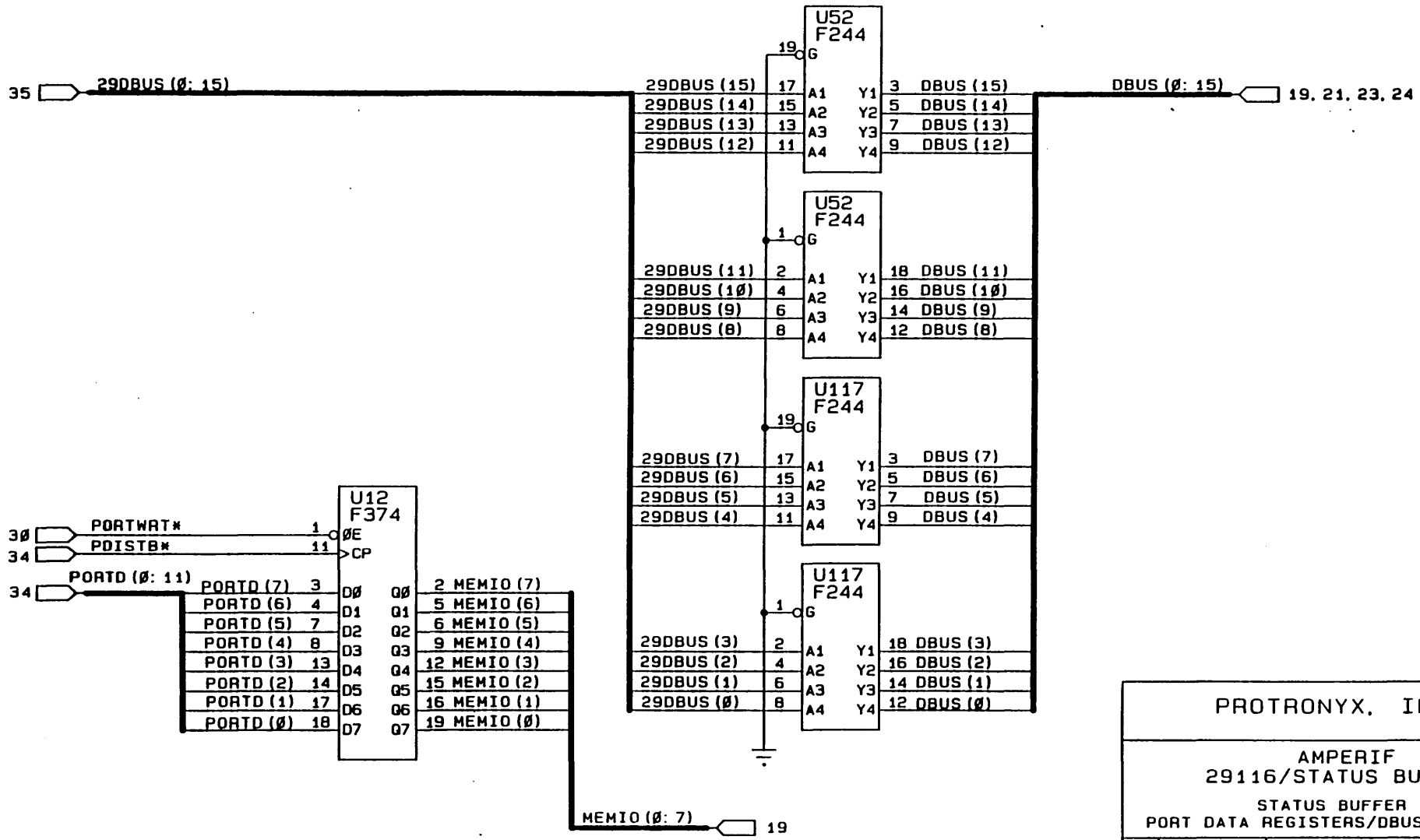
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

STATUS BUFFER
29ØØ DATA REGISTERS

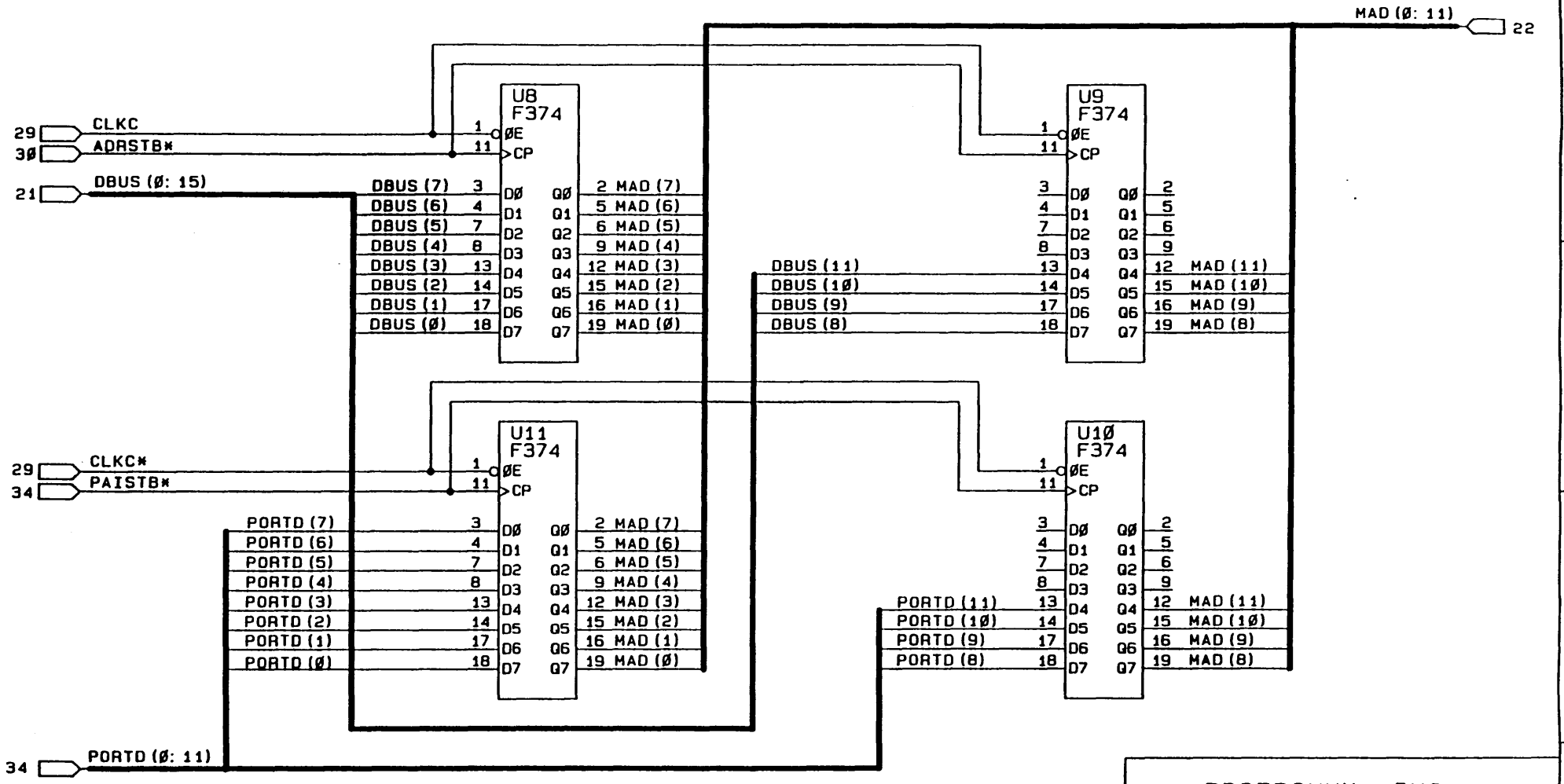
B	BD B	ASSY # 21002100	REV B
ECO	P/N		19 OF 35

ECO 2588
SH 53



PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER STATUS BUFFER PORT DATA REGISTERS/DBUS BUFFERS			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		2Ø OF 35

ECO2588
SH 54


MAD (Ø: 11)
22
U8
F374
U9
F374
U11
F374
U10
F374
29 CLKC
30 ADRSTB*
21 DBUS (Ø: 15)
29 CLKC*
34 PAISTB*
34 PORTD (Ø: 11)
ØE
CP
DBUS (7) DBUS (6) DBUS (5) DBUS (4) DBUS (3) DBUS (2) DBUS (1) DBUS (Ø)
DBUS (11) DBUS (1Ø) DBUS (9) DBUS (8)
PORTD (7) PORTD (6) PORTD (5) PORTD (4) PORTD (3) PORTD (2) PORTD (1) PORTD (Ø)
PORTD (11) PORTD (1Ø) PORTD (9) PORTD (8)
MAD (7) MAD (6) MAD (5) MAD (4) MAD (3) MAD (2) MAD (1) MAD (Ø)
MAD (11) MAD (1Ø) MAD (9) MAD (8)

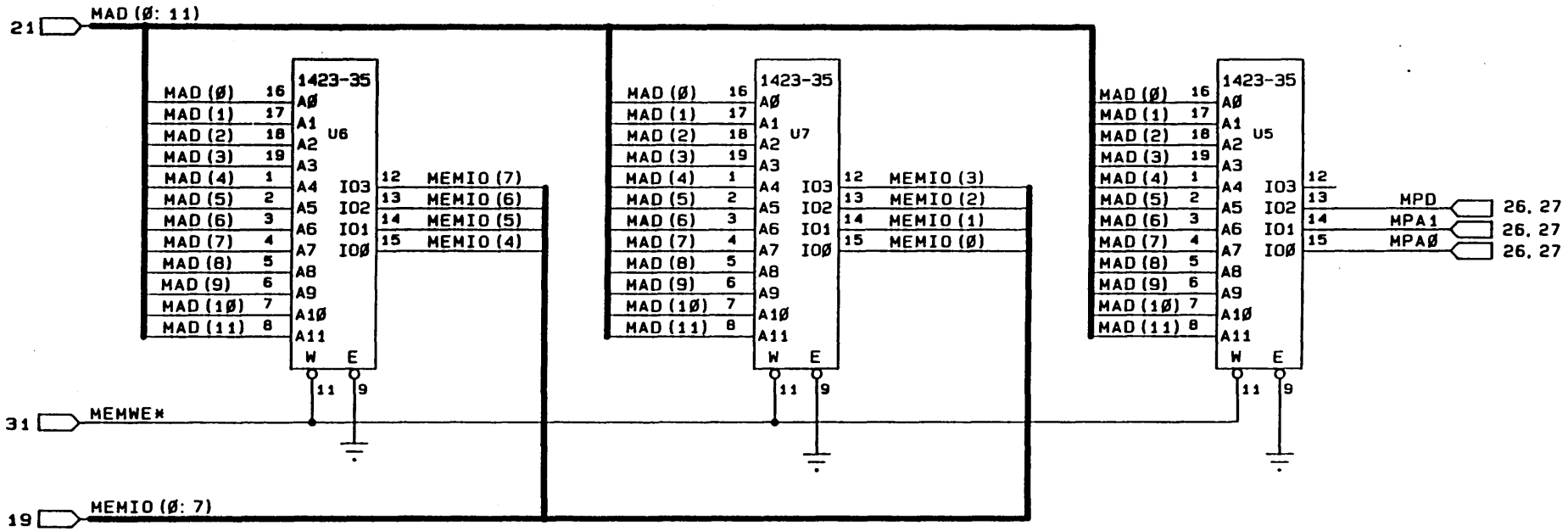
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

STATUS BUFFER
ADDRESS REGISTERS

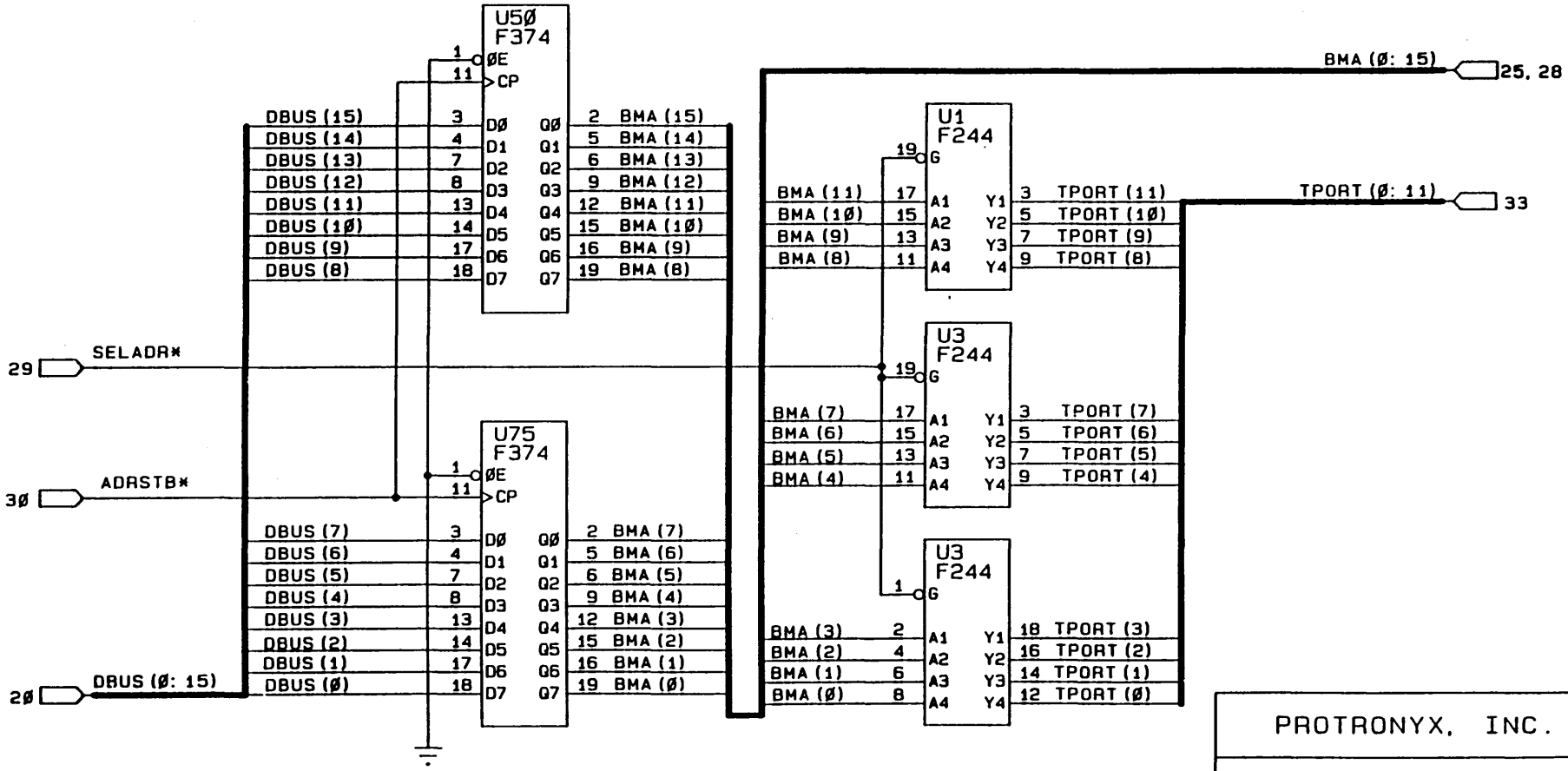
B	BD B	ASSY # 21002100	REV B
ECO	P/N		21 OF 35

ECO 2588
SH 55



PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER STATUS BUFFER MEMORY			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		22 OF 35

ECO 2588
SH 56

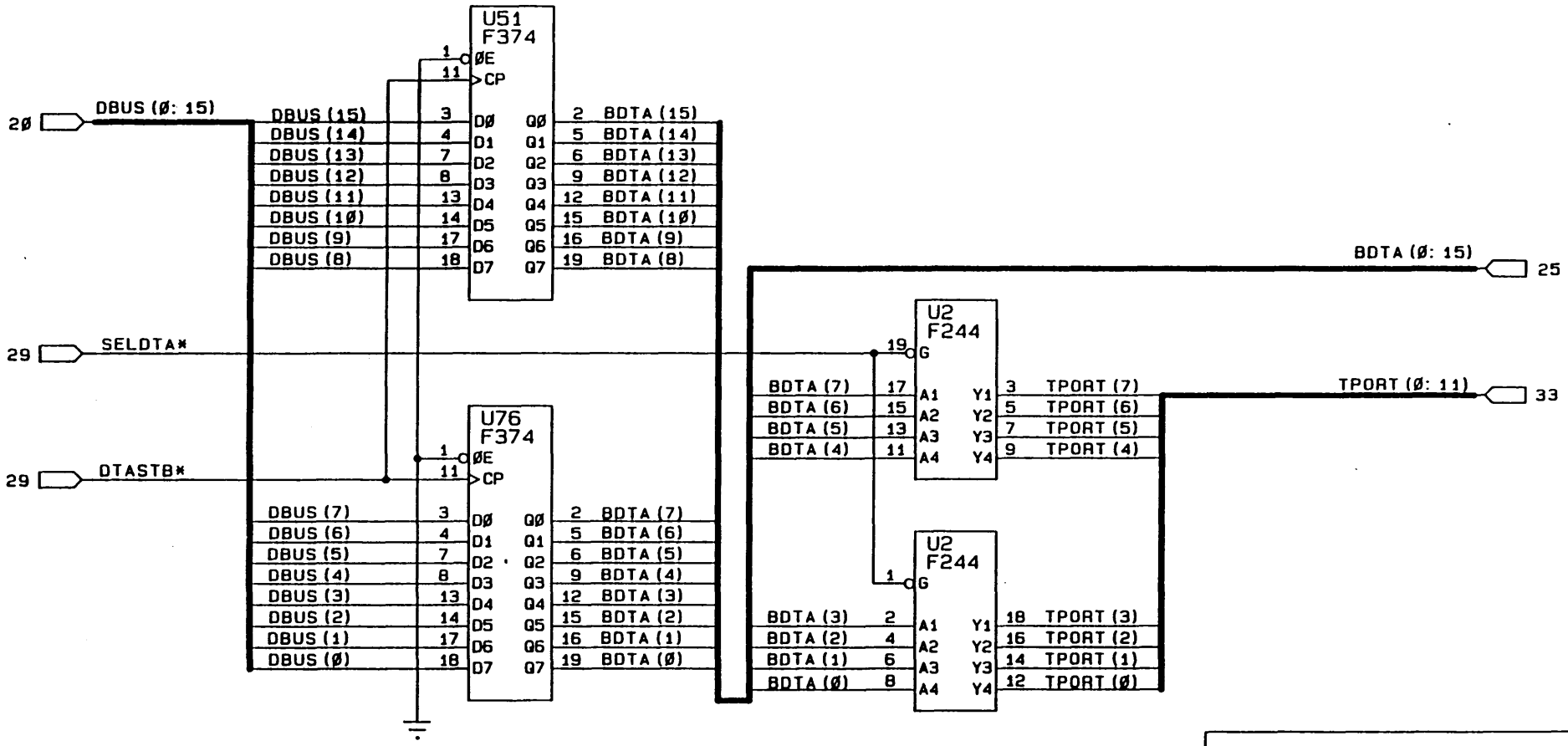


PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER
STATUS BUFFER
PORT DRIVERS/ADDRESS

B	BD B	ASSY # 21002100	REV B
ECO	P/N		23 OF 35

ECO 2588
SH 57



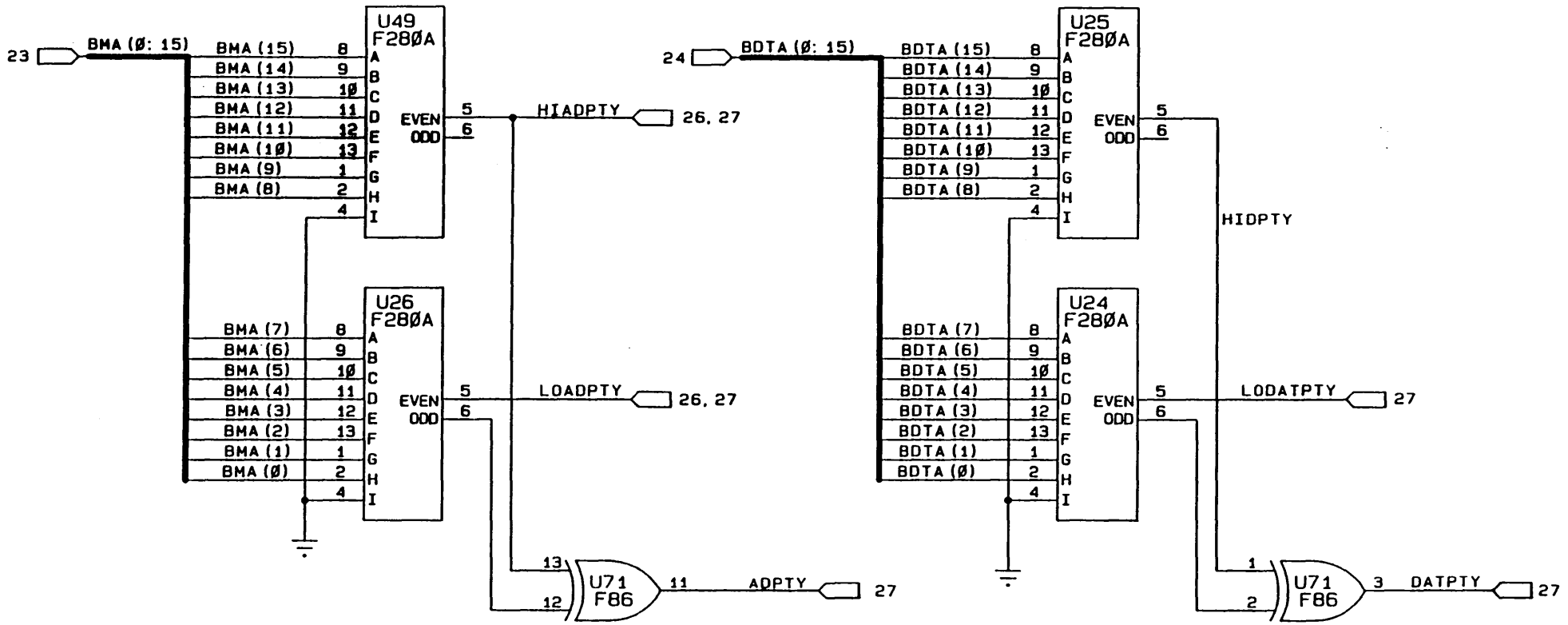
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

STATUS BUFFER
PORT DRIVER/DATA

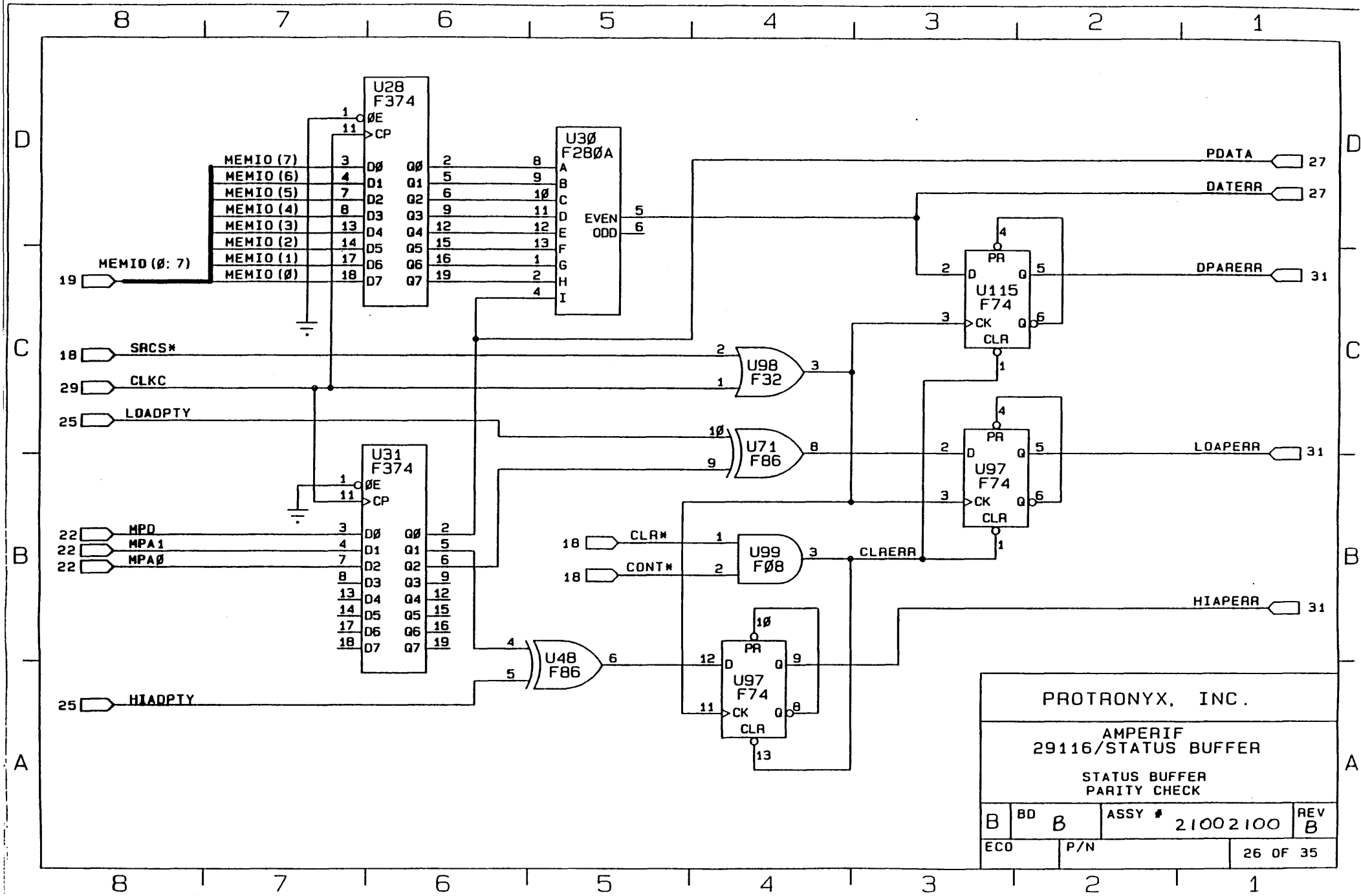
B	BD B	ASSY # 21002100	REV B
ECO	P/N		24 OF 35

ECO 2588
SH 58

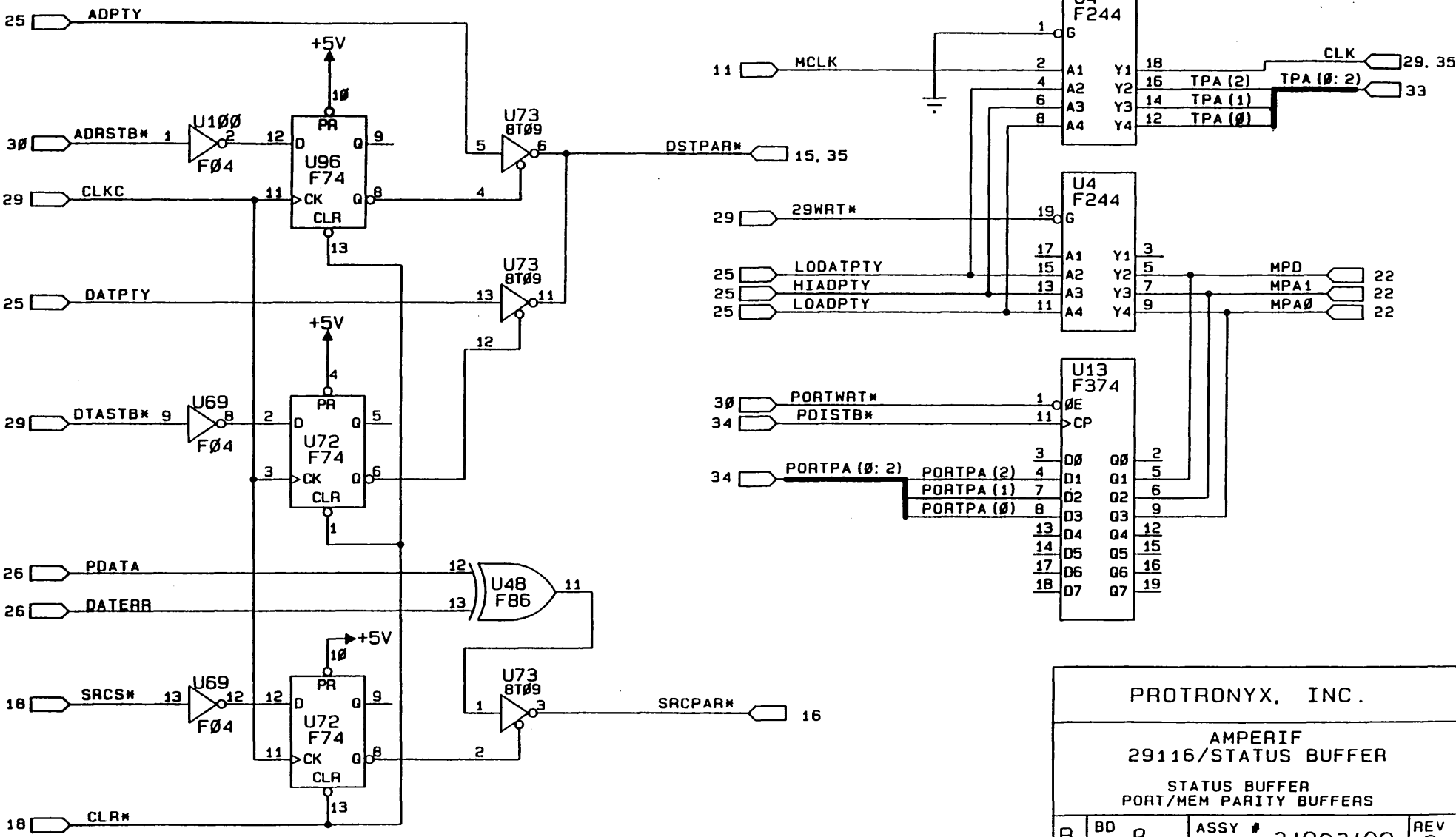


PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER STATUS BUFFER PARITY GENERATORS			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		25 OF 35

ECO 2588
SH 59

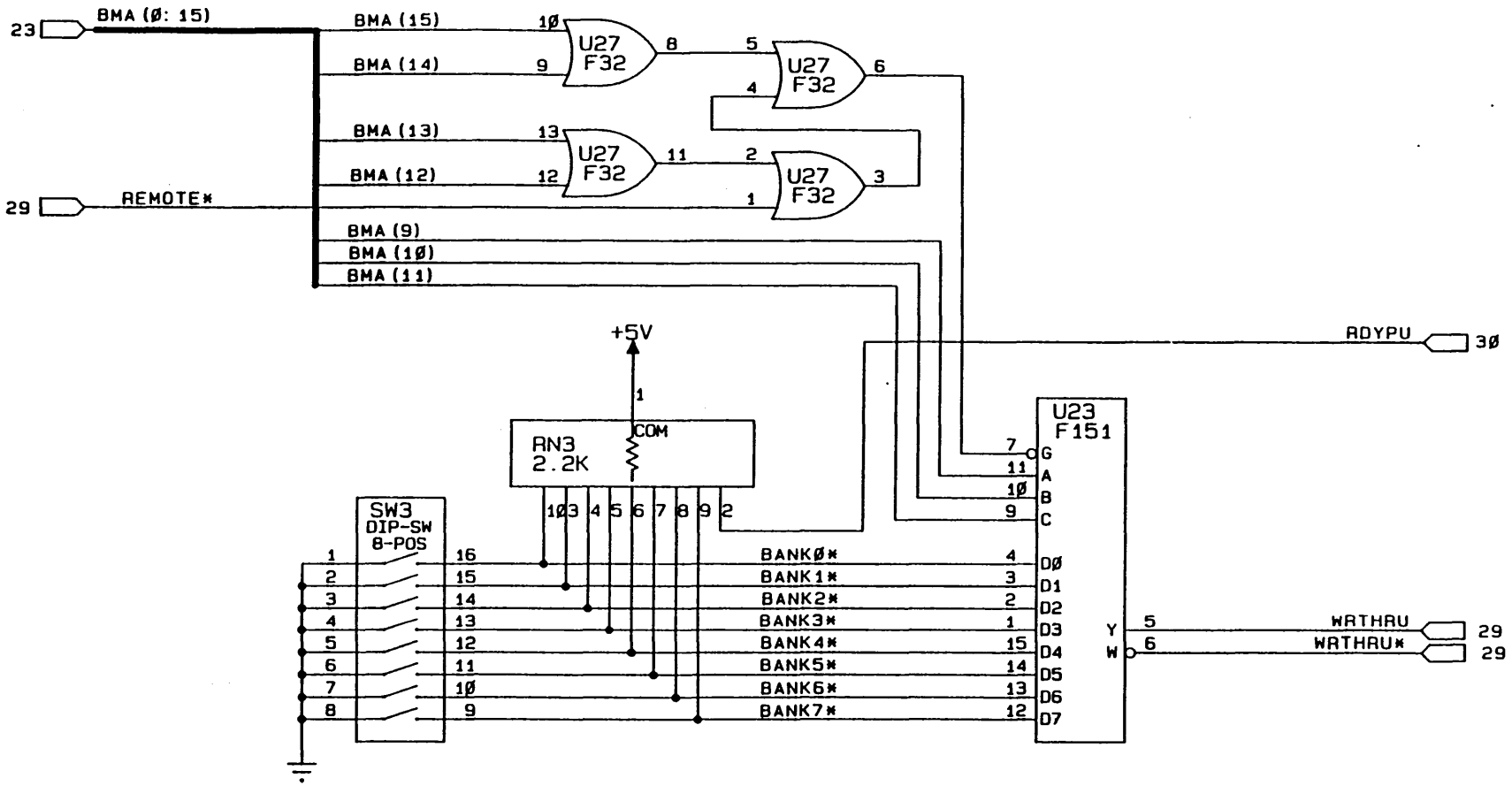


ECO 2588
SH 60



PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER			
STATUS BUFFER PORT/MEM PARITY BUFFERS			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		27 OF 35

ECO 2588
SH 6I



NOTES:

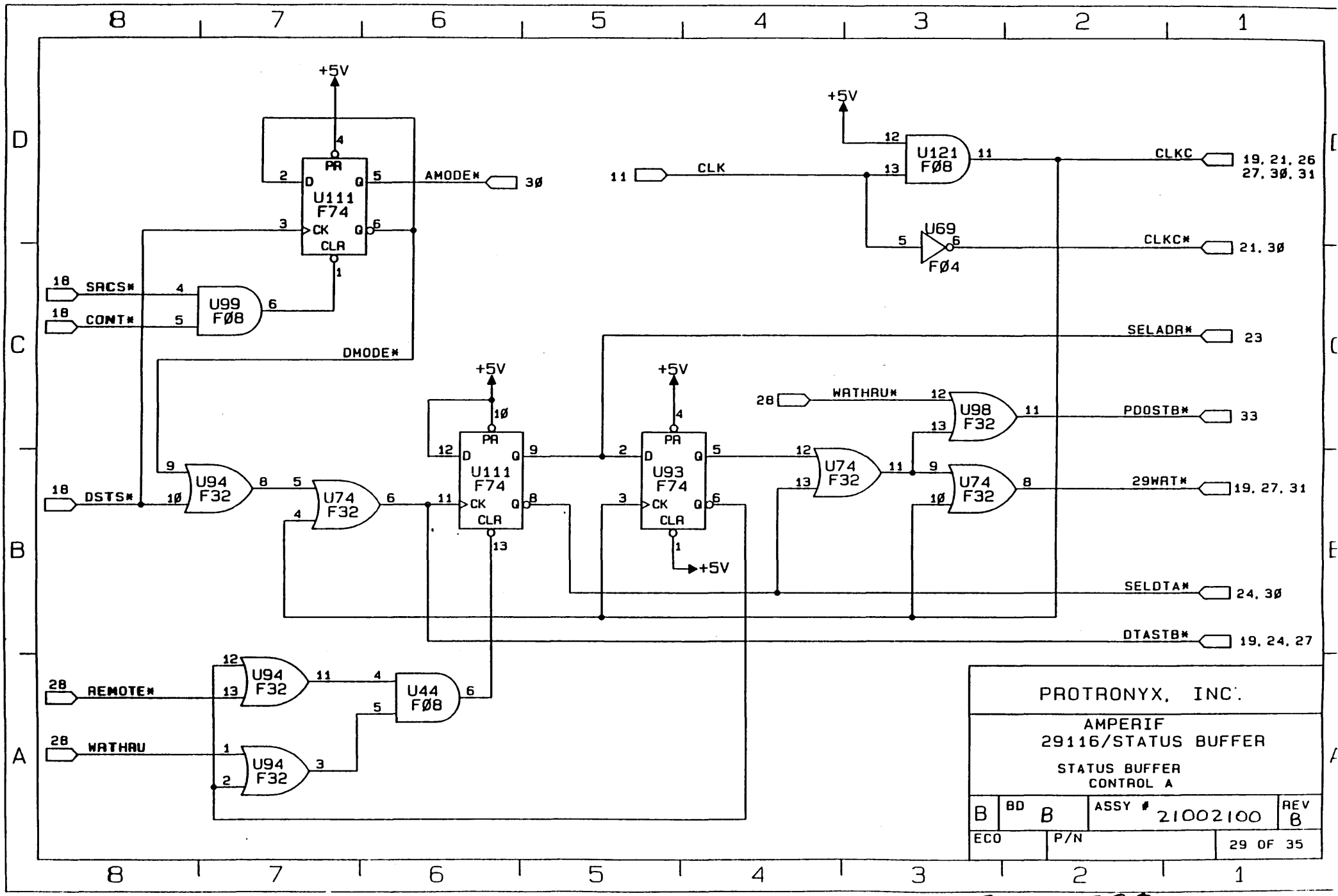
4. SW3 SELECTS RESPECTIVE 512 WORD BANK FOR WRITE THROUGH WHEN OPEN.
   i.e. ADDRESSES Ø-511 WILL WRITE THROUGH WHEN SW3, POSITION 1 IS OPEN.

PROTRONYX, INC.

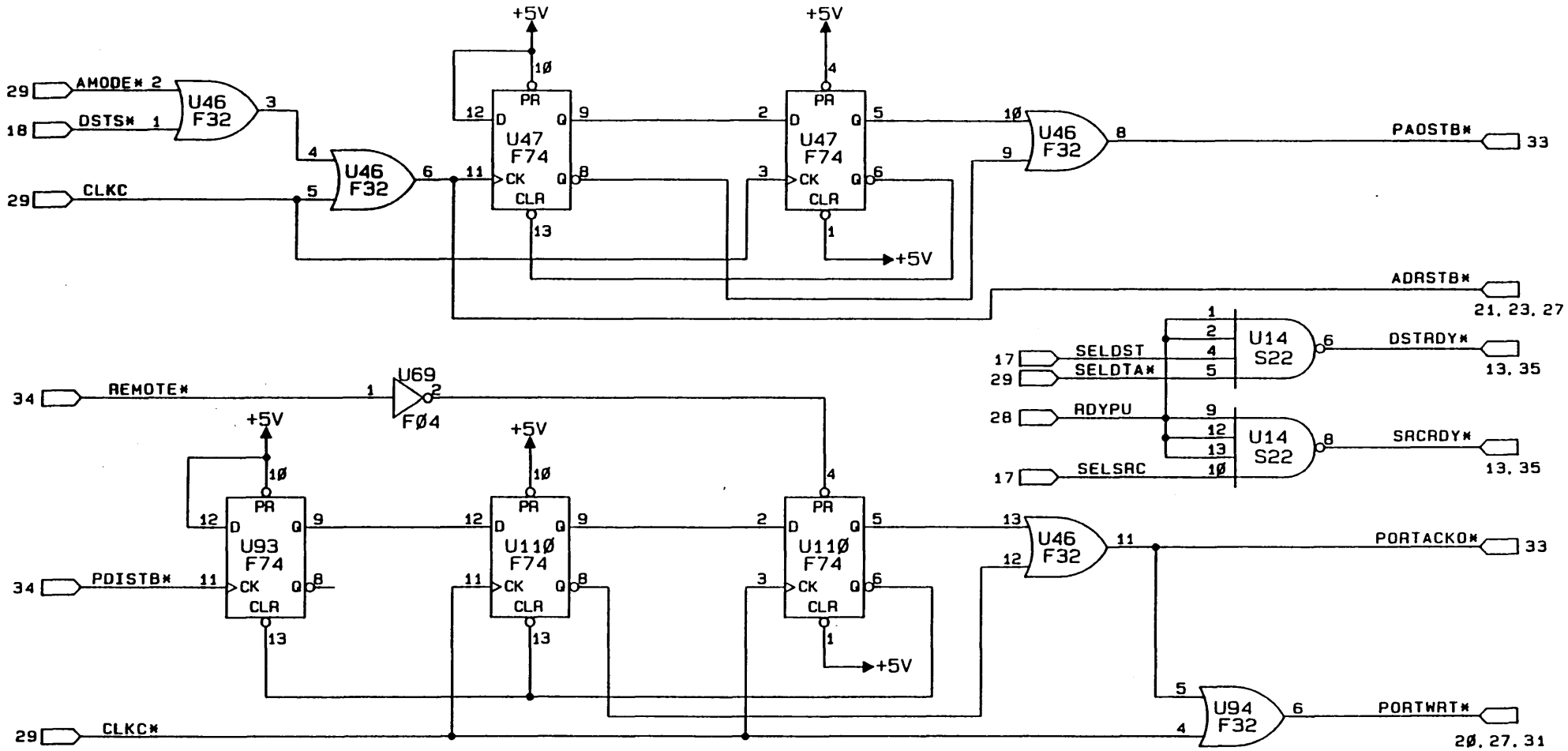
AMPERIF
29116/STATUS BUFFER
STATUS BUFFER
ADDRESS RANGE SELECTOR

B	BD B	ASSY # 21002100	REV B
ECO	P/N		28 OF 35

ECO 2588
SH 62

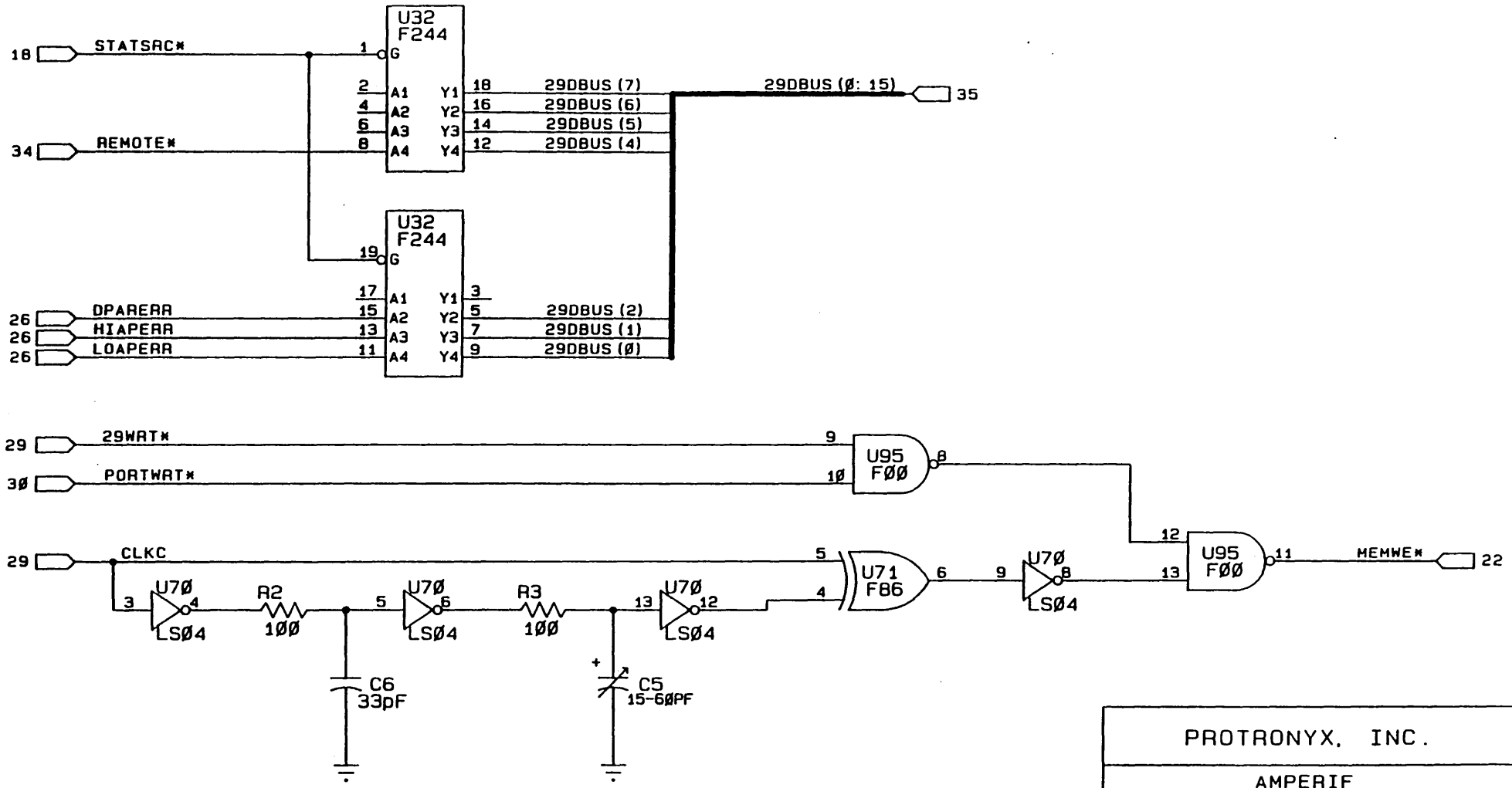


ECO 2588
SH 63



PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER STATUS BUFFER CONTROL B			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		30 OF 35

ECO 2588
SH 64



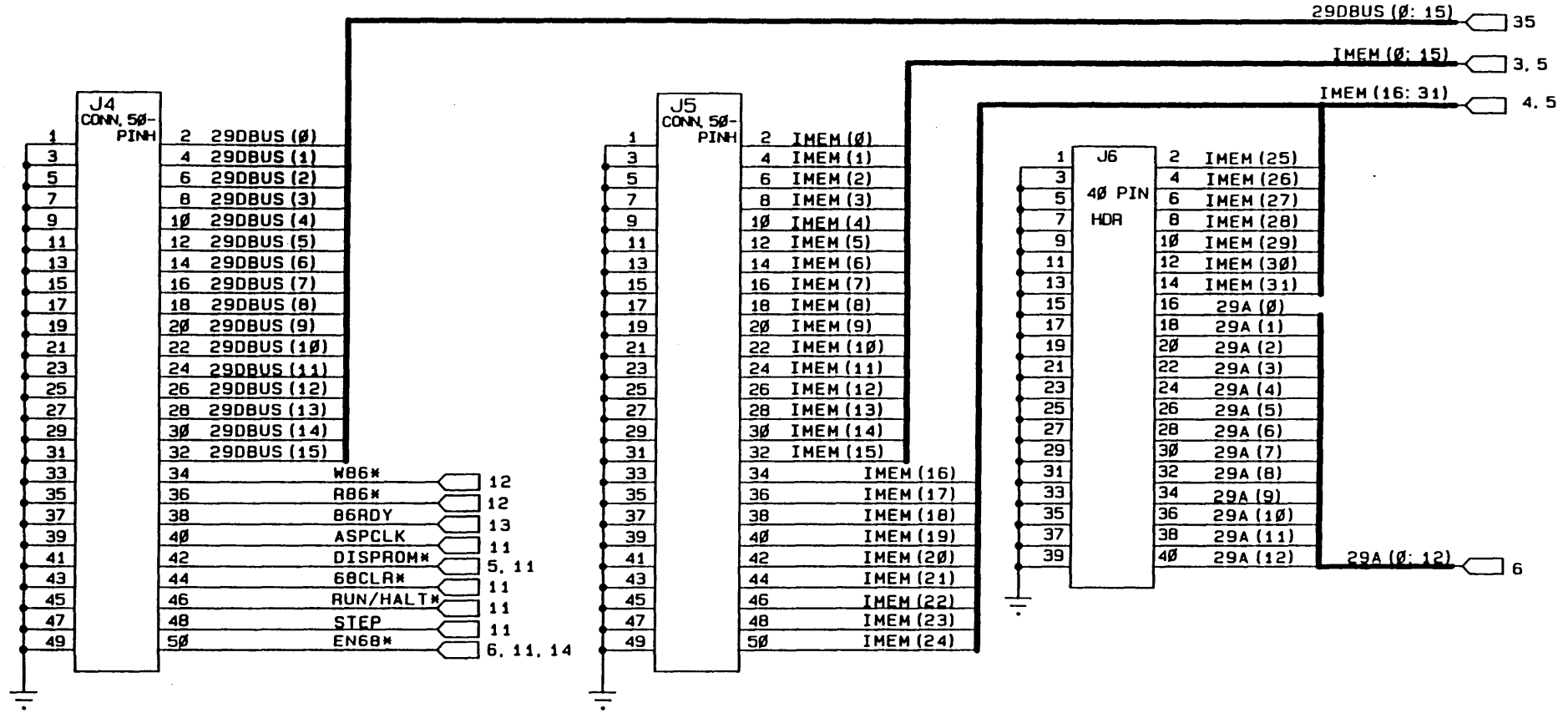
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

STATUS BUFFER
STATUS OUT/WRITE ENABLE

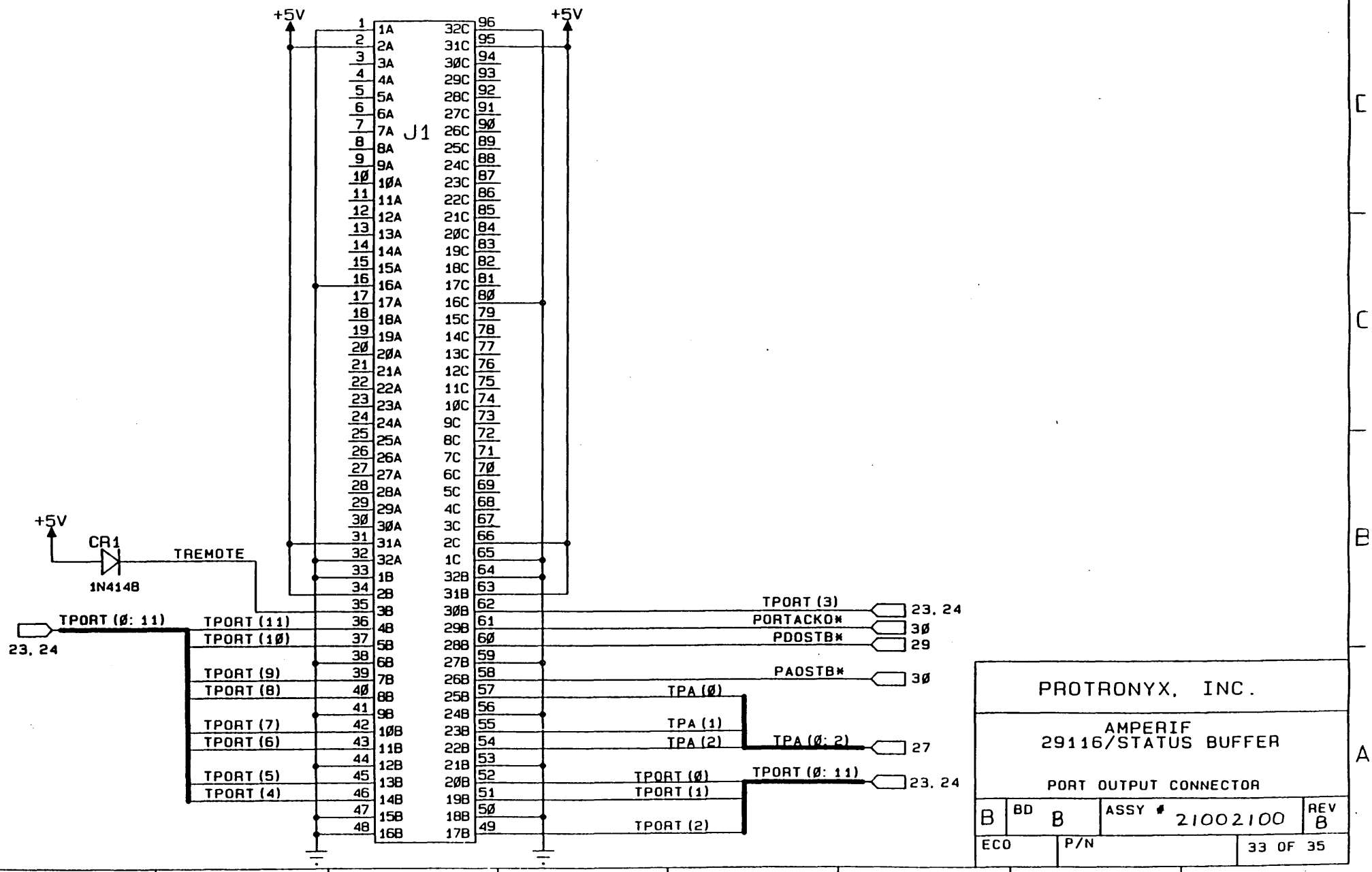
B	BD B	ASSY # 21002100	REV B
ECO	P/N		31 OF 35

ECO 2588
SH 65



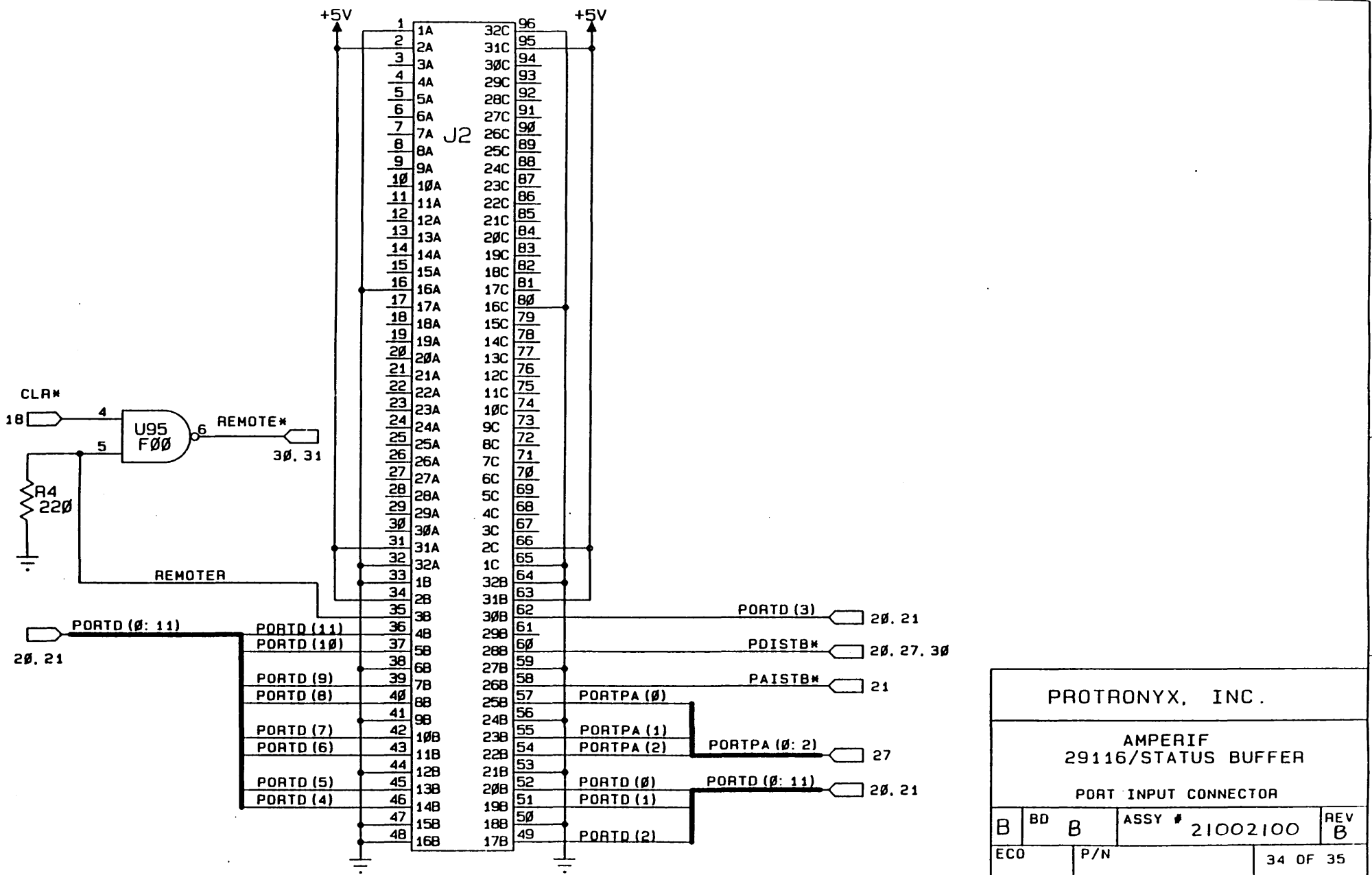
PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER			
ASP CONNECTORS			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		32 OF 35

ECO 2588
SH-66



PROTRONYX, INC.			
AMPERIF 29116/STATUS BUFFER			
PORT OUTPUT CONNECTOR			
B	BD B	ASSY # 21002100	REV B
ECO	P/N		33 OF 35

ECO 2588
SH 67



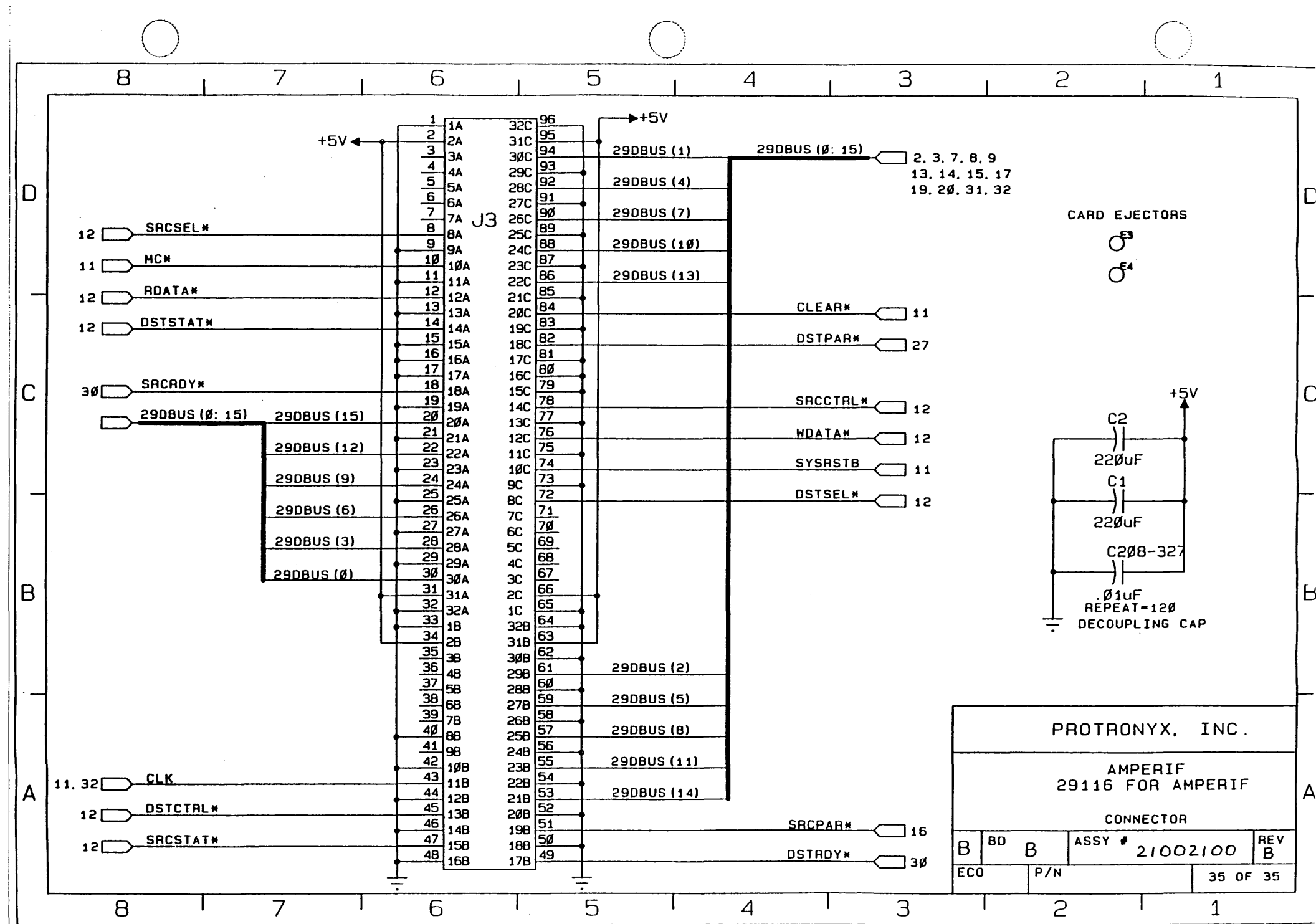
PROTRONYX, INC.

AMPERIF
29116/STATUS BUFFER

PORT INPUT CONNECTOR

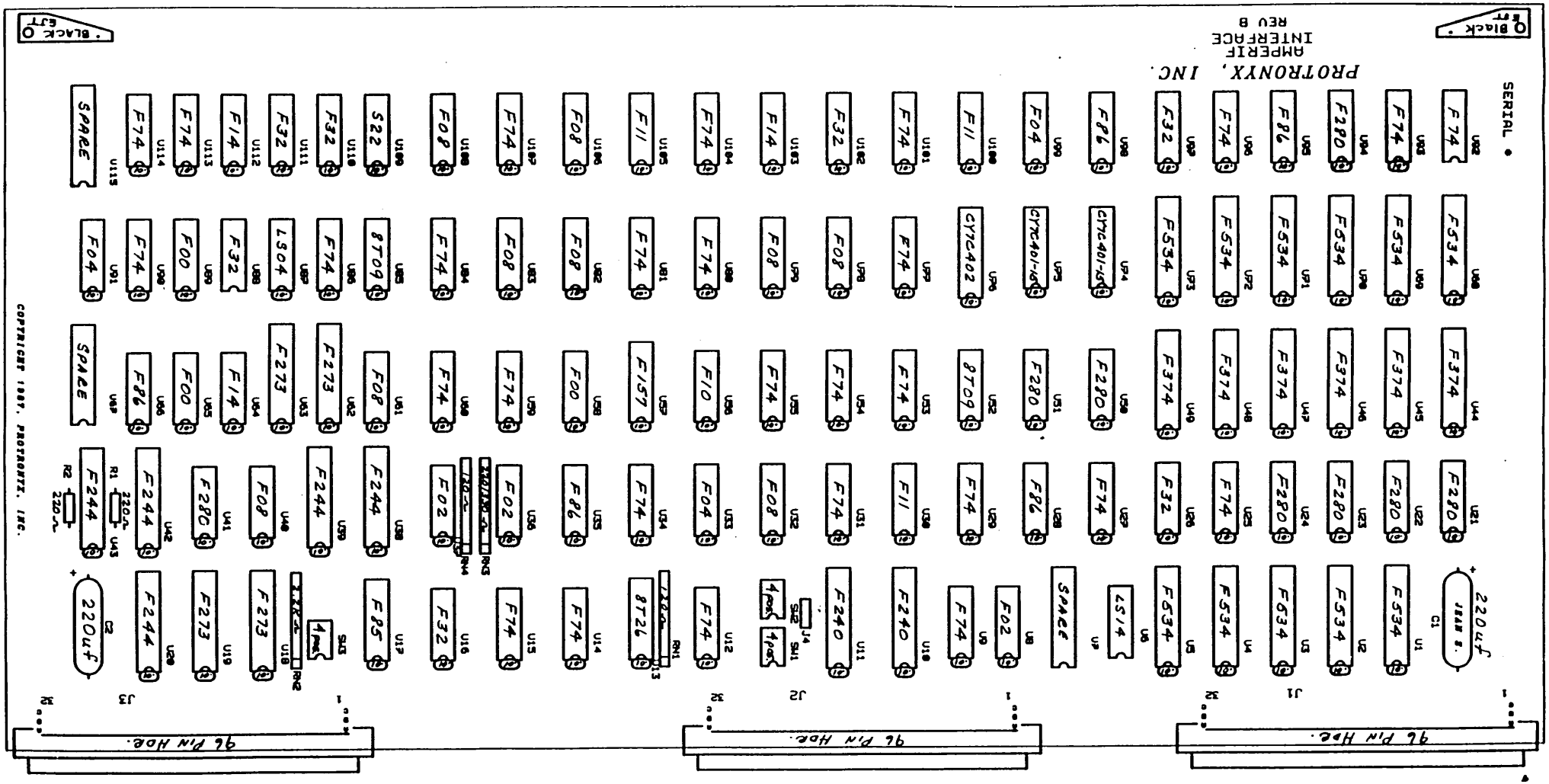
B	BD B	ASSY # 21002100	REV B
ECO	P/N		34 OF 35

ECO 2588
SH 68



ECO 2588
SH. 69

Assembly 21002000 11/25/87
Rev. B (Board)
Rev. B (Assembly)



ECO 2588
SH 4 OF

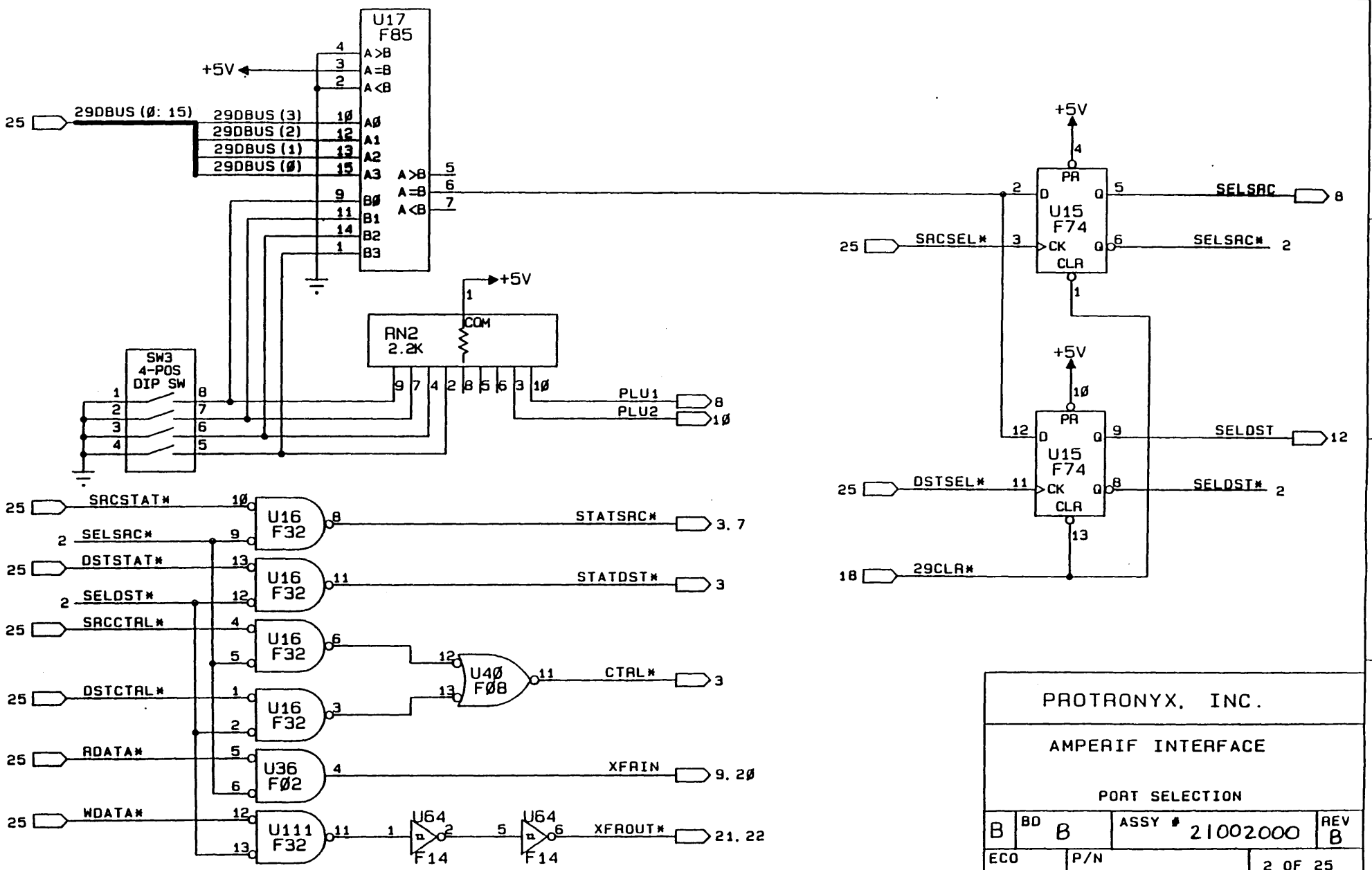
PROTRONYX, INC.

AMPERIF INTERFACE
U BUS
REVISION HISTORY

B	BD B	ASSY # 21002000	REV B
ECO	P/N		1 OF 25

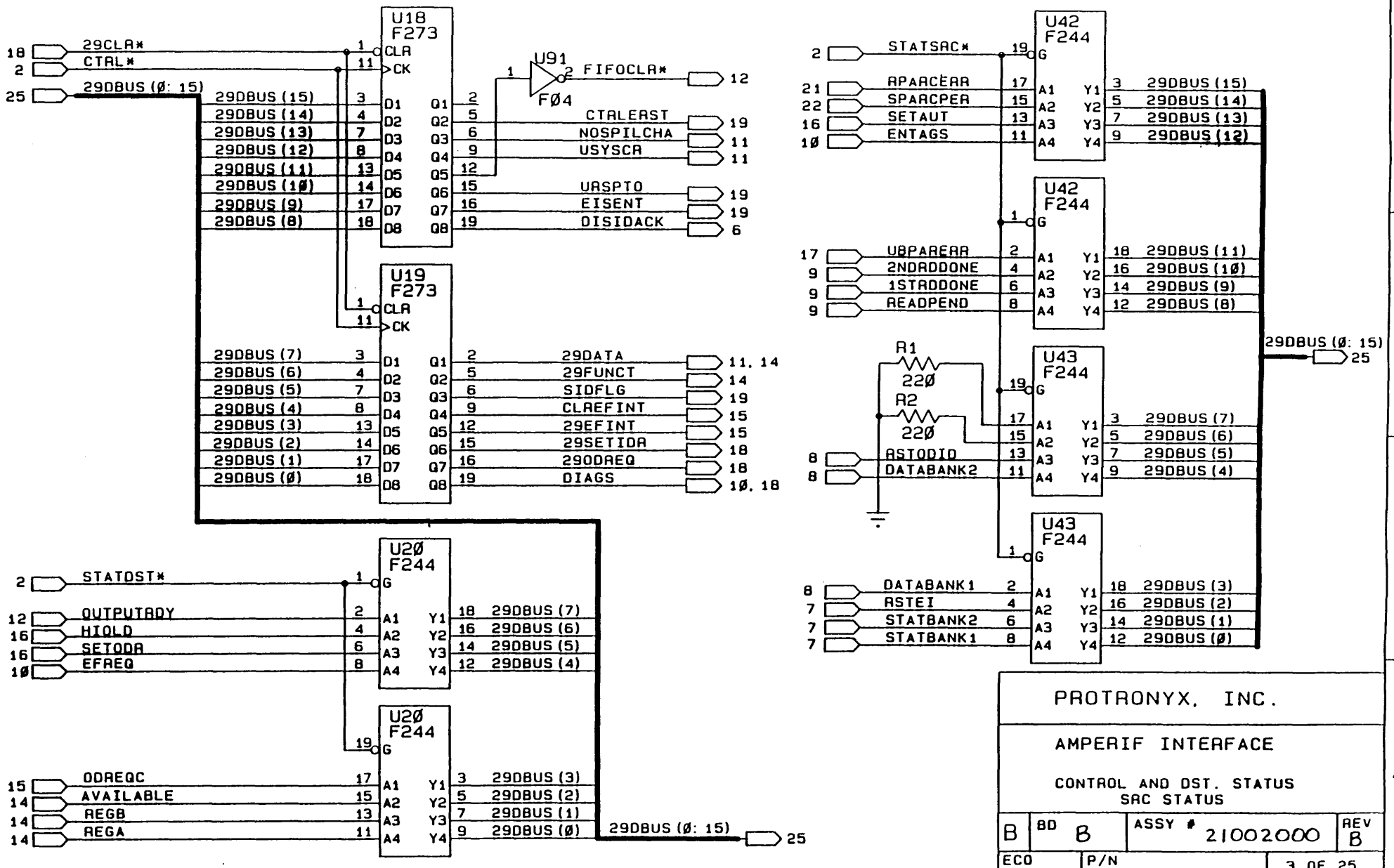
PROTRONYX, INC.
COPYRIGHT, 1987

ECO 2588
SH 7

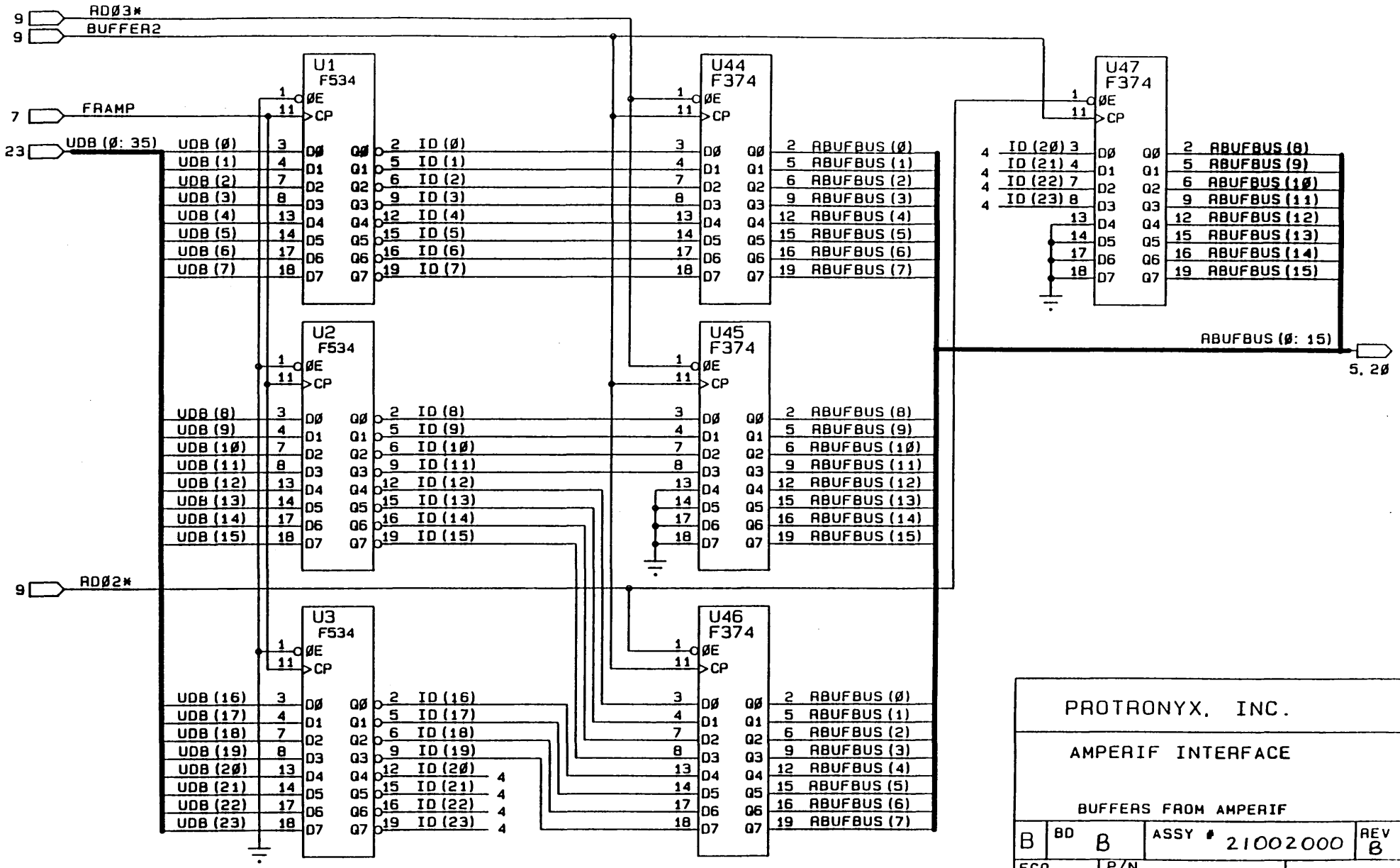

U17
F85
A>B
A=B
A<B
+5V
25
29DBUS (Ø: 15)
29DBUS (3)
29DBUS (2)
29DBUS (1)
29DBUS (Ø)
AØ
A1
A2
A3
BØ
B1
B2
B3
RN2
2.2K
COM
SW3
4-POS
DIP SW
PLU1
PLU2
U15
F74
PR
CK
CLR
SELSRC
SELSRC*
SRCSEL*
SELDST
SELDSI*
DSTSEL*
29CLR*
SRCSTAT*
DSTSTAT*
SELDST*
SRCCTRL*
DSTCTRL*
RDATA*
WDATA*
U16
F32
U36
FØ2
U111
U4Ø
FØ8
CTRL*
XFRIN
XFROUT*
U64
F14
STATSRC*
STATDST*
PROTRONYX, INC.
AMPERIF INTERFACE
PORT SELECTION
BD B
ASSY # 21002000
REV B
ECO
P/N
2 OF 25

ECO 2588

548


U18 F273
U19 F273
U91 F04
U20 F244
U20 F244
U42 F244
U42 F244
U43 F244
U43 F244
29CLR*
CTRL*
29DBUS (Ø: 15)
29DBUS (15)
29DBUS (14)
29DBUS (13)
29DBUS (12)
29DBUS (11)
29DBUS (1Ø)
29DBUS (9)
29DBUS (8)
29DBUS (7)
29DBUS (6)
29DBUS (5)
29DBUS (4)
29DBUS (3)
29DBUS (2)
29DBUS (1)
29DBUS (Ø)
FIFOCLR*
CTRLERST
NOSPILCHA
USYSCR
UBSPTO
EISENT
DISIDACK
29DATA
29FUNCT
SIDFLG
CLREFINT
29EFINT
29SETIDA
29ODREQ
DIAGS
STATDST*
OUTPUTRDY
HIOLD
SETODA
EFREQ
ODREQC
AVAILABLE
REGB
REGA
STATSAC*
APARCERR
SPARCPER
SETAUT
ENTAGS
UBPARERR
2NDRADDONE
1STRADDONE
READPEND
R1
220
R2
220
RSTODID
DATABANK2
DATABANK1
RSTEI
STATBANK2
STATBANK1
PROTRONYX, INC.
AMPERIF INTERFACE
CONTROL AND DST. STATUS
SAC STATUS
B
BD B
ASSY # 21002000
REV B
ECO
P/N
3 OF 25

ECO 2588
SH 9



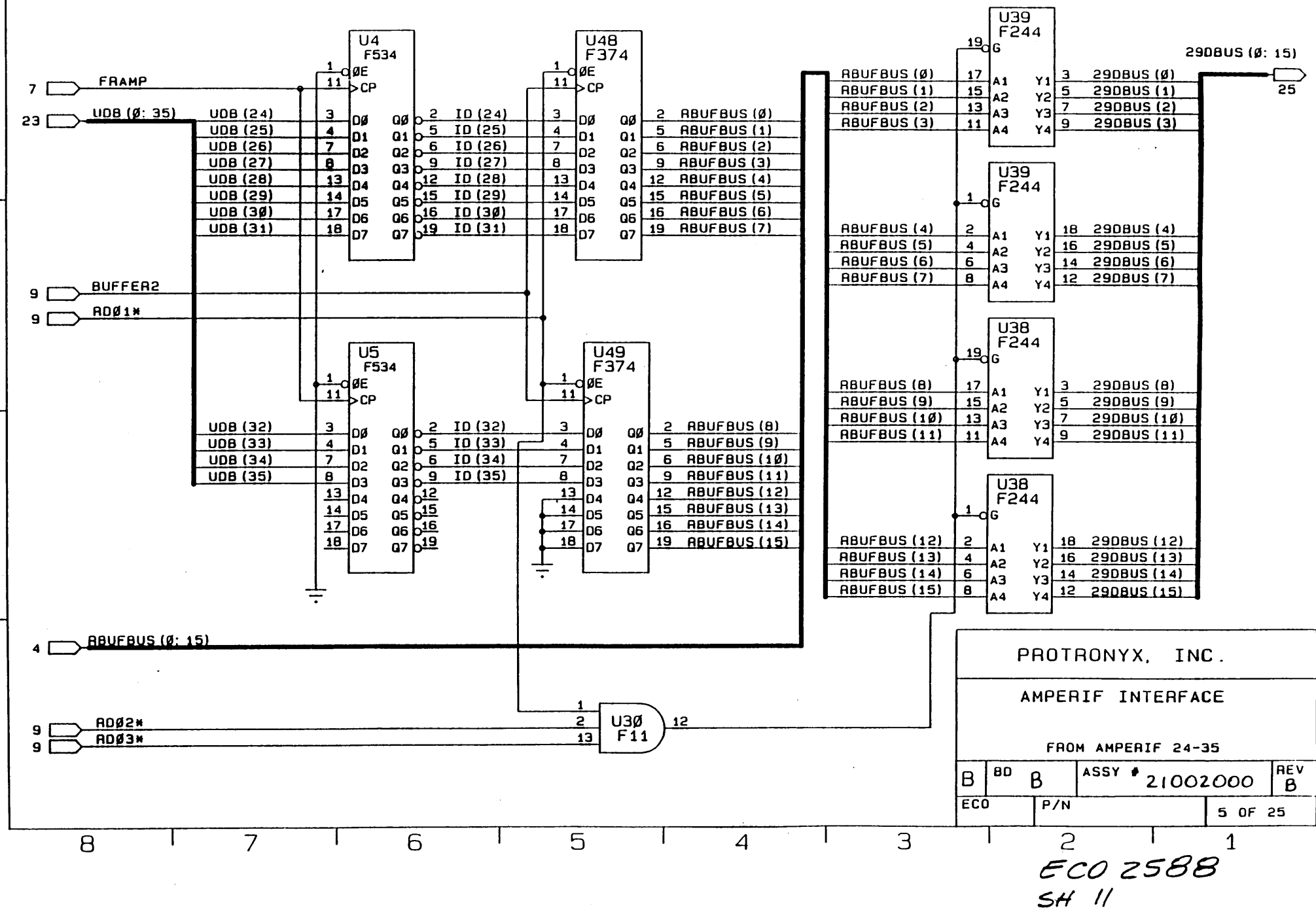
PROTRONYX, INC.

AMPERIF INTERFACE

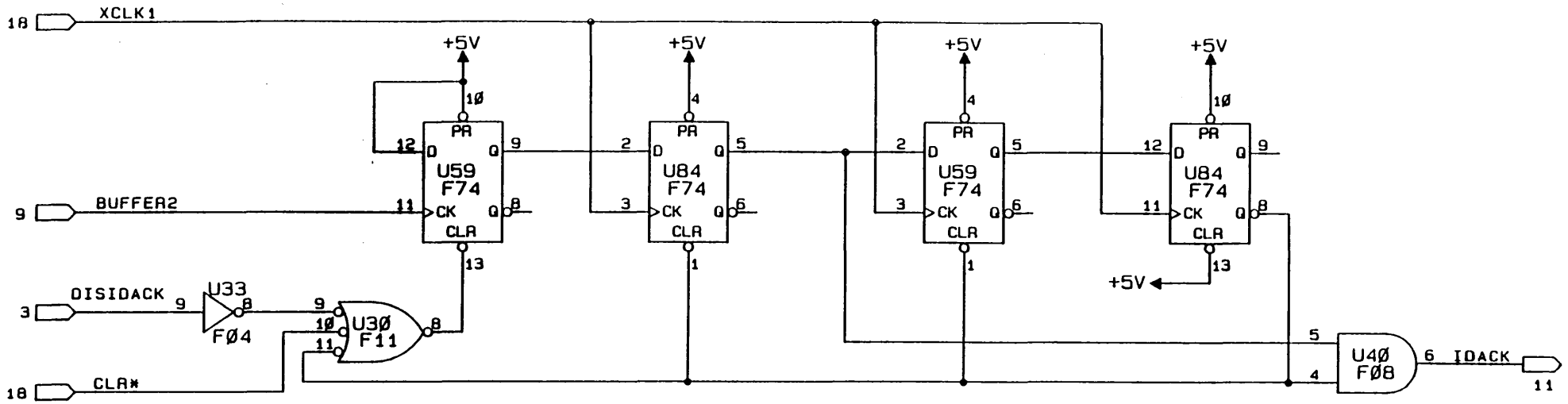
BUFFERS FROM AMPERIF

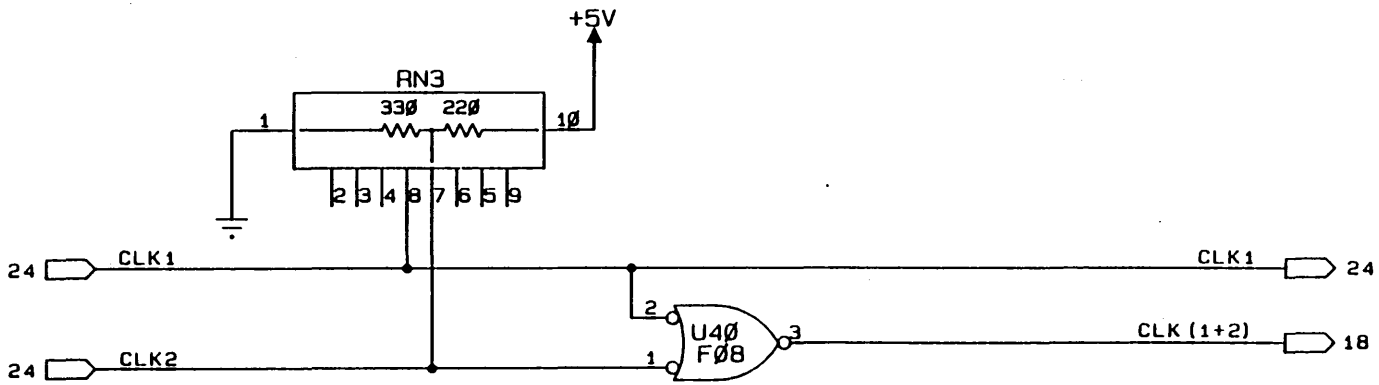
B	BD B	ASSY # 21002000	REV B
ECO	P/N		4 OF 25

ECO 2588
SH 10



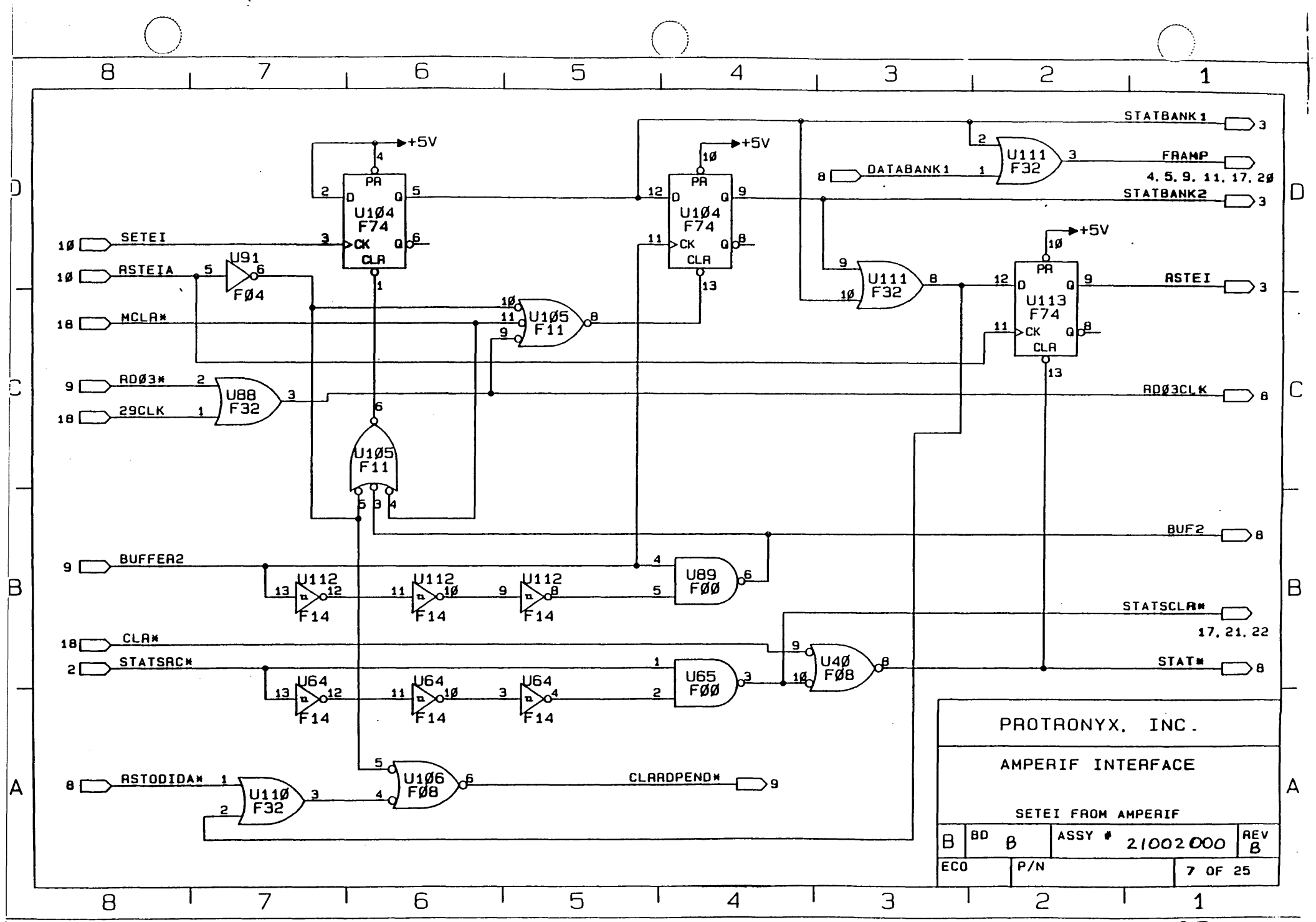
ECO 2588
SH 11



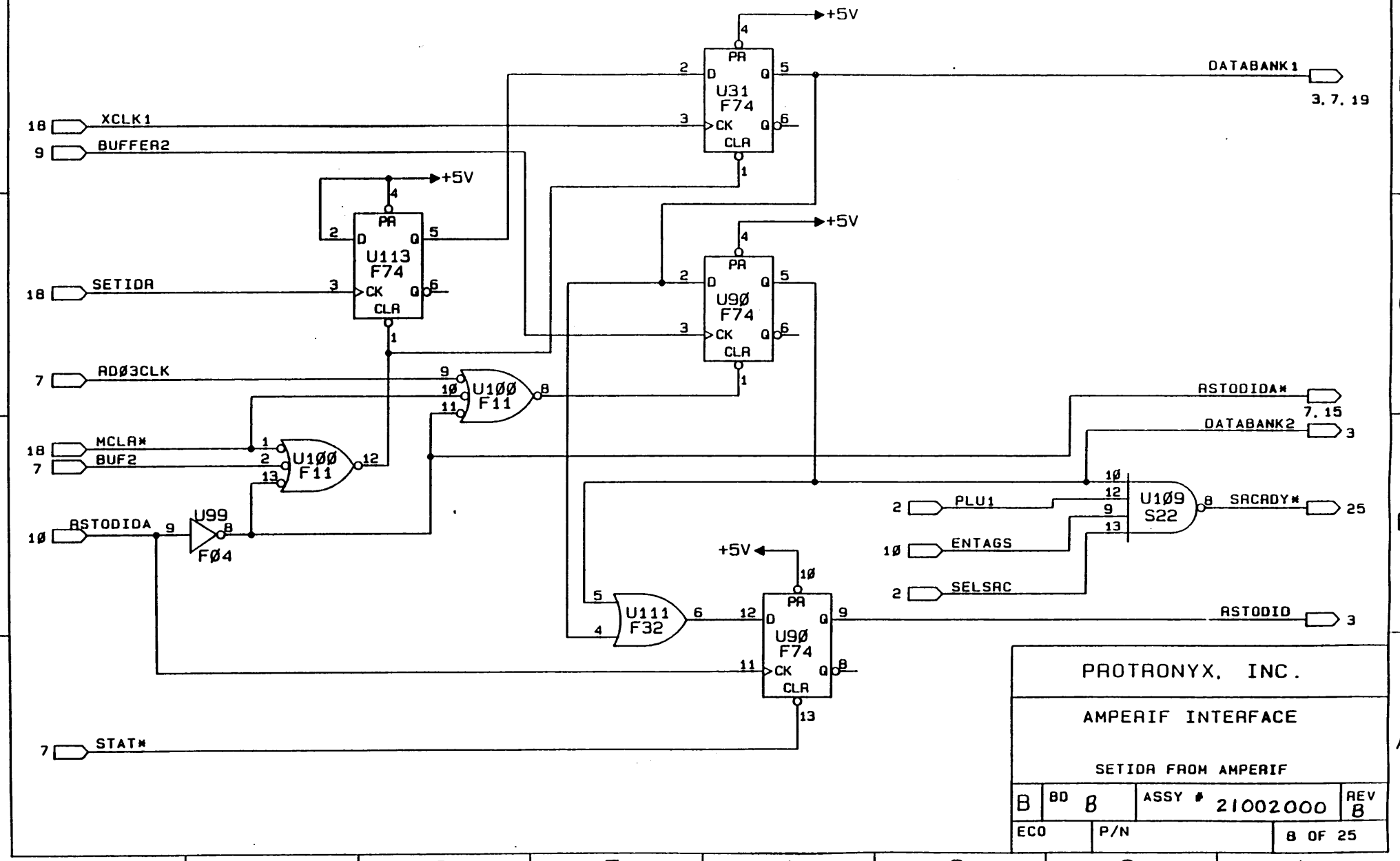


PROTRONYX, INC.			
AMPERIF INTERFACE			
IDACK - UBUS CLOCKS			
B	BD B	ASSY # 21002000	REV B
ECO	P/N		6 OF 25

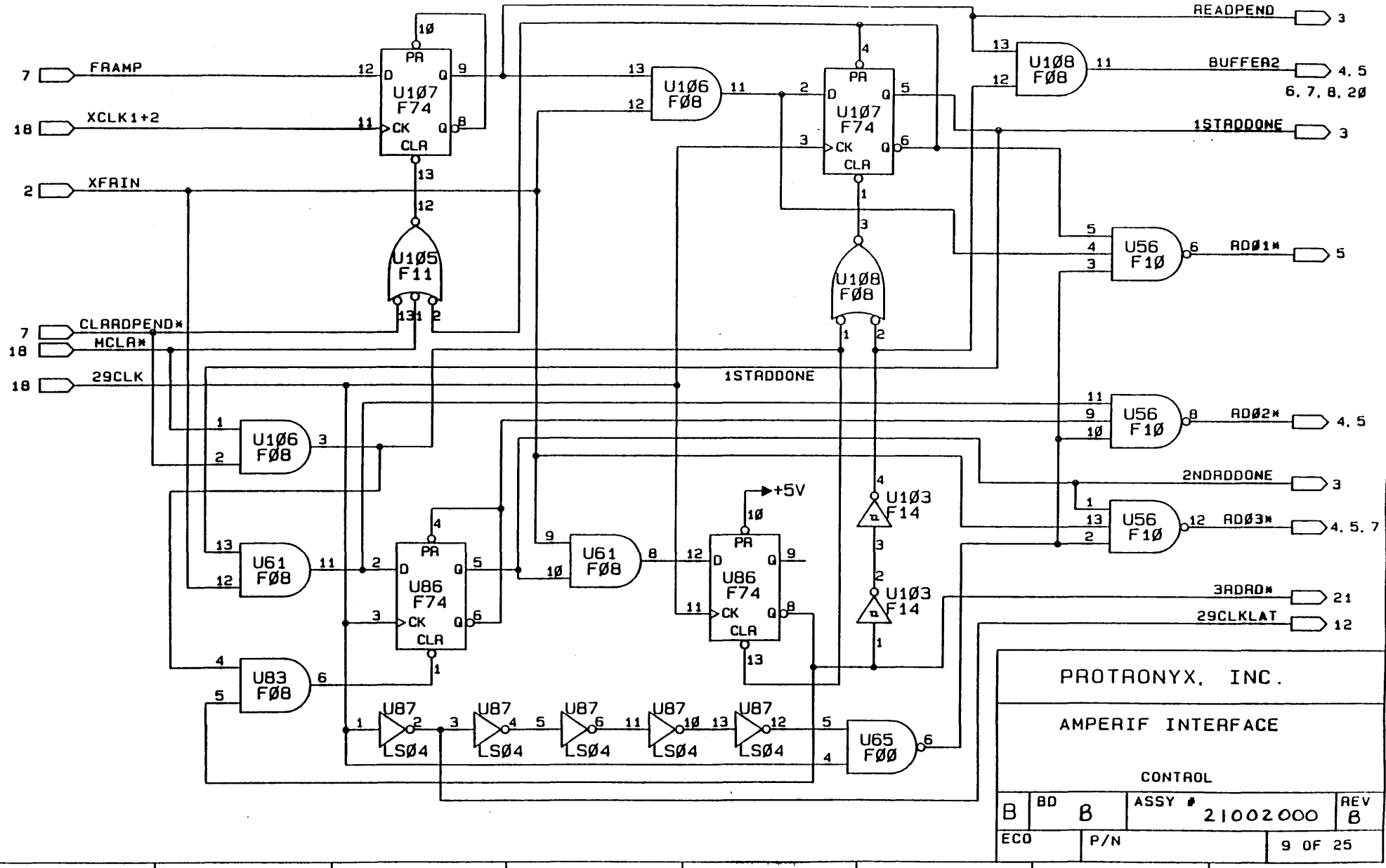
ECO 2588
SH 12



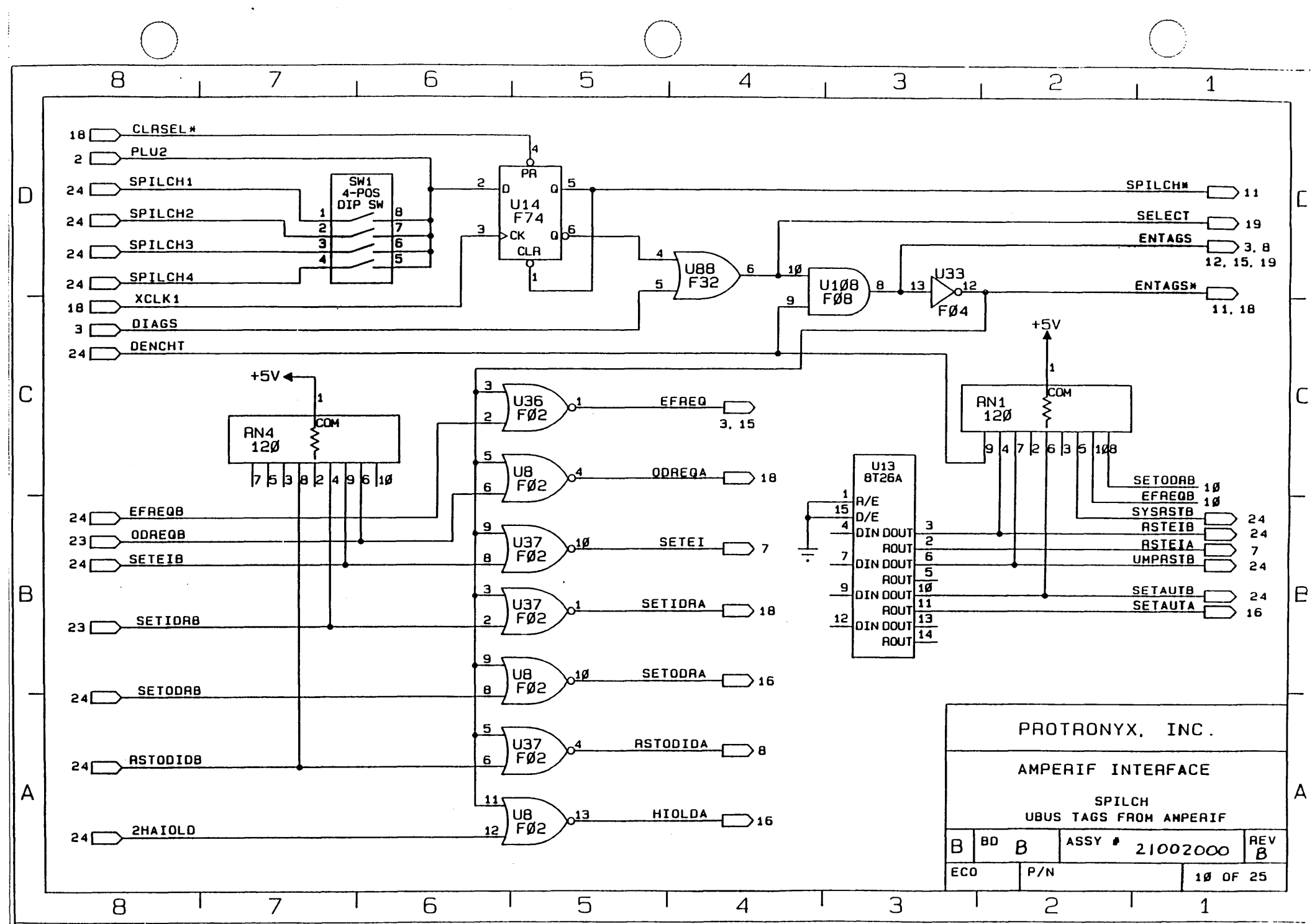
ECO 2588
SH 13



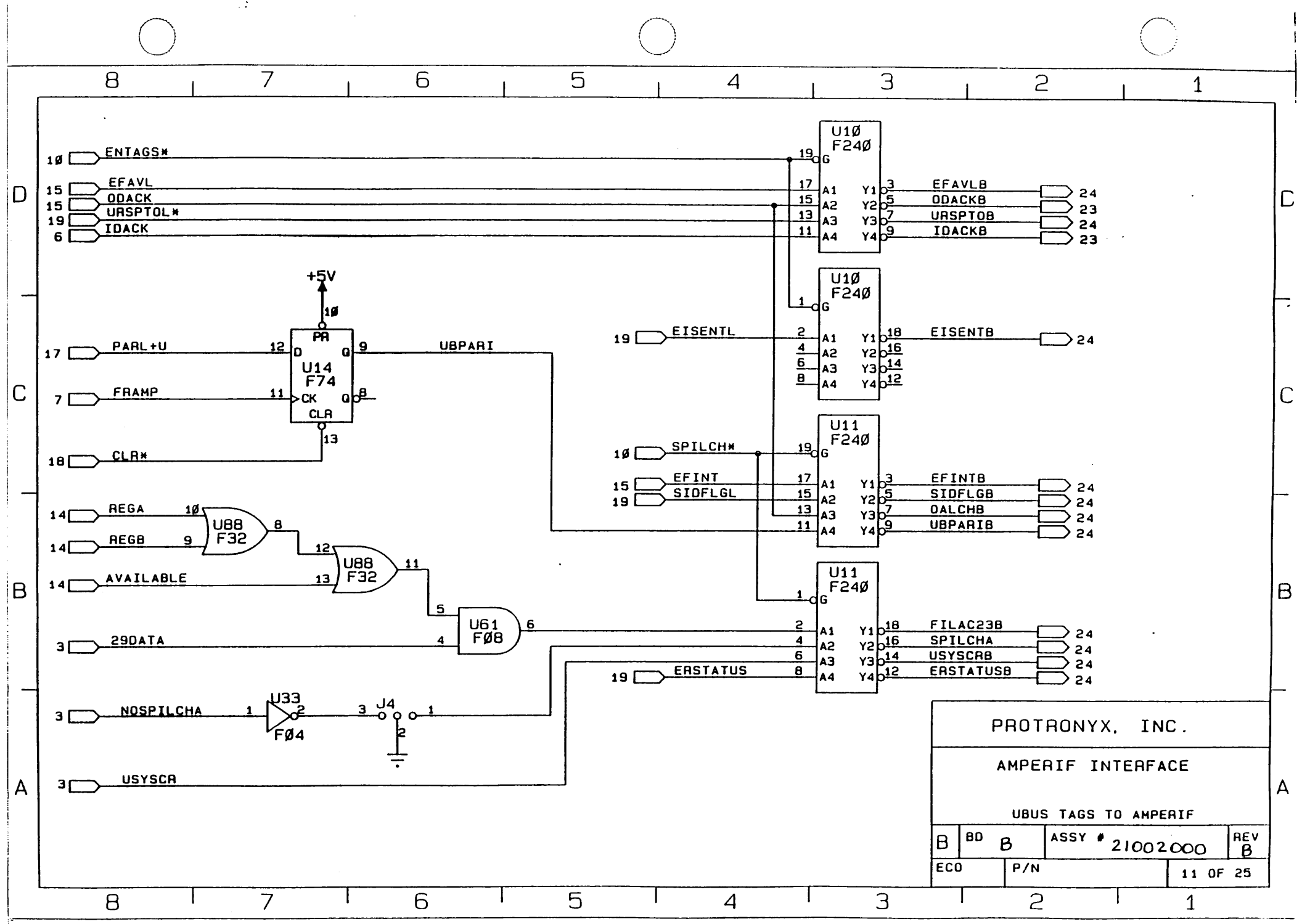
ECO 2588
SH 14



ECO 2588
SH 15



ECO 2588
SH 16



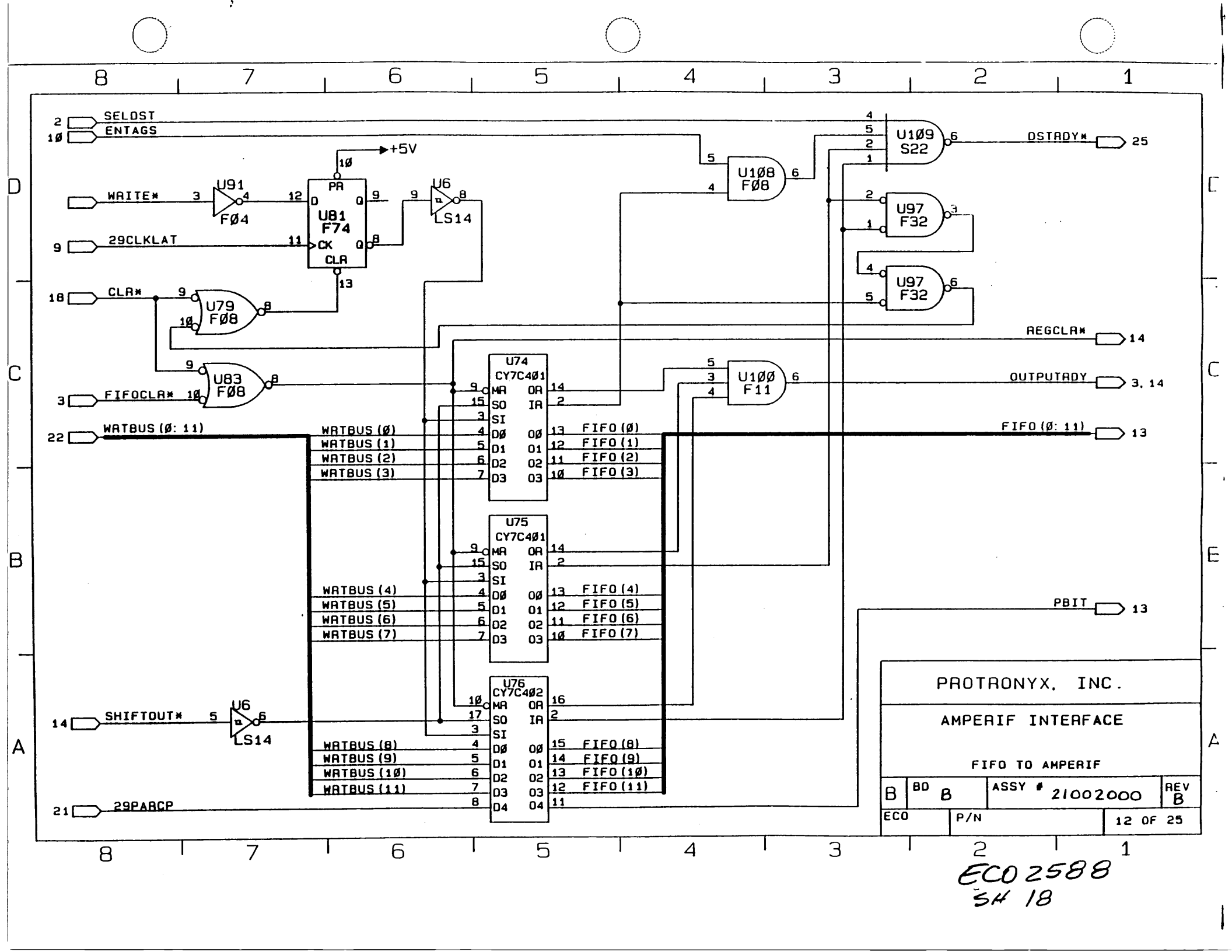
PROTRONYX, INC.

AMPERIF INTERFACE

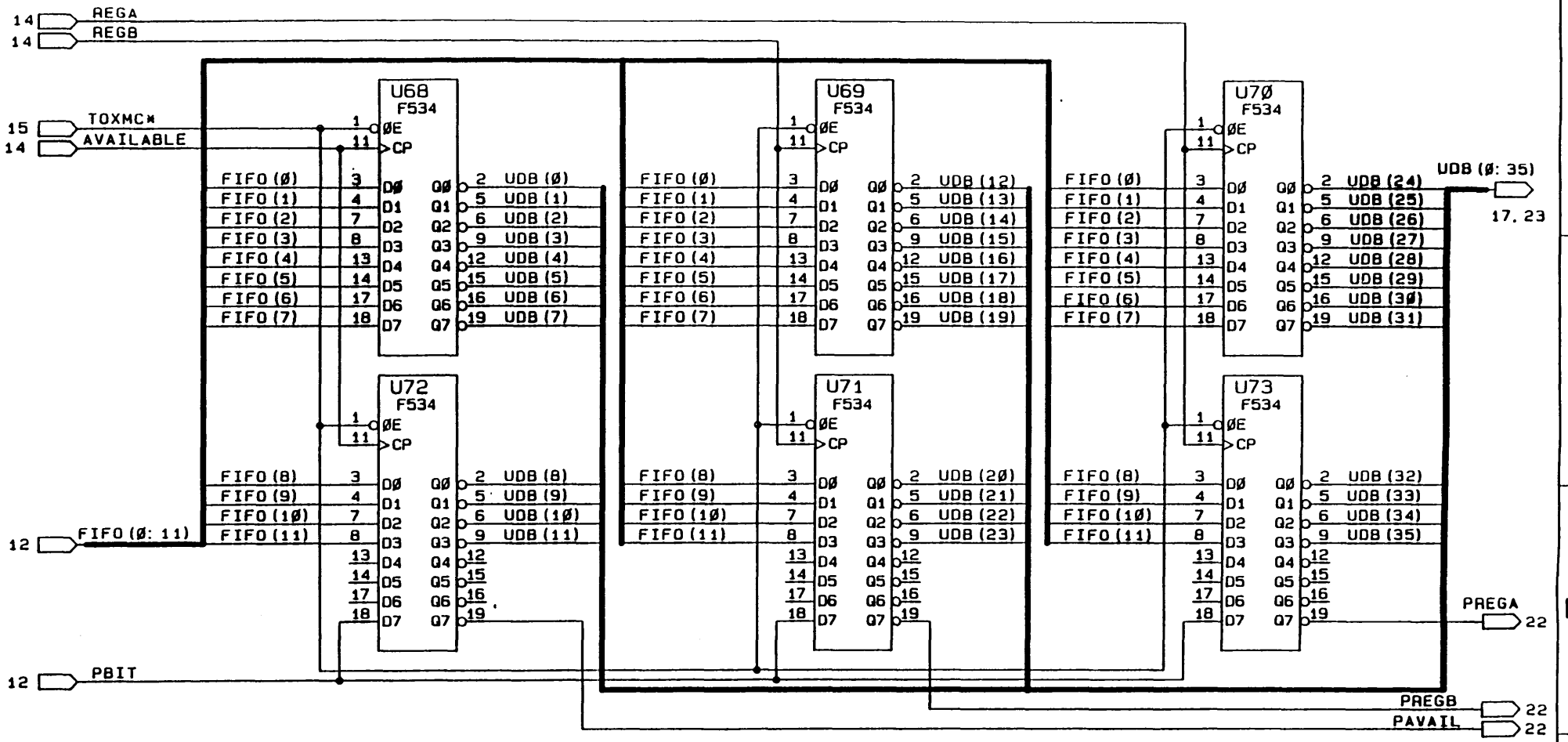
UBUS TAGS TO AMPERIF

B	BD B	ASSY # 21002000	REV B
ECO	P/N		11 OF 25

ECO 2588
SH 17

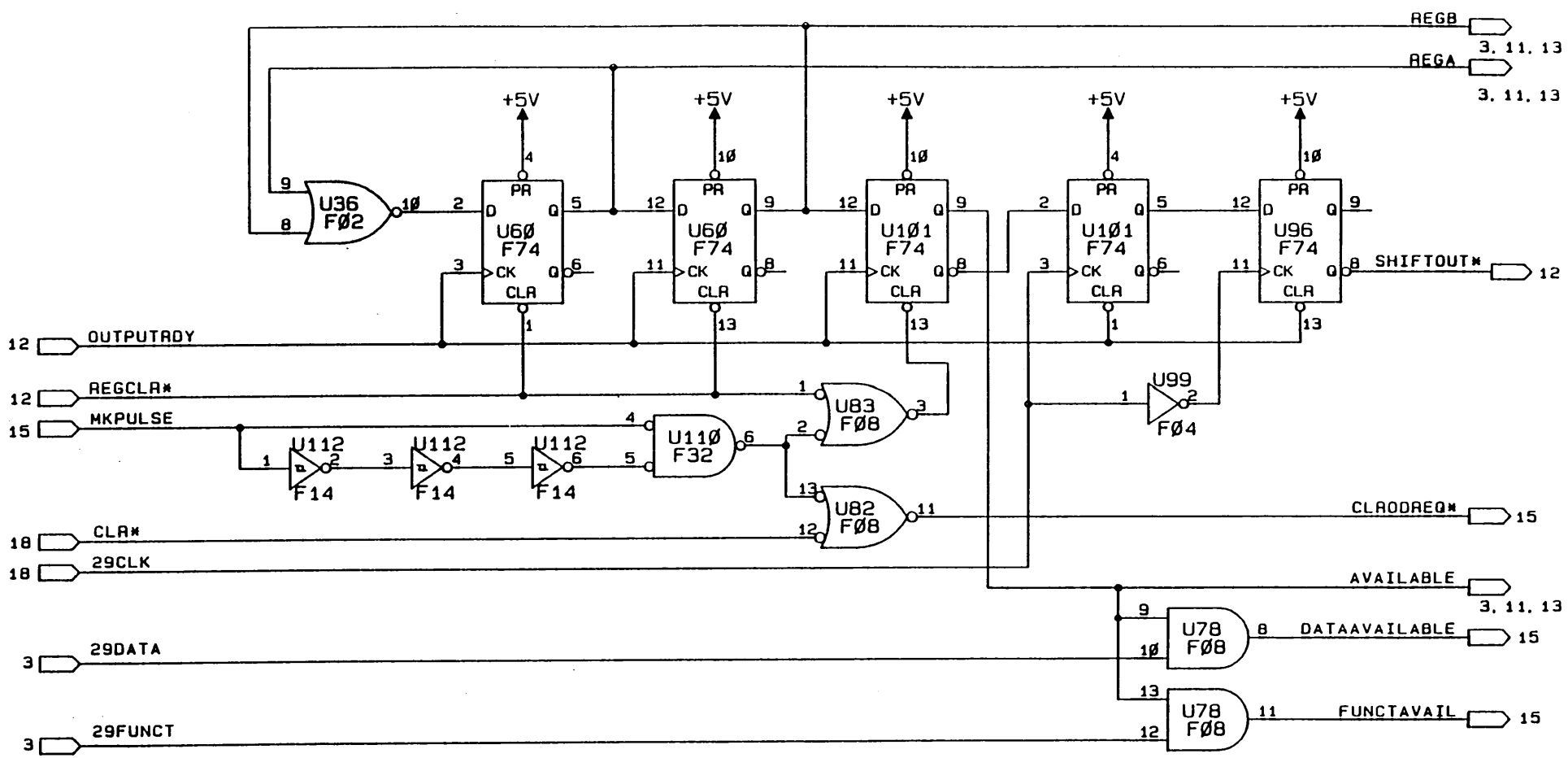


ECO 2588
SH 18


14 REGA
14 REGB
15 TOXMC*
14 AVAILABLE
12 FIFO (Ø: 11)
12 PBIT
U68 F534
U69 F534
U70 F534
U71 F534
U72 F534
U73 F534
ØE
CP
DØ D1 D2 D3 D4 D5 D6 D7
QØ Q1 Q2 Q3 Q4 Q5 Q6 Q7
FIFO (Ø) FIFO (1) FIFO (2) FIFO (3) FIFO (4) FIFO (5) FIFO (6) FIFO (7)
UDB (Ø) UDB (1) UDB (2) UDB (3) UDB (4) UDB (5) UDB (6) UDB (7)
FIFO (8) FIFO (9) FIFO (1Ø) FIFO (11)
UDB (8) UDB (9) UDB (1Ø) UDB (11)
UDB (12) UDB (13) UDB (14) UDB (15) UDB (16) UDB (17) UDB (18) UDB (19)
UDB (2Ø) UDB (21) UDB (22) UDB (23)
UDB (24) UDB (25) UDB (26) UDB (27) UDB (28) UDB (29) UDB (3Ø) UDB (31)
UDB (32) UDB (33) UDB (34) UDB (35)
UDB (Ø: 35)
17, 23
PREGA 22
PREGB 22
PAVAIL 22

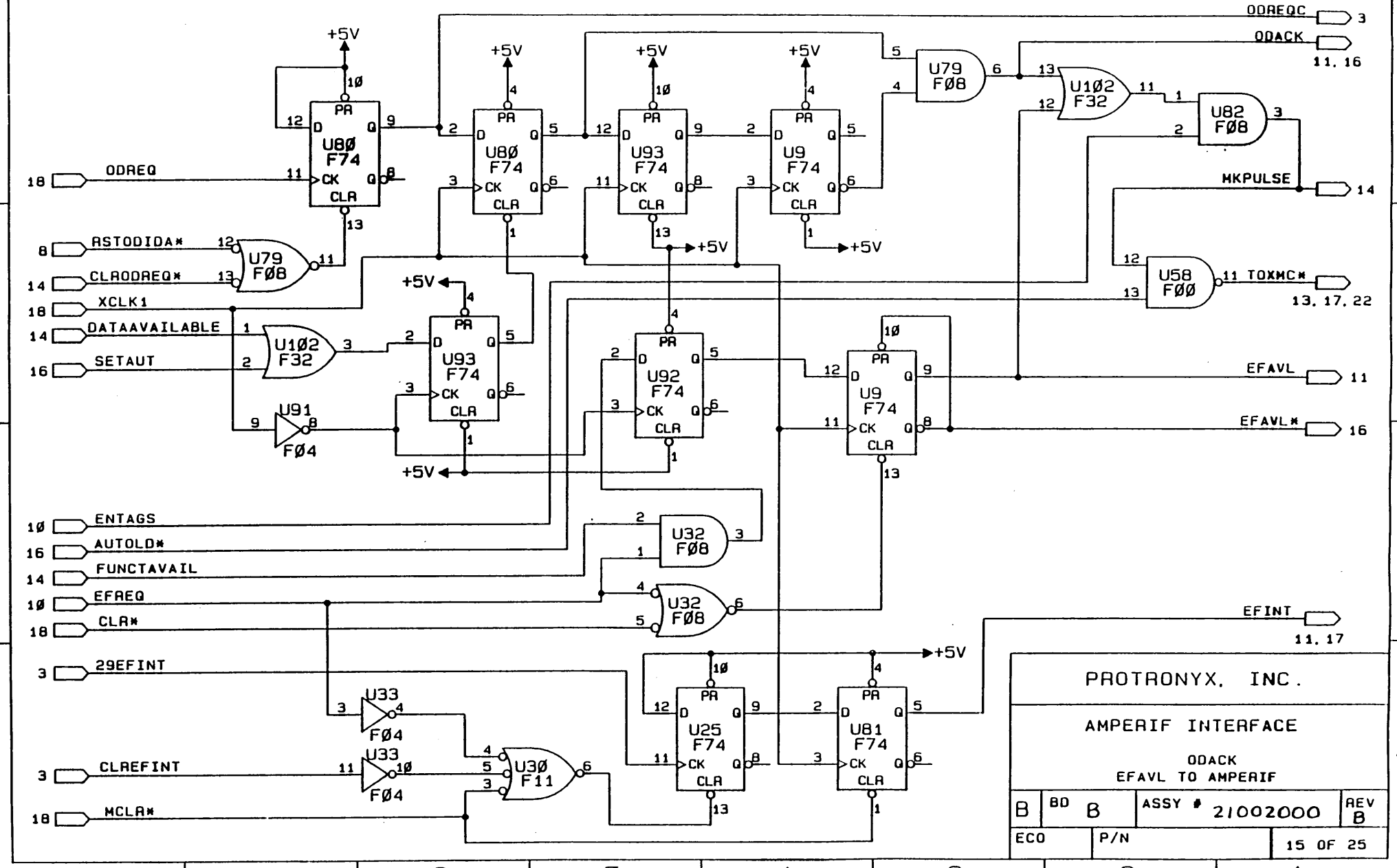
PROTRONYX, INC.			
AMPERIF INTERFACE			
REGISTERS A & B			
B	BD B	ASSY # 21002000	REV B
ECO	P/N		13 OF 25

ECO 2588
SH 19

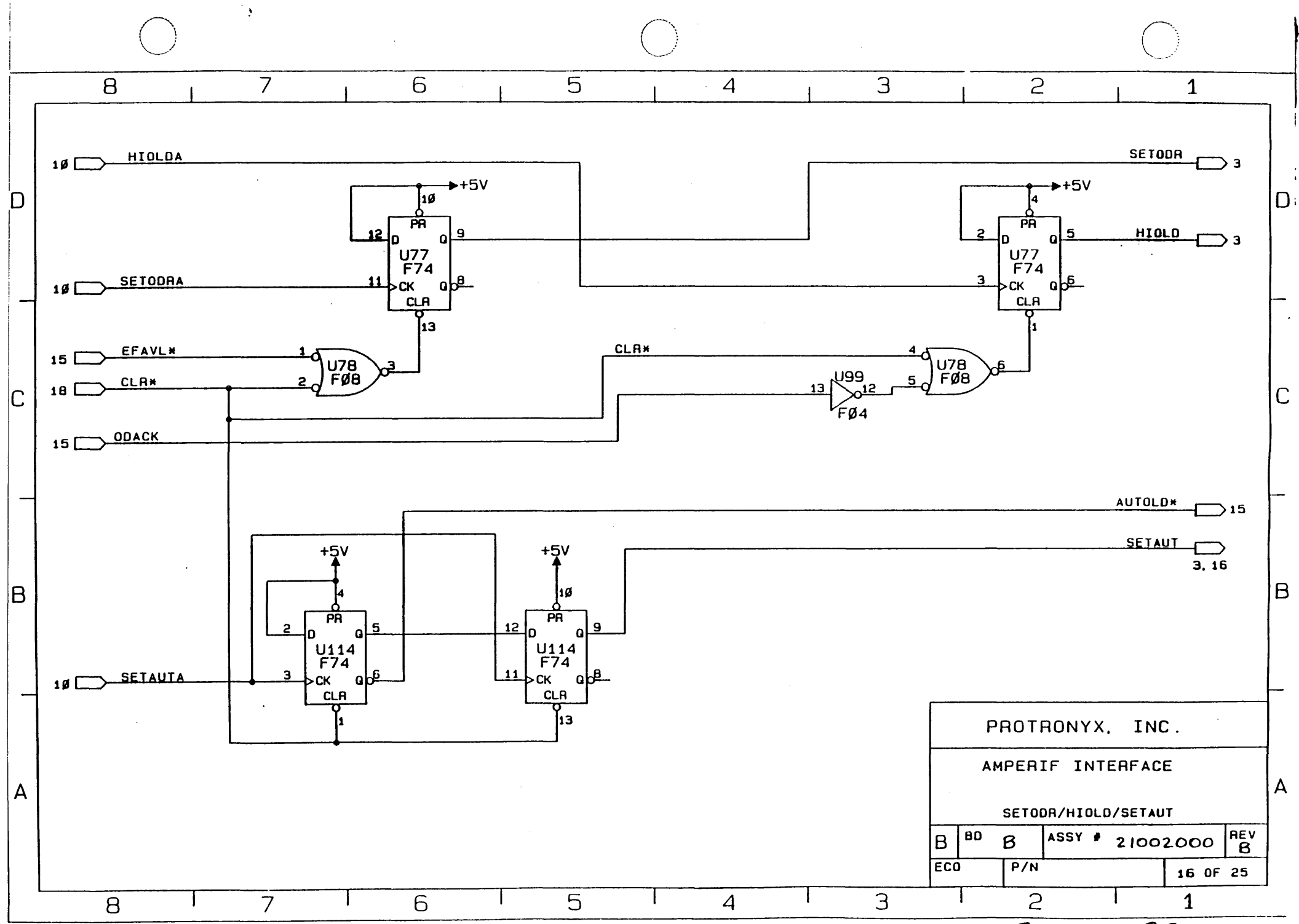


PROTRONYX, INC.			
AMPERIF INTERFACE			
FIFO SHIFTOUT AND REGISTER CONTROL			
B	BD B	ASSY # 21002000	REV B
ECO	P/N		14 OF 25

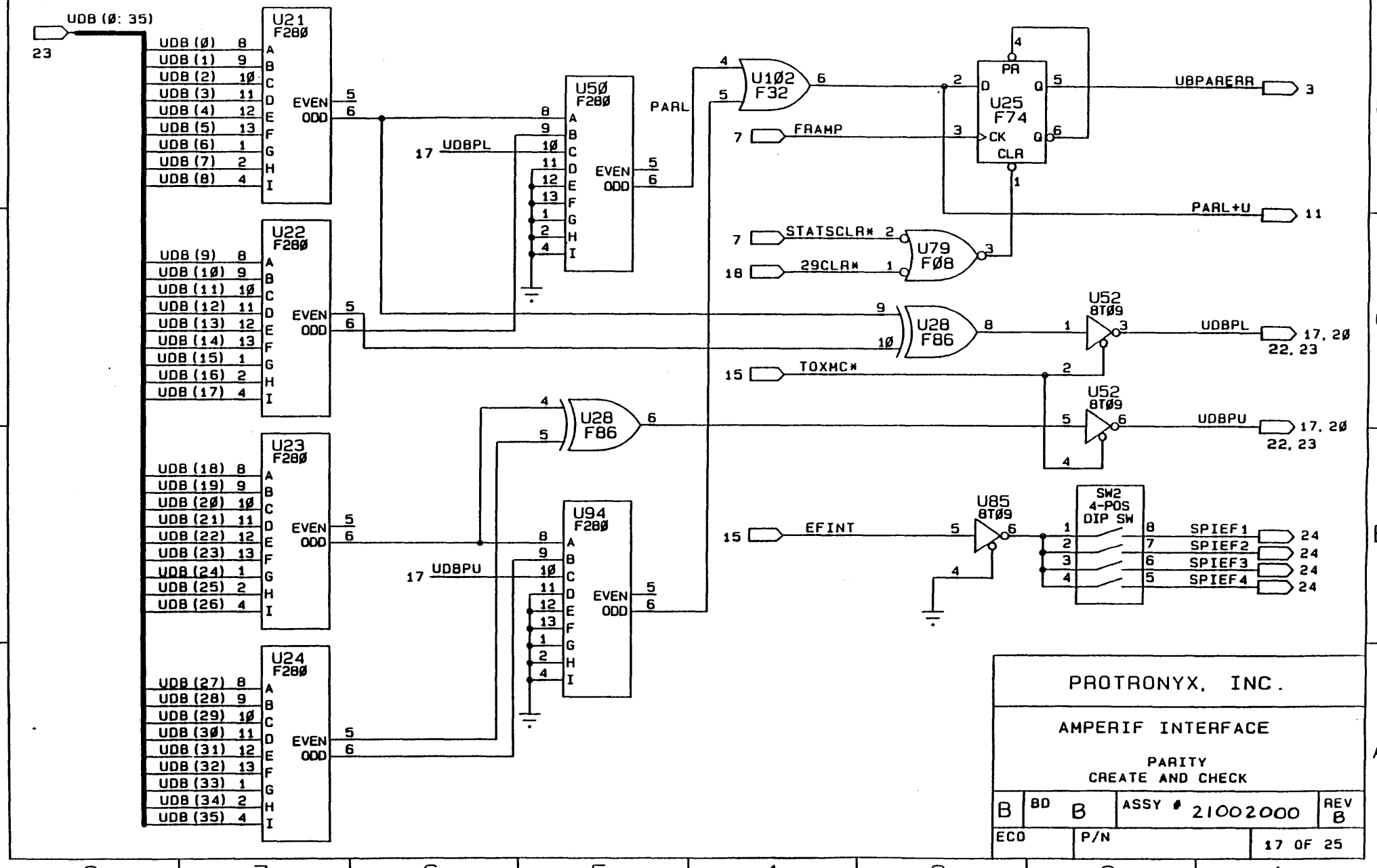
ECO 2588
SH 20



ECO 2588
SH 21



ECO 2588
SH 22



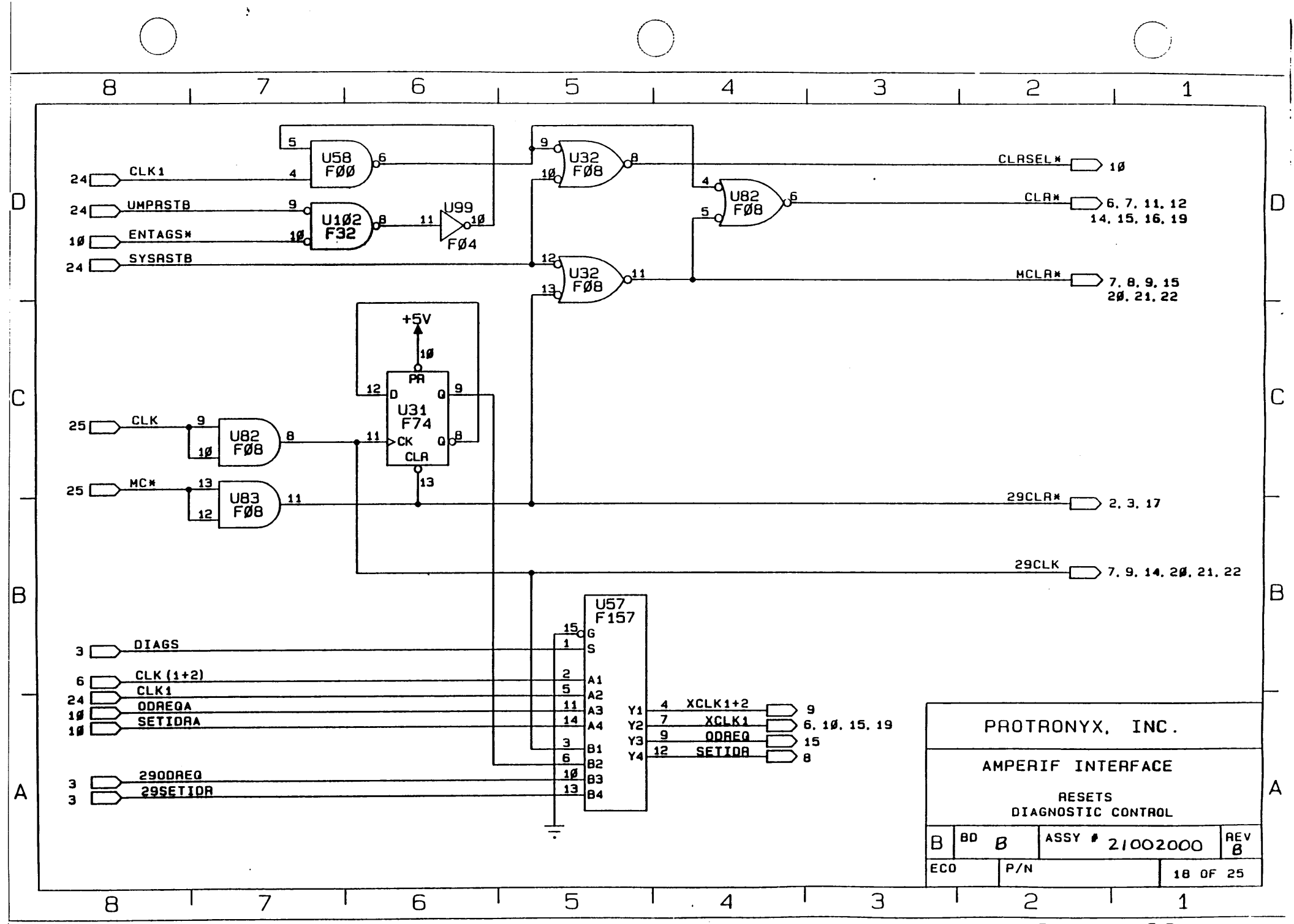
PROTRONYX, INC.

AMPERIF INTERFACE

PARITY
CREATE AND CHECK

B	BD B	ASSY # 21002000	REV B
ECO	P/N		17 OF 25

ECO 2588
SH 23



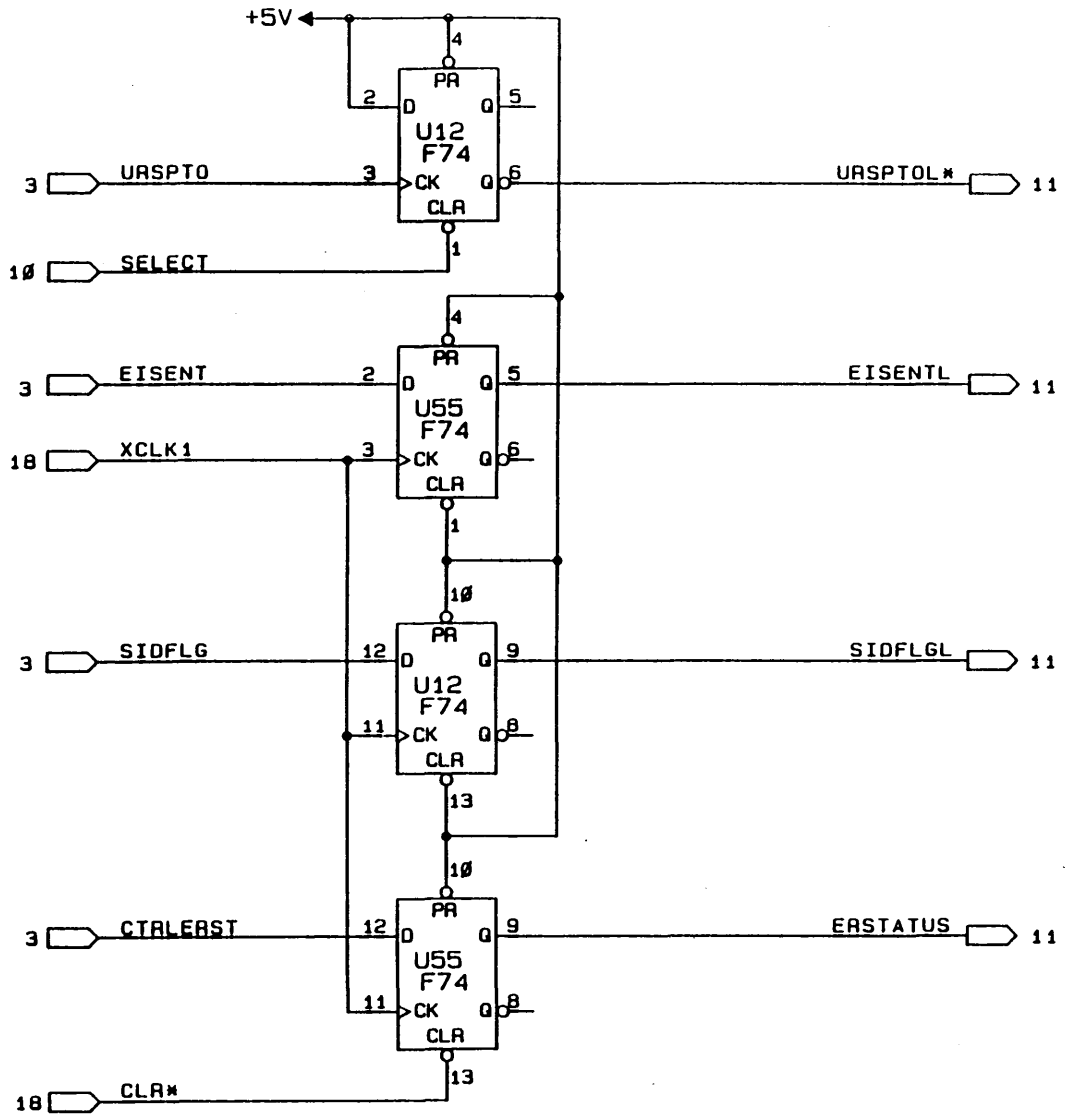
PROTRONYX, INC.

AMPERIF INTERFACE

RESETS
DIAGNOSTIC CONTROL

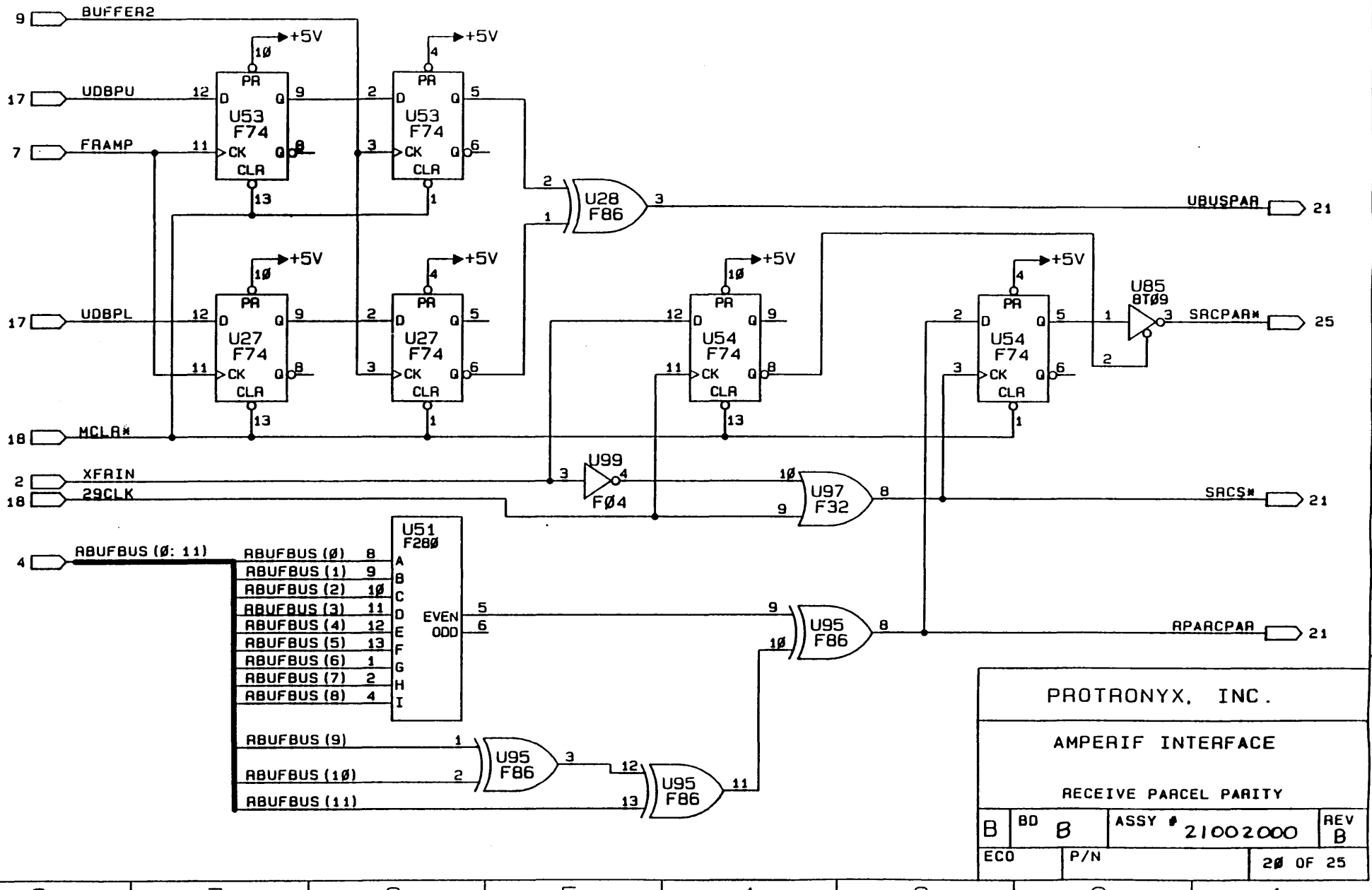
B	BD B	ASSY # 21002000	REV B
ECO	P/N		18 OF 25

ECO 2588
SH 24



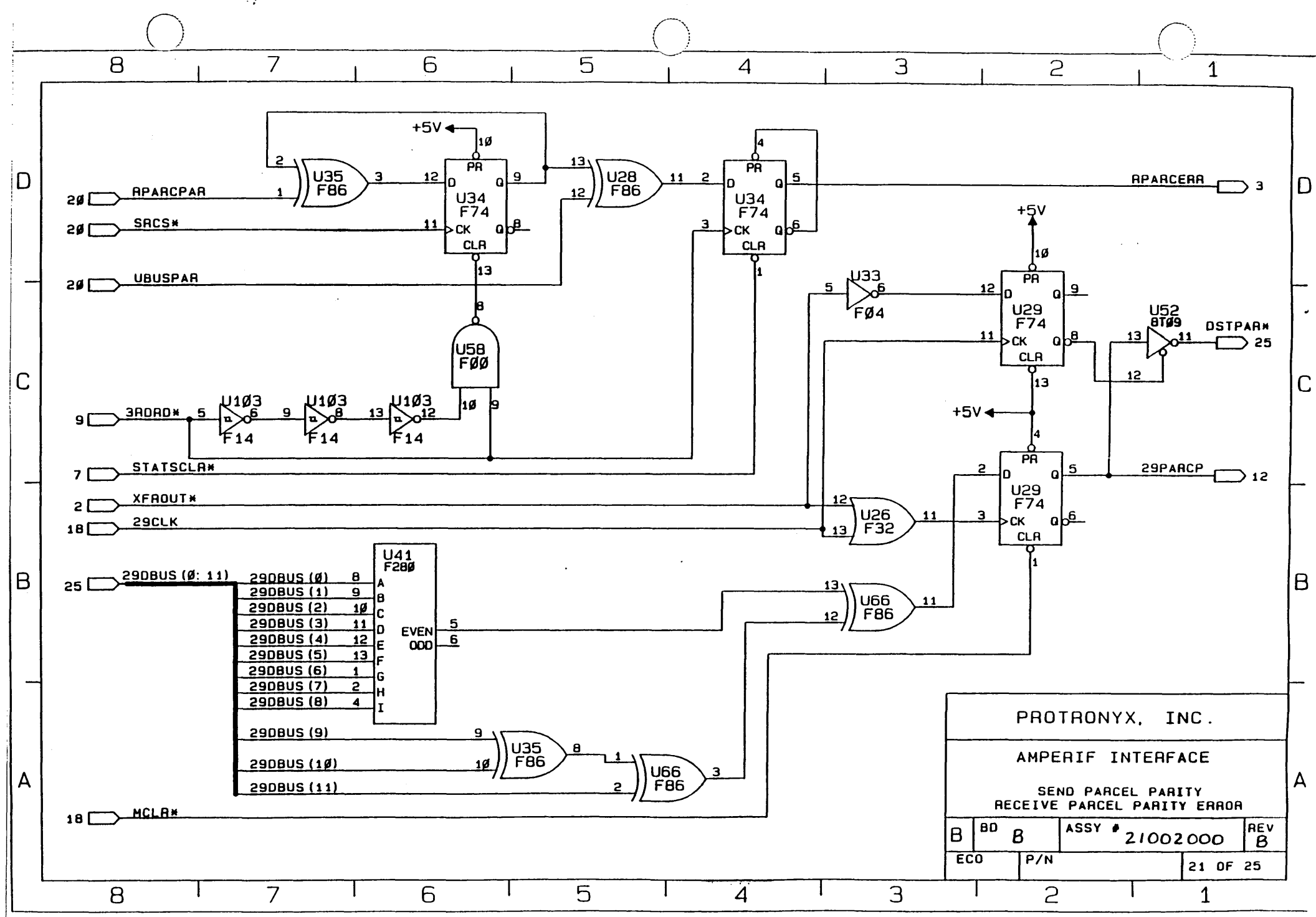
PROTRONYX, INC.			
AMPERIF INTERFACE			
B	BD B	ASSY # 21002000	REV B
REV	P/N		19 OF 25

ECO 2588
SH 25

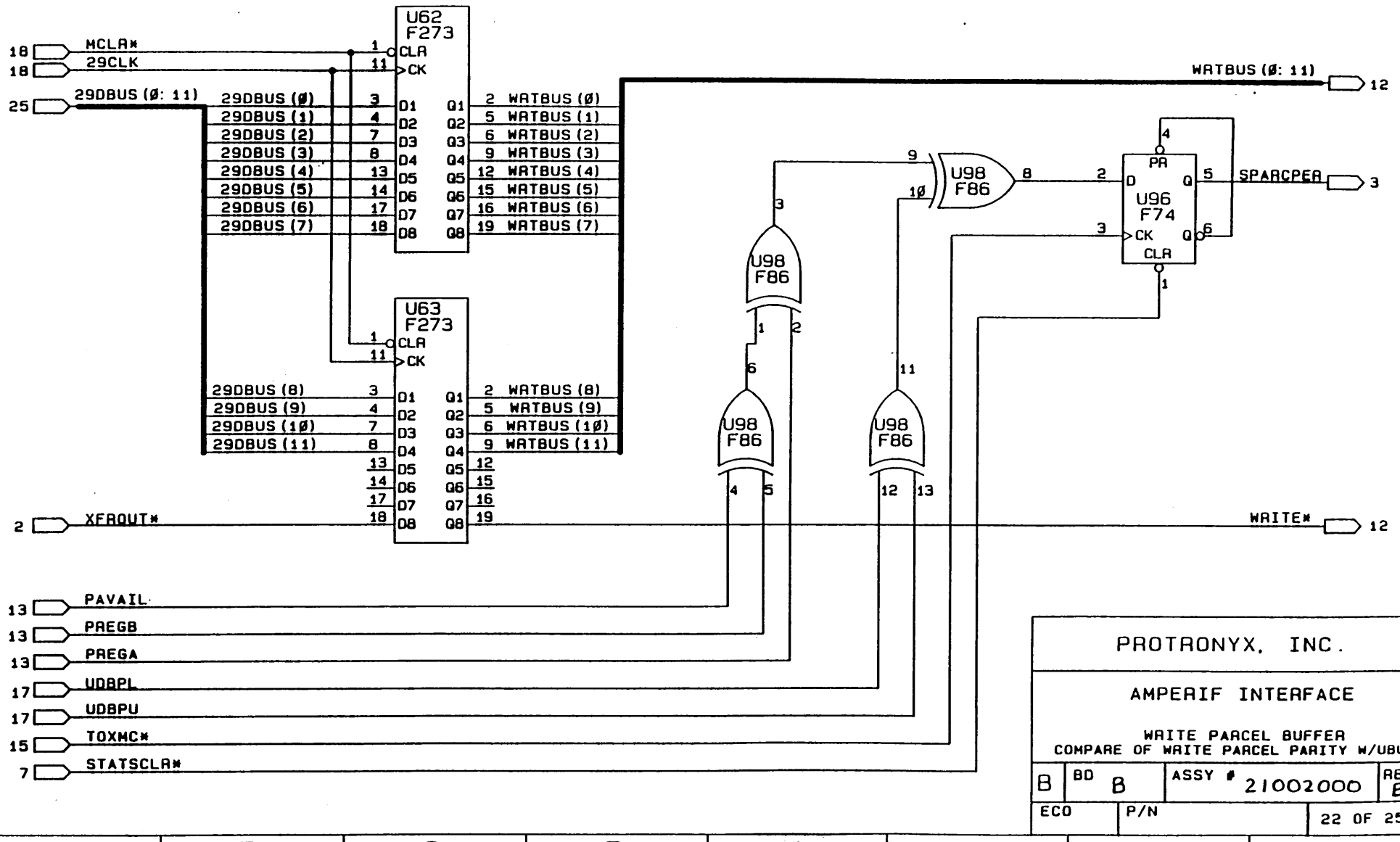


PROTRONYX, INC.			
AMPERIF INTERFACE			
RECEIVE PARCEL PARITY			
B	BD B	ASSY # 21002000	REV B
ECO	P/N		2Ø OF 25

ECO 2588
SH- 26



ECO 2588
SH 27



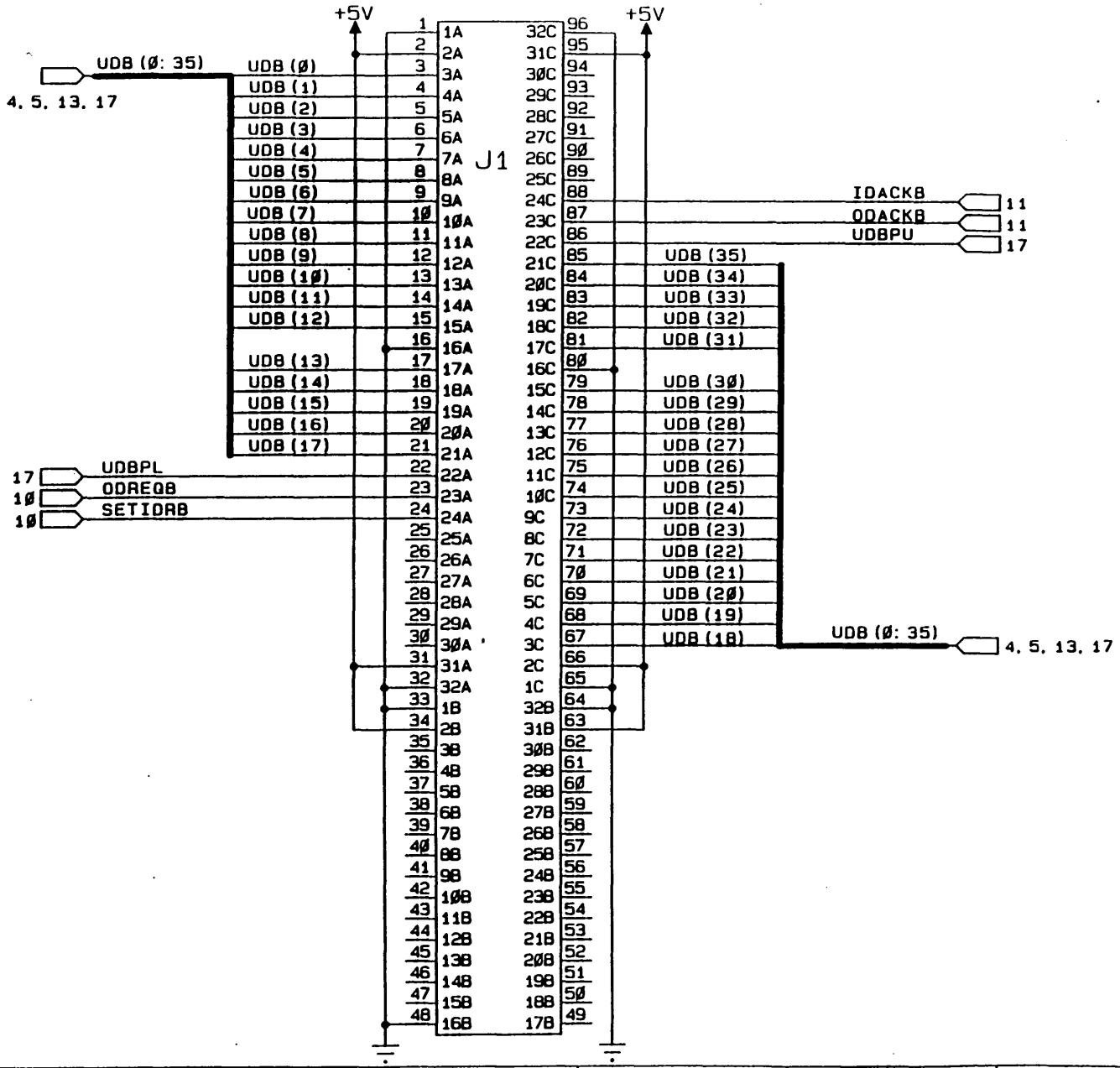
PROTRONYX, INC.

AMPERIF INTERFACE

WRITE PARCEL BUFFER
COMPARE OF WRITE PARCEL PARITY W/UBUS

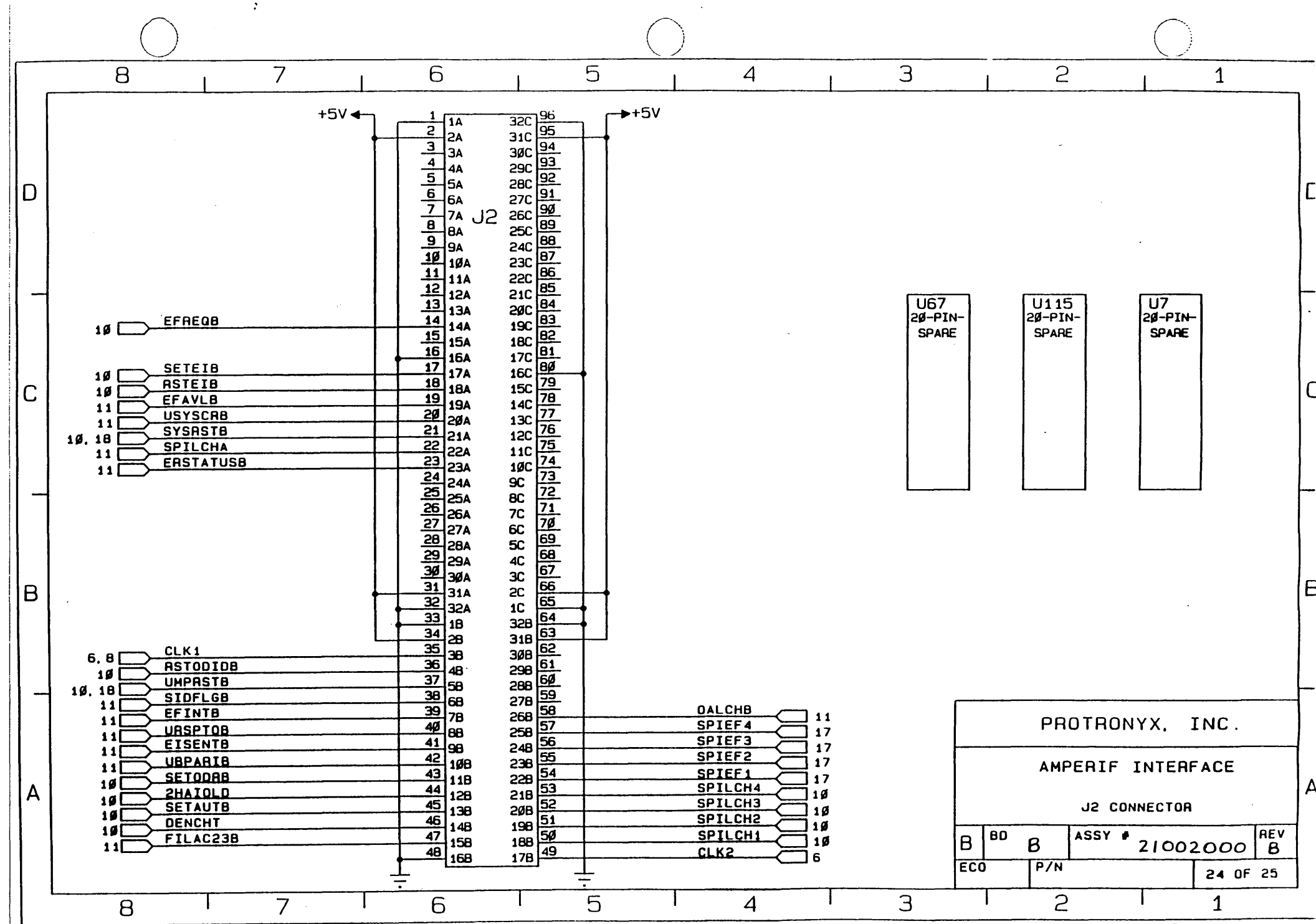
B	BD B	ASSY # 21002000	REV B
ECO	P/N		22 OF 25

ECO 2588
SH 28

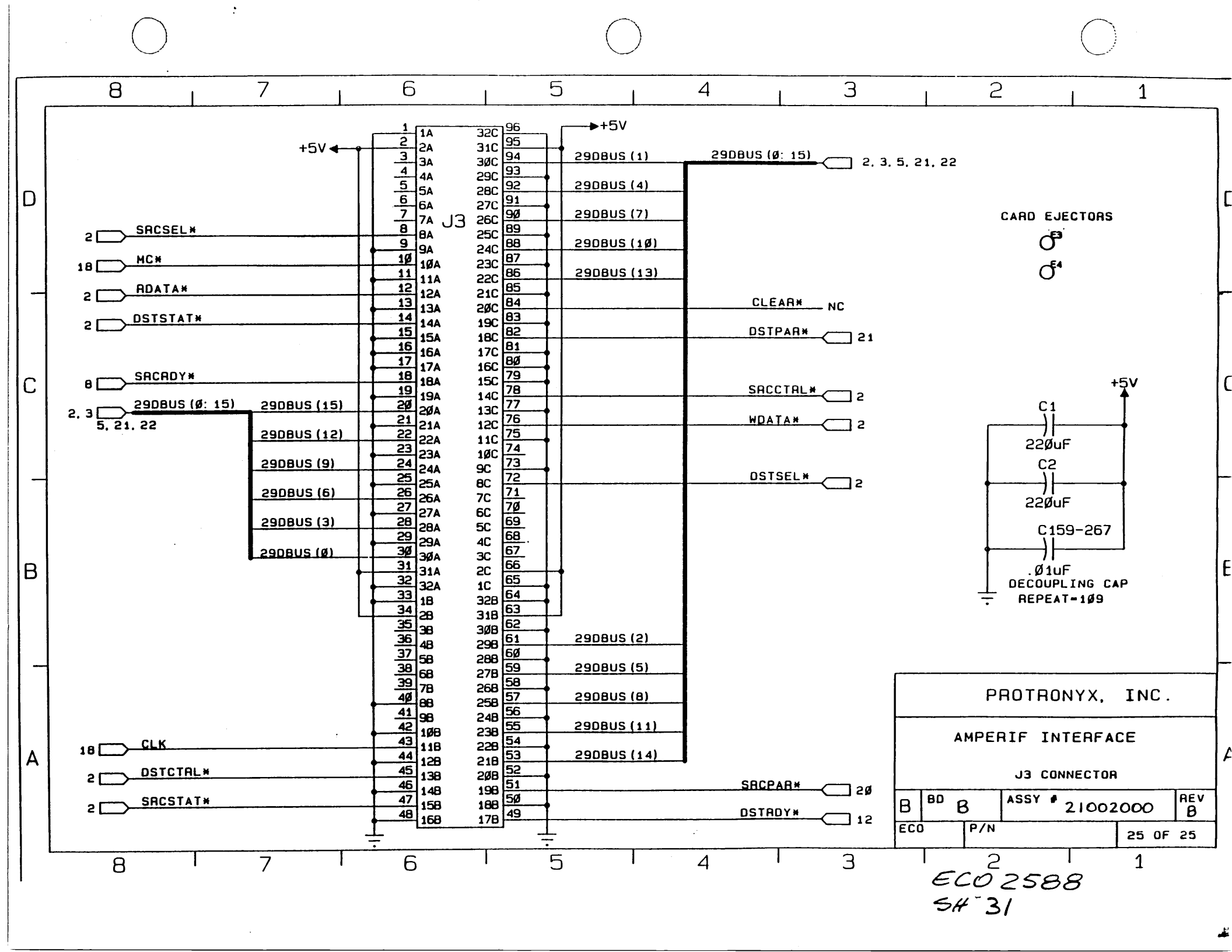


PROTRONYX, INC.				
AMPERIF INTERFACE				
J1 CONNECTOR				
B	BD B	ASSY # 21002000		REV B
ECO	P/N		23 OF 25	

ECO 2588
SH 29



ECO 2588
SH 30



ECO 2588
SH 31

AMPERIF COMPANY HISTORY

1971-1975

The Company was incorporated in California in 1971. From its inception 1971 to 1975, Amperif was engaged in the consulting business.

1976

Amperif designs and produces the first peripheral mass storage system using semiconductor memory. The Solid State Drum or SSD introduced unprecedented performance levels to the mass storage industry, accessing information 20 times faster than conventional drum storage systems.

1978

Amperif begins using dynamic random access memory chips (DRAM's) to increase the speed of the system.

1980

Amperif designs and manufactures the first Cache Disk System for a large scale computer. The 5046 represented a major breakthrough in storage device technology with the use of "Cache" memory. Cache/disk memory devices are intelligent solid state memory systems placed between the mainframe and the disk drive. The Controller's microcode programs decide which data to hold in the high speed solid state "Cache" memory and which data to hold in disk memory. Depending on the application the average user can expect a "hit rate" , or the number of times a the data is found in Cache, of between 80% and 90%. A 5046 with Cache is able to access information 4 to 7 times faster than a conventional disk system by using Cache.

1982

Amperif delivers the first commercial back-end database machine for a large scale computer. The RDM-1100 is a hardware version of a relational database management system. The RDM-1100 offloads data management functions from the host computer, resulting in improved operating efficiency of the mainframe and enhancing the utilization of data bases by allowing access by up to four mainframes.

1983

Amperif introduces the Challenger I, a compact high performance cache disk system which provides two controllers, 1.8 gigabytes of disk storage, and up to 27 megabytes of cache or solid state storage in a cabinet occupying 12.5 square feet of floorspace. The Challenger I uses four CDS 513 (19" HDA) disk drives with a capacity of 513 megabytes each.

1984

The RDM-1100 is improved to provide higher performance with the addition of a Database Accelerator (DAC). The unit is also re-packaged to use the CDS 513 (19" HDA) disk drive.

1985

Amperif introduces the Challenger II Cache Disk System. The Challenger II, which uses a disk array design, can provide more than 4.5 gigabytes of high performance (SMD-E) disk storage, 10 megawords of cache memory and 10 megawords of solid state storage in a 12 square foot floorspace. Disk expansion cabinets can be added to increase the total to 64 disk drives for a total capacity of 18 gigabytes. The Challenger II also offers greater reliability and maintainability with the use of 256K DRAM memory chips, pluggable board assemblies and sixteen Fujitsu 2333 8" disk drives with a capacity of 337 megabytes each.

1986

Amperif enters into two agreements with the Sperry (UNISYS) Corporation. The Third Party Service (TPS) contract provides continued support for Amperif products in the field via the Unisys TPS Customer Engineering organization. The OEM contract provides Unisys with exclusive rights to market the Amperif Sierra Cache Disk System. The Sierra Cache Disk System can provide more than 5 gigabytes of high performance (SMD-E) disk storage, 10 megawords of cache memory and 10 megawords of solid state storage in a 12 square foot floorspace. Disk expansion cabinets can be added to increase the total to 64 disk drives for a total capacity of 20 gigabytes.

The Sierra Cache Disk System is improved with the new 2 channel Host Adapters (2-HAIO) which have a transfer rate of 845 kilowords per second and the new XM16KP board with a pluggable EPROM daughter board for easy microcode updates. The Sierra Cache Disk System uses sixteen CDC 8" 9720 disk drives with a capacity of 368 megabytes each.

1987

The Sierra Cache Disk system is again improved with data path through checking and rotational position sensing (RPS). Amperif releases several diagnostic improvements including 1) Disk Diagnostic Test (DDT) version 4R1, an online test package, 2) the Controller Confidence Test (CCT), a power on/reset confidence test, and 3) a freestanding diagnostic microcode cartridge.

Sierra Plateau 5 is released to Unisys customers under Type numbers 5090-xx (Cache Disk System), 8490-xx (Disk Expansion) and the 7059-xx (Memory Expansion).

Amperif acquires Protronics Inc.. Based in Boulder Colorado, Protronics designs and manufacturers CDC compatible adapters for peripheral equipment.

Amperif introduces the model 7000 Cache Disk System for CDC 170/180 Series Cyber channel compatibility. The 7000, which uses a disk array design, can provide up to 13 gigabytes of high performance (SMD-E) disk storage, 35 megabytes of cache memory and 45 megabytes of solid state storage in a 12 square foot floorspace. The model 7000 uses sixteen Fujitsu 8" Swallow 5 disk drives with a capacity of 837 megabytes each.

Amperif designs and builds a 3 Megabyte Cache Disk System in response to a Unisys RPQ. The 3Mb system achieves a 3 megabyte transfer rate by using Emitter Coupled Logic (ECL) to drive the SMD-E signals out to the eight Fujitsu 8" Swallow 5 disk drives. Each Swallow 5 disk drive has a capacity of 837 megabytes.

1988 and beyond

The Database Computer or DBC is a more technologically advanced relational database management system. The system takes advantage of improvements in technology such as caching and parallel processing. The DBC is being developed to be compatible with Unisys 1100 and IBM 4300 and 30XX series computers.

The Challenger III will represent the next generation of Cache Disk Systems from Amperif. Improvements include cache memory integrated into the controller cardcage and a host adapter cardcage to allow easy adaptation to any host environment. The unit will be designed and packaged to be even faster and smaller than existing products.